A New PWM Strategy for Grid-Connected Half-Bridge Active NPC Converters With Losses Distribution Balancing Mechanism

Lin Ma, Tamas Kerekes, Pedro Rodriguez, Xinmin Jin, Remus Teodorescu, *Fellow, IEEE*, and Marco Liserre, *Fellow, IEEE*

Abstract—Photovoltaic systems technological development is driven by the request for higher efficiency and safety. These concerns influence also the choice of the power converter stage. Several topologies have been proposed and many of them are available commercially. Among them, the neutral point clamped (NPC) and derived topologies offers high efficiency, low leakage current, and low EMI. However, one main disadvantage of the NPC inverter is given by an unequal distribution of the losses in the semiconductor devices, which leads to an unequal distribution of temperature that can affect lifetime. By using the active NPC (ANPC) topology, where the clamping diodes are replaced by bidirectional switches, the power losses distribution problem is alleviated. The modulation strategy is a key issue for losses distribution in this topology. In this paper, two known strategies are discussed and a new PWM strategy, namely the adjustable losses distribution is proposed for better losses distribution in the ANPC topology. Simulations and experimental results help in evaluating the modulation strategies.

Index Terms—Active NPC (ANPC), adjustable losses distribution (ALD), NPC, PV system.

I. INTRODUCTION

SINGLE-PHASE photovoltaic (PV) systems (1–10 kW) are attractive distributed power generation system in household applications. Hence, they have specific needs such as maximum profitability through high efficiency, long lifetime, low prices, small volume, and safety [1], [2]. In order to improve the efficiency of household PV inverters and lower the system prices, isolation transformers used in the past to interface the PV system with the electric grid in order to provide higher safety and lower leakage current is typically not present in the new generation of PV systems. Thereby, many transformerless applications were proposed [3]–[6], including HERIC topology [7], full-bridge (FB) with dc bypass topology [8], H5 topology [9], Neutral Point Clamped (NPC) topology, Conergy NPC topology, and active NPC (ANPC) topology. All these voltage source transformerless PV inverter topologies can be classified in two groups: One is the topologies derived from conventional FB topology as HERIC, H5, and FB with dc Bypass topology; the other group is the topologies derived from conventional half-bridge NPC topology as NPC, Conergy NPC, and ANPC.

The NPC topology was proposed by Baker in a patent in 1970s, in 1981 for the first time stated in the paper by Nabae, Takahashi, and Akagi in [10] and it has been proven to provide high efficiency and to allow connection to the grid without step-up transformer [11], [12]. Compared with the traditional two-level FB PWM inverters, the NPC topology inverters produce no common-mode current, which make it appealing for PV application [13]. Meanwhile, one disadvantage of the NPC inverter is given by an unequal distribution of the losses in the semiconductor devices, which leads to an unequal distribution of temperature and limits the output power of the inverter. In order to overcome this drawback, the conventional NPC topology was extended to the ANPC structure [14], [15].

Compared with the conventional NPC topology, the total efficiency of the ANPC topology is not improved, but this topology has more switching states freedom degrees, which could be used in dc-bus voltage balancing applications [16]–[19], which is another essential for all NPC topologies. Some of the ANPC PWM strategies were also used for balancing the losses distribution [20], [21], but all of them were not optimal.

This paper introduced two ANPC PWM strategies [20], [21] used for balancing the power losses distribution and proposed a novel PWM strategy named adjustable losses distribution (ALD) for better losses distribution balancing. This modulation method could adjust the switching losses distribution depended on different switches conduction loss distribution. By using this method, it could optimal the total switches losses distribution.

Simulation and experimental results are given to validate that the proposed strategy has better losses distribution performance, which could enlarge the components and inverter SOA areas.

II. POWER UNBALANCE DRAWBACKS OF HALF-BRIDGE NPC TOPOLOGY

Due to the structure of PV panels, the leakage capacitance between the PV panels' output terminals and ground reaches a significant value. In order to save using isolation transformers, the conventional half-bridge NPC topology is a popular topology that is used in PV inverter applications [22], [23]. In half-bridge NPC converters, zero voltage can be achieved by "clamping" the

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T. Kerekes, P. Rodriguez, R. Teodorescu, and M. Liserre are with Aalborg University, 9100 Aalborg, Denmark (e-mail: tak@iet.aau.dk; prodriguez@ee.upc.edu; ret@et.aau.dk; liserre@gmail.com)

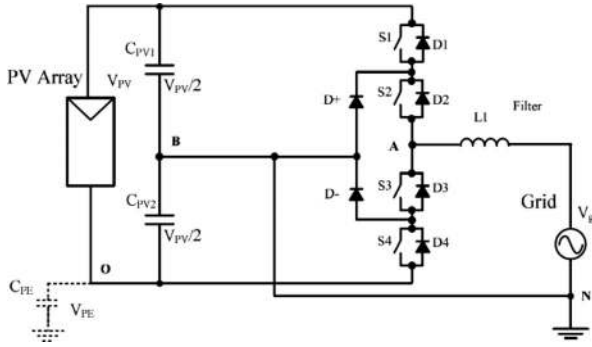X. Jin is with Beijing Jiao Tong University, 100044 Beijing, China (e-mail: jinxm@bjtu.edu.cn;).

Fig. 1. NPC Half Bridge.

TABLE I
SWITCHES STATES OF NPC HALF-BRIDGE INVERTER

Voltage	S1	S2	S3	S4
Positive	1	1	0	0
0^+	0	1	1	0
0^-	0	1	1	0
Negative	0	0	1	1
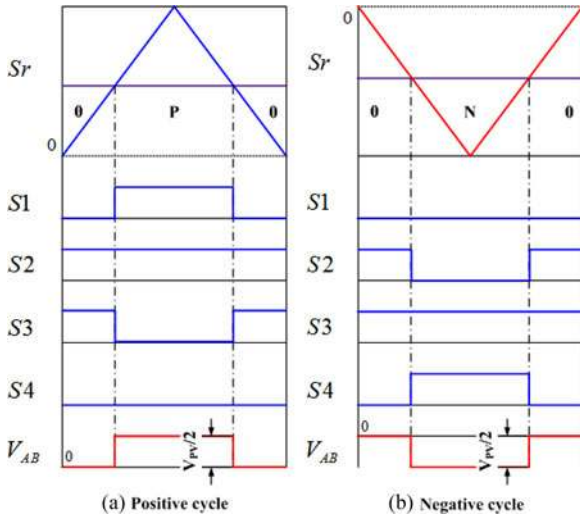
Fig. 2. Sinusoidal PWM for conventional NPC half-bridge inverter, (a) $Sr > 0$ and (b) $Sr < 0$.

Fig. 3. Switching losses of a 5-kW NPC topology inverter at different frequencies, $M = 0.9$ and $PF = 1$. (a) Switching frequency at 10 kHz. (b) Switching frequency at 16 kHz.

output to the grounded "middle point" of the dc bus using D+ or D− depending on the sign of the output current. As presented in Fig. 1, by using this topology, the voltage V_{PE} is clamped to $V_{PV}/2$, the leakage current could not be generated through C_{PE}. All half-bridge topologies could be used in this kind of applications to eliminate the leakage current. However, the NPC half-bridge topology has three output voltage levels and better efficient performance.

Since this topology has just one zero state, the PWM method of half-bridge NPC has no more options. The commutation states and the switching PWM pattern of the NPC inverter are given by Table I and Fig. 2, where "0" stands for "OFF" state of IGBTs, while "1" stands for "ON" state of IGBTs. In Fig. 2, Sr is the output voltage reference sinusoidal modulation wave

which is generated by grid-connected current-loop controller [20], [21]. During the positive half cycle of the grid voltage, S2 is ON and only S1 switches at the switching frequency. Therefore, the dead time between S1 and S2 might be set to zero by using this PWM strategy. S3 and S4 work complementarily to S1 and S2, respectively.

Fig. 3 shows the switching losses of a 5-kW NPC topology inverter at different switching frequencies, which presents unbalance losses distribution among the semiconductors. This figure points out that the stresses due to switching losses on the outer switches S1 and S4 is higher than on the inner switches, especially at higher frequency [see Fig. 3(b)]. As the switching frequency increases, the uneven losses distribution in the NPC inverter gets even worse. For the grid-connected PV system, the modulation index (M) is often fixed when dc bus voltage and grid voltage are given, e.g., by using the traditional FB topology connected with 230-V RMS grid, usually using 400-V dc bus, the modulation index is set to $M = 0.9$.

In the case of half-bridge NPC topologies, the other obvious drawback is that these topologies need double dc-bus voltage compared with the traditional FB topology, which is the common drawback of all the half-bridge topologies. The higher dc-bus voltage usually needs more PV panels in series or using an additional dc/dc boost converter, but more PV panels in series would influent the maximum power point tracking, while using an additional dc/dc boost converter would decrease the efficiency of PV systems [24], [25]. Although by using dc/dc boost converter [26], cascade technique [27], or some other methods

TABLE II
SIMULATION PARAMETERS

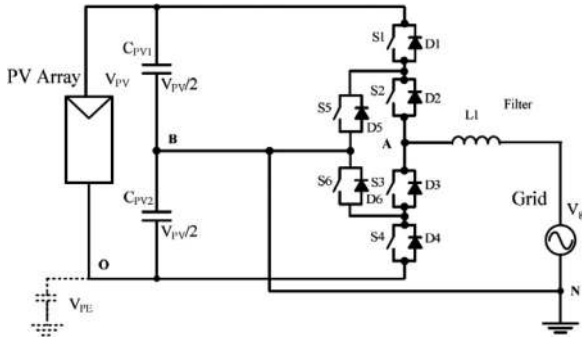| Quantity	Value	Comment
Simulation step	5 e–5 s	
Grid	230 V(RMS); 50 Hz	
Carrier frequency	10 kHz/16 kHz	
Output filter L	10 mH	
C_{DC}	1000 μF	Each dc bus
DC Bus voltage	800 V	400 V each level
Power rate	5000 W	
Switches	PM75DSA120	IPM
PF	1.0	
Modulation rate	0.9	

Fig. 4.   ANPC Half Bridge.

[28] could solve this problem ideally; it usually introduces more facilities.

In this paper, all the simulation models parameters are shown in the Table II.

III. ANPC CONVERTER

The ANPC topology inverter [14] is derived from the conventional NPC topology as presented in Fig. 4. Two active switches with antiparallel diodes are used for clamping. In contrast to the conventional NPC converter, it has more than one way to clamp the midpoint. The upper clamping path results from turning on S2 and S5 and the lower clamping path from turning on S3 and S6. The current can be conducted through both clamping ways in both directions.

The distribution of the conduction losses during the zero states can be controlled by the selection of the different NPC paths. The switching losses could be controlled by the selection of different commutation states. There are many different PWM strategies for ANPC control by using different zero states and conduction paths [19]. In this section, two PWM strategies are introduced, and a new PWM strategy named ALD is proposed in the next section.

A. Classical Active PWM Strategy

In [20], two PWM strategies, named PWM-1 and PWM-2, for ANPC are discussed. In the case of the PWM-1 strategy, the inner switches have only conduction losses and the switching losses mainly stress the outer IGBTs. In the case of PWM-2 strategy, the switching losses only stress the inner switches.

TABLE III
SWITCHES STATES OF DF-ANPC HALF-BRIDGE INVERTER

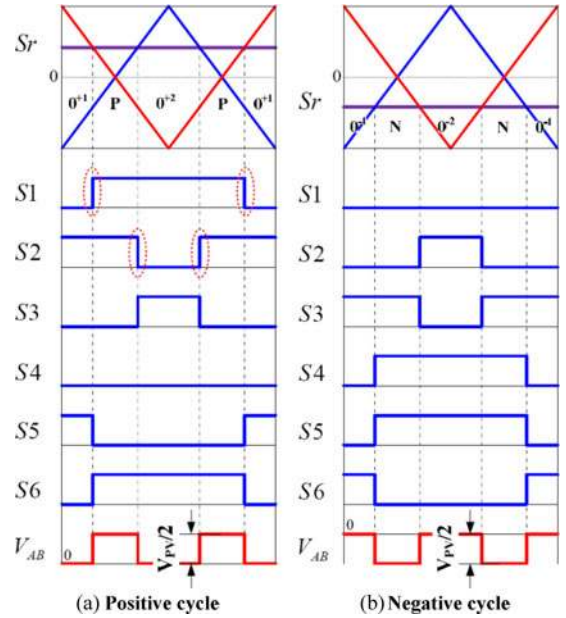| Voltage	S1	S2	S3	S4	S5	S6
Positive	1	1	0	0	0	1
0^{+1}	0	1	0	0	1	0
0^{+2}	1	0	1	0	0	1
0^{-2}	0	1	0	1	1	0
0^{-1}	0	0	1	0	0	1
Negative	0	0	1	1	1	0

Fig. 5.   Sinusoidal PWM for ANPC-DF strategy: (a) $Sr > 0$ and (b) $Sr < 0$.

The power losses distribution situation is not improved in the PWM-1 strategy and gets even worse in the PWM-2 strategy compared with the conventional NPC topology.

B. Double-Frequency (DF)-ANPC Strategy

Papers [20] show a PWM strategy named double-frequency (DF) ANPC control which naturally doubles the apparent switching frequency. In comparison with the other ANPC PWM strategies, the DF-ANPC strategy has four zero states: 0^{+1}, 0^{+2}, 0^{-1}, and 0^{-2} (see Table III). The modulation wave Sr is compared with two different carrier waves phase shifted by $T_S/2$ to generate the pulse as shown in Fig. 5. As there are two active states during one switching period, the output voltage has an apparent switching frequency equal to $2f_S$.

The work mode during positive half cycle is analyzed as below: As shown in Fig. 5(a), there are two active state periods with $V_{AO} = V_{PV}/2$ during one switching cycle. In the case of the first period, when S1 turns on, S2 keeps on state from zero state to active state, the switching on losses totally stresses on S1. When S2 turns off, S1 keeps on state from active state to zero state, all the switching off losses stresses on S2. In the case of second period, the situation is opposite, S2 takes the turn-on losses and S1 takes the turn-off losses.
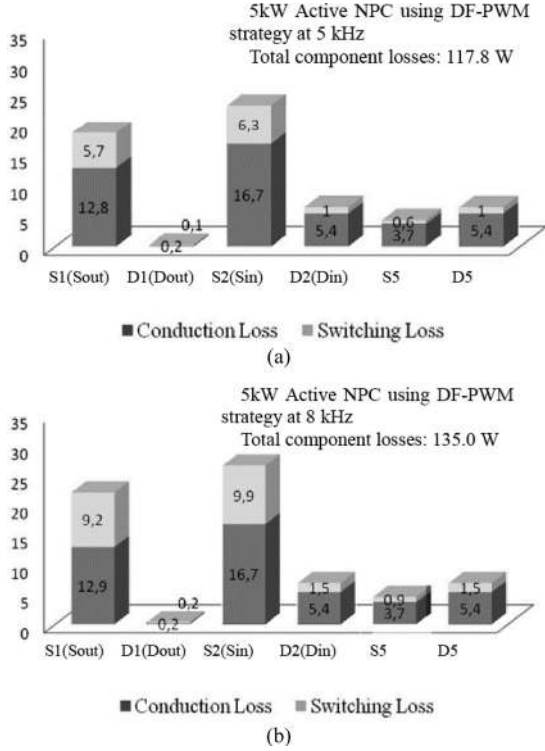
Fig. 6. Switching losses of a 5-kW DF-ANPC topology inverter at different frequencies, $M = 0.9$ and $\text{PF} = 1$. (a) Switching frequency at 5 kHz. (b) Switching frequency at 8 kHz.

TABLE IV
SWITCHES STATES OF ALD-ANPC HALF-BRIDGE INVERTER

Voltage	S1	S2	S3	S4	S5	S6
Positive	1	1	0	0	0	1
$0^{+\,In}$	1	0	1	0	0	1
$0^{+\,Out}$	0	1	1	0	0	1
0^{+}	0	0	1	0	0	1
0^{-}	0	1	0	0	1	0
0^{-Out}	0	1	1	0	1	0
0^{-In}	0	1	0	1	1	0
Negative	0	0	1	1	1	0

By using this PWM method, the switching losses are distributed more uniformly among inner and outer IGBTs as presented in Fig. 6. Compared with the conventional NPC topology, although the efficiency was not improved, the power losses distribution problem is improved.

IV. ALD ANPC STRATEGY

A. ALD Strategy

In the case of previously described classical strategies, the switching losses are concentrated on the outer or inner switches, which lead the power losses distribution unbalanced. The DF strategy could distribute the switching losses between inner switches and outer switches equally, however which still cannot optimize the total losses distribution. In this part, a new PWM
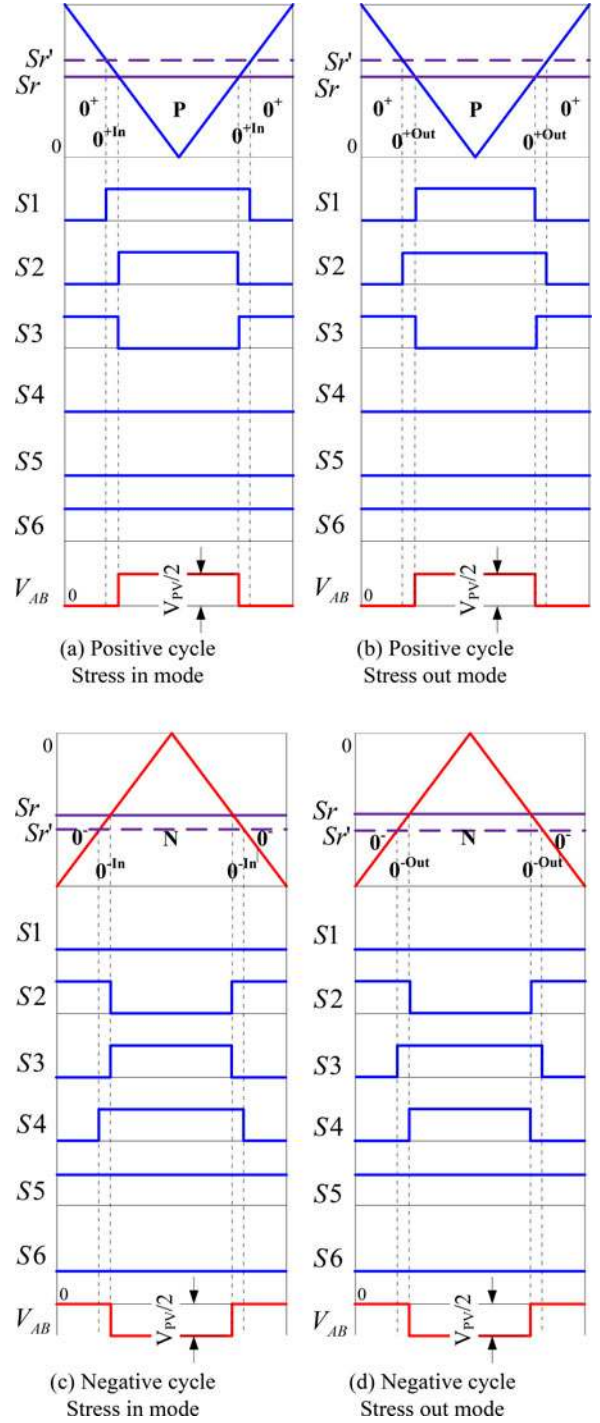

Fig. 7. Switches states and output voltage of ALD strategy, (a) $Sr > 0$ stress-in mode, (b) $Sr > 0$ stress-out mode, (c) $Sr < 0$ stress-in mode, (d) $Sr < 0$ stress-out mode.

strategy (named ALD strategy) is proposed, which combines the classical and DF PWM strategies' advantages.

This strategy uses six different zero states and a total of eight switches states as shown in Table IV and Fig. 7.

By distributing switching losses between inner and outer switches, ALD PWM could optimize the IGBT total losses distribution, and simplify the heat sink design.
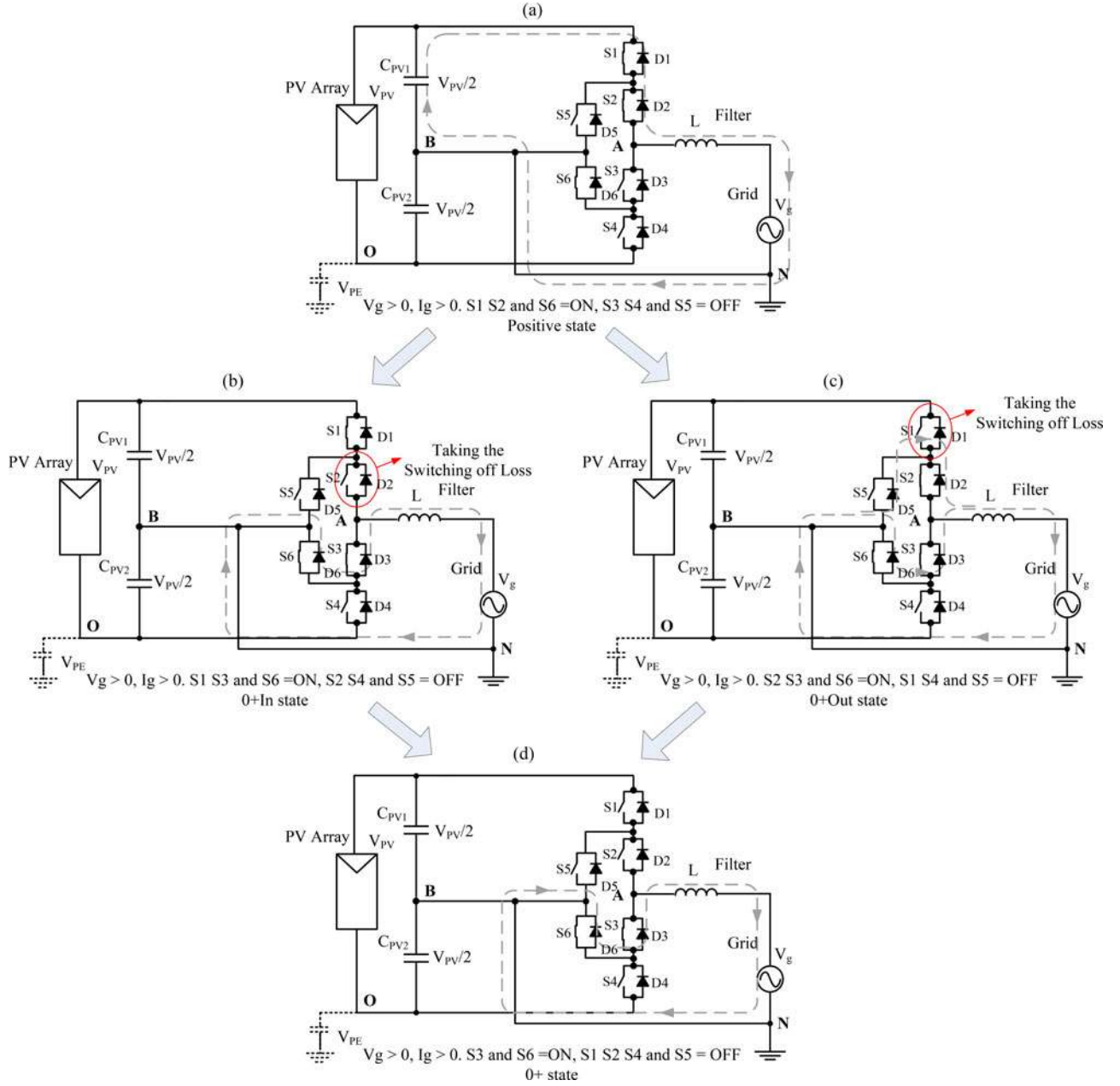
Fig. 8. Stress-in mode and stress-out mode selection during positive half cycle (turn off). (a) Positive. (b) Stress-in mode $0^{+\text{in}}$. (c) Stress-out mode $0^{+\text{out}}$. (d) 0^+.

When the switching sequence follows as 0^+, $0^{+\text{In}}$, Positive, $0^{+\text{In}}$, 0^+ or 0^-, $0^{-\text{In}}$, Negative, $0^{-\text{In}}$, 0^- as shown in the Fig. 7(a) and (c), as the inner switches turn off before outer switches while turn on later than outer switches, all the switching losses stress the inner IGBTs, in this case named this mode stress-in mode.

When the switching sequence follows as 0^+, $0^{+\text{Out}}$, Positive, $0^{+\text{Out}}$, 0^+ or 0^-, $0^{-\text{Out}}$, Negative, $0^{-\text{Out}}$, 0^- as shown in the Fig. 7(b) and (d), as the outer switches turn off before inner switches while turn on later than inner switches, all the switching losses stress on the outer IGBTs, in this case named this mode stress-out mode.

Accounting for different distributions (different modulation index and power factor), the inner and outer semiconductors

losses could be totally balanced by selecting a suitable stress-in mode/stress-out mode ratio.

B. Modulation Method of ALD

In this strategy, a new modulation signal Sr' is composed by a synchronized sinusoidal wave signal Sr_{add} added to the original modulation wave Sr. Actually the stress-in mode/stress-out mode selected is depended on which semiconductors (inner or outer) use the new modulation wave Sr'.

By using different modulation wave, different switching orders could be achieved to distribute the switching losses flexibly. In theory, using the new modulation wave Sr' will not change

the modulation index. In the case of positive active state, S1 and S2 must be ON at the same time, the same situation with the S3 and S4 in the case of negative active state.

For example, using stress-in mode during the positive half cycle, S1 uses Sr' as modulation signal and turns on before S2. However, this does not influence the output current, since the state of S1 neither influences the active state nor changes the modulation index. That because S2 also used the old modulation wave Sr, the duration of the both switches ON states is not changed. Therefore, the modulation index will not be changed (see Fig. 10).

The amplitude of Sr_{add} (A_{Sr_add}) is depended on the modulation index

$$A_{Sr\_\mathrm{add}} \leq (1 - M) \cdot A_{Sr}.$$

In the experiments, the pulse generation not only used DSP PWM1-6, but also used PWM 7-12, two different clocks need some margin to make sure the PWM generation. Therefore, the amplitude of this adding wave is chosen as 10% of the modulation wave, which could make sure the edge comparison accuracy and restrict the over modulation part.

S5 and S6 switches with grid frequency, half cycle on, and half cycle off (see Figs. 7 and 9).

When stress-in mode is selected, during the positive half cycle, S1 uses signal Sr' instead modulation signal Sr, whereas during the negative half cycle, S4 uses Sr' instead Sr. When stress-out mode is used, during the positive half cycle, S2 uses Sr', whereas during the negative half cycle, S3 uses Sr' instead Sr, which is illustrated by Fig. 7.

Fig. 8 shows the stress-out mode/stress-in mode selection and commutation process from positive state to zero state during positive half cycle. When stress-in mode is selected, the commutation process follows as (a), (b), (d). From (a) to (b), S2 turns off before S1, the main switching losses stress on S2. From (b) to (d), S1 switches off with soft switch condition. Meanwhile, when stress-out mode is selected, the commutation process follows as (a), (c), (d). From (a) to (c), S1 turns off before S2, the main switching losses stress on S1. From (c) to (d), S2 switches off with soft switch condition. The commutation process from zero state to positive state during positive half cycle is opposite. When stress-in mode is selected, the commutation process follows as (d), (b), (a). The main switching losses stress on S2. Meanwhile, when stress-out mode is selected, the commutation process follows as (d), (c), (a), the main switching losses stress on S1.The negative half cycle commutation process is contrary.

Moreover, Fig. 9 shows two grid cycles, the first one with 50–50% stress-in/stress-out mode and the second one with 30–70% stress-in/stress-out mode. 50–50% is the time ratio of stress-in and stress-out mode. As shown in Fig. 9, the first grid cycle with 50–50% stress-in/stress-out mode in order to distribute the switching losses between S1 and S4 equally, S1 takes first 25% positive stress-out mode switching losses and S4 takes the another 25% negative stress-out mode. The stress-in mode is also shared by positive and negative cycle equally in order to S2 and S3 take the same switching losses.
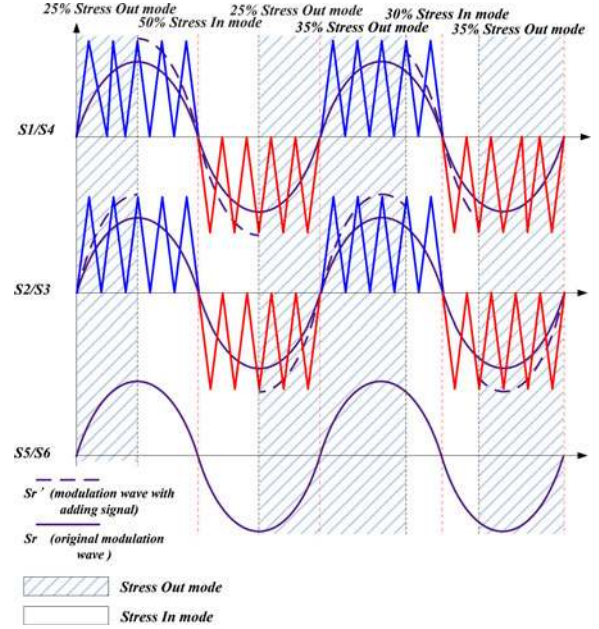

Fig. 9. PWM generation for one cycle of 50–50% stress-in/stress-out mode and one cycle of 30–70% stress-in/stress-out mode.

As in (1), [29], the conduction losses depended on the switches' threshold voltage V_{offset}, on-state resistor R, pass through current I, and integration time T are shown

$$E_{\mathrm{con}} = \int_0^T \left(V_{\mathrm{offset}} + IR\right) \cdot I \cdot dt. \tag{1}$$

For different modulation index (M) and power factor (PF) used, the integration time ratio between in and out switches is different, so the conduction losses distribution is different.

If the conduction losses are mainly stressed inner IGBTs (the conduction losses distribution are depending on the modulation index M and PF), then the ALD control could give more switching losses to outer IGBTs by increasing the rate of stress-out mode. Thereby, the total losses of inner and outer IGBTs are balanced. Otherwise, it could give more switching losses to outer IGBTs by increasing the rate of stress-in mode.

The switching loss also could be expressed approximately as (2), v_j and i_j are the instantaneous values of voltage and current at jth switching [30]

$$E_{\mathrm{sw}} = \sum_{j=1}^{n} \frac{1}{6} v_j \times i_j \times \left(T_{\mathrm{on}} + T_{\mathrm{off}}\right). \tag{2}$$

By using (1) and (2), the conduction losses and switching losses could be estimated then distributed equally. It could also get the stress-in/stress-out mode ratio by simulating or temperature closed-loop control in order to find the suitable work mode ratio.
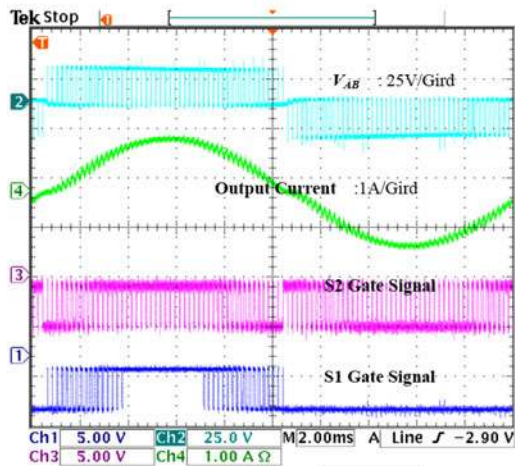
V. SIMULATION AND EXPERIMENTAL RESULTS
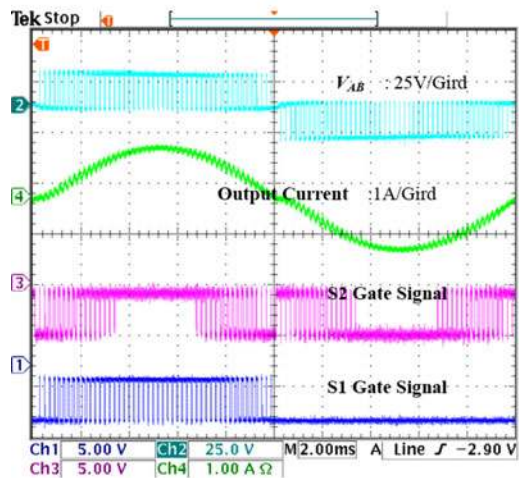
A. ALD Modulation Experimental Waves

1) Fig. 10 validates that using different modulation waves, Sr' does not change the modulation rate (M) and influence the
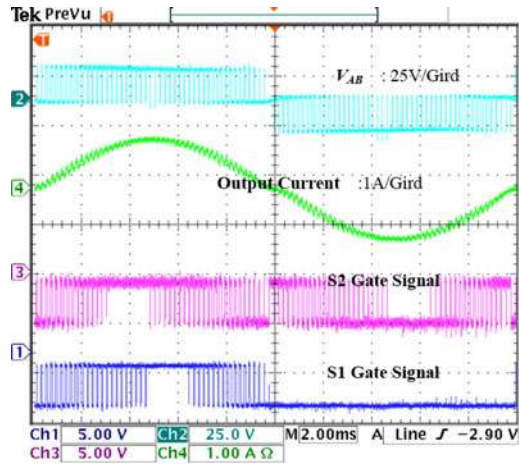
(a)

(b)

(c)

Fig. 10. Experimental waveform. (a) Waveforms 50–50% stress-out/stress-in mode. (b) Waveforms 70–30% stress-out/stress-in mode. (c) Waveforms 30–70% stress-out/stress-in mode.

output current as the S1 and S2 both ON periods were not changed. In case of Fig. 10(a), 50–50% stress-out/stress-in is used where it could see that Ch1 (S1) and Ch3 (S2) take the same switching losses during the positive half cycle. In Fig. 10(b), 70–30% stress-out/stress-in is
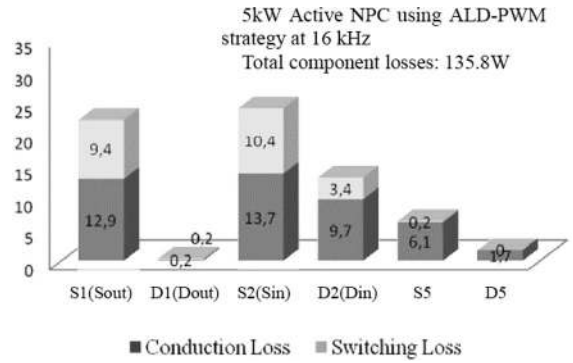

Fig. 11. Switching losses of ALD-ANPC 50–50% stress-out/stress-in mode at $PF = 1$, $M = 0.9$.
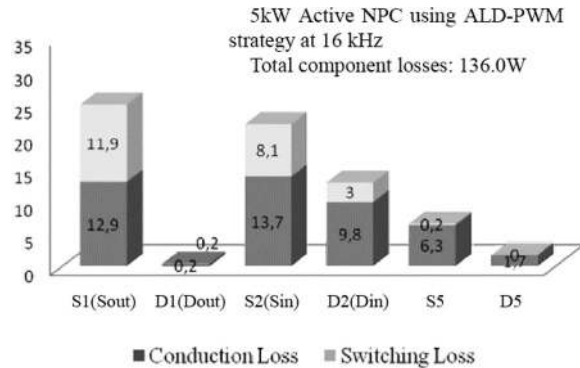

Fig. 12. Switching losses of ALD-ANPC 60–40% stress-out/stress-in mode.

used, whereas in Fig. 10(c), 30–70% stress-out/stress-in is used.

2) When ANPC topology inverter works, it must make sure that S1 and S5; S4 and S6; S1, S2, S3, and S4 are not ON at the same time. In theory, it is necessary to add dead time between them. However, during the positive half cycle, S5 and S4 keep OFF, meanwhile during the negative half cycle, S6 and S1 keep OFF, therefore there is no need to add dead time in this PWM strategy.

3) As shown in Fig. 7, during the positive half cycle $0^{+\,\mathrm{out}}$ stress-out mode, there are two routes the current could pass in the case of PF = 1: D5, S2; S6, S3. In the case of PF≠1, during the periods current is negative, there is just one route the current could pass through: S6, S3.

4) Fig. 10 also shows that the output voltage V_{AB} has three voltage levels as ordinary FB inverters.

Otherwise, if the conduction losses are mainly stressed outer IGBTs, then the ALD strategy could give more switching losses to outer IGBTs by increasing the rate of stress-in mode.

B. Simulation Results of ALD

Some simulation results are shown in Figs. 11–13. For 50–50% stress-in/stress-out mode (see Fig. 11), the total losses of S1/D1 and S2/D2 are 22.3 and 37.2 W, respectively, the losses distribution between outer and inner switches is not ideal. For 40–60% stress-in/stress-out mode (see Fig. 12), the losses
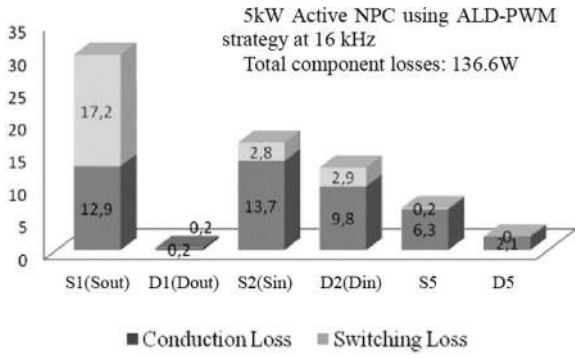
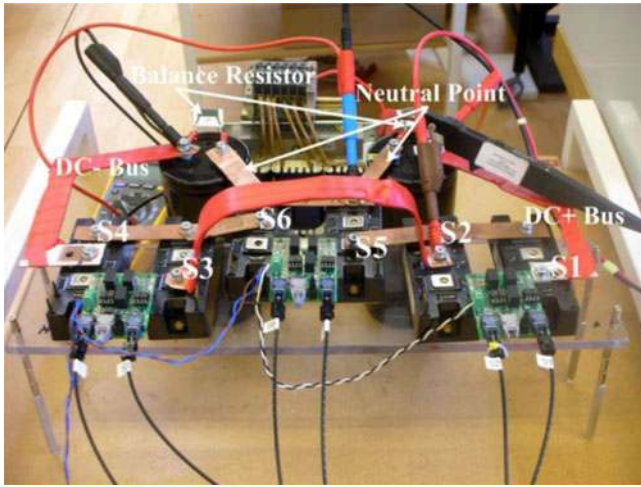Fig. 13.   Switching losses of ALD-ANPC 70–30% stress-out/stress-in mode.

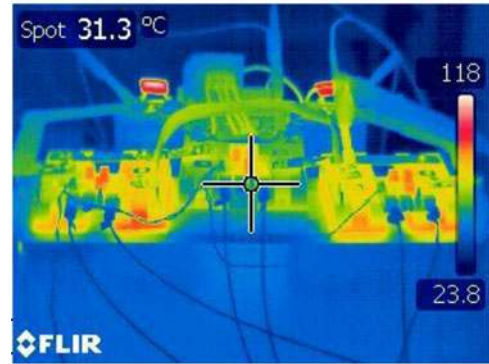Fig. 14.   Experimental equipments.

(a)

(b)

Fig. 15.   Thermal experimental results, (a) 50–50% stress-out/stress-in mode experiment (outer IGBTs around 70 °C, inner IGBTs over 110 °C), (b) 80–20% stress-out/stress-in mode experiment (outer IGBTs around 90 °C, inner IGBTs around 100 °C).
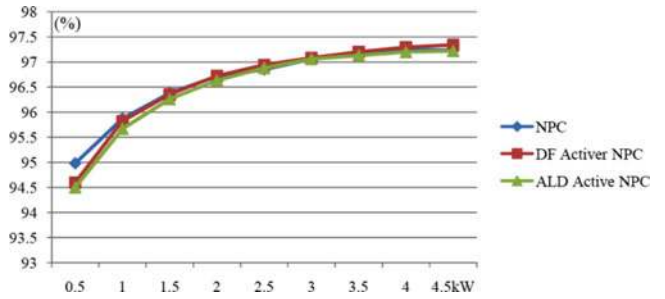

Fig. 16.   5-kW efficiency comparison experimental results.

distribution is improved to: 24.8 and 34.6 W, respectively. For 30–70% stress-in/stress-out mode (see Fig. 13), the losses distribution is balanced to 30.1 and 29.2 W, respectively. By using this strategy, the power losses distribution problem could be alleviated.

The main features of this ANPC converter with ALD strategy are as follows:

1) it is possible to control the switching losses distribution by controlling the stress-out/stress-in mode ratio, which means distribute the switching losses to outer or inner IGBTs;
2) from Figs. 3, 6, and 11–13, they show that the efficiency of these topologies are same, the different point is the losses distribution;
3) there are six zero states in the current switching process;
4) the adding sine wave has same phase angle and frequency as the modulation wave;
5) it is easy to control the switching distribution, since just one parameter needs to be modified.
6) no need for high-frequency dead time. Just need dead time add to zero crossing period.

C. Thermal Experimental Results

The experimental tests setup is constructed by MITSUBISHI PM75DSA120 IPM and the system parameters are shown in Table V. The YOGOGAWA WT3000 precision power analyzer is used for calculating the efficiency of the different inverters. The PV panels are replaced by one-stage dc power supply (MAGNA power). Power resistor is used as load, in order to increase the temperature faster. The thermal experiment setup uses six individual IPMs without heat sink as shown in Fig. 14, where S1, S3, and S5 using P module; S2, S4, and S6 using N module.

Fig. 15(a) shows the thermal photo of 50–50% stress-in/stress-out work mode, it is clear that the inner switches take

TABLE V
LOSSES DISTRIBUTION EXPERIMENTAL SYSTEM PARAMETERS

Quantity	Value
Line frequency	50 Hz
Carrier frequency	18 kHz
Output filter L	6 mH
C_{DC}	3000 μF
Rated dc voltage	450 V
R_{Load}	15 Ω
Power rate	1350 W
Switches	PM75DSA120
Power fact	1.0
Modulation rate	0.9

more stress than outer switches. It is easy to find that the losses distribution in (b) is much balanced than the losses distribution in (a).

From the experiments, the efficiency curves for the tested topologies are given in Fig. 16. The efficiencies of the ANPC and conventional NPC are almost equal. In fact, the efficiency of inverter by using different ANPC PWM strategies should be same. Due to the experimental environment difference, the efficiency is slightly different.

VI. CONCLUSION

The NPC topology has been proven to be very suitable for transformerless PV systems due to their high efficiency, low leakage current, and low EMI. The main disadvantage of the NPC inverter is given by an unequal distribution of the losses in the semiconductor devices, which leads to an unequal distribution of temperature and limits the output power of the inverter. The ANPC structure has been developed in order to overcome this drawback.

For the ANPC topology, due to the presence of switches instead of clamping diodes, it is possible to use different modulation strategies aiming at obtaining a better power losses distribution. Thus, the ANPC topology is suitable for the high-power transformerless PV system applications. The modulation strategy is a key issue in this topology. In this paper, a new ANPC modulation strategy named ALD is proposed.

This PWM method combines the losses distribution advantages of classical and DF-ANPC strategies. Depending on the different modulation index and PF (which means different conduction losses distribution between inner and outer switches), it is able to choose the most suitable stress-in/stress-out mode rate to balance the total losses distribution between inner and outer switches, where the switching losses distribution is controlled by the stress-in/stress-out mode rate.

The simulation and experimental results show that the losses distribution could be balanced without adding any new components in all the modulation index and PF conditions. Thermal experiments worked at $\text{PF} = 1$ (for PV systems) illustrate that the losses distribution could be balanced by using this PWM method.

Moreover, in some work mode fixed applications (modulation index and PF fixed), the stress-out/stress-in ratio could be fixed by losses calculation or simulation off-line. For the work mode changeable applications, the stress-out/stress-in ratio could be chosen in a closed thermal loop fashion using online temperature monitor, which could lead this strategy to suit for any work conditions.

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