A New Regenerative Divider by Four up to 160 GHz in SiGe Bipolar Technology

Saverio Trotta[1, 2], Herbert Knapp[1], Thomas F. Meister[1], Klaus Aufinger[1], Josef Böck[1], Bernhard Dehlink[1,2], Werner Simbürger[1], Arpad L. Scholtz[2]

[1] Infineon Technologies AG, Am Campeon 1-12, D-81726 Munich, Germany
[2] Vienna University of Technology, Karlsplatz 13, A-1040 Vienna, Austria
E-mail: Saverio.Trotta@infineon.com

***Abstract* — A new topology for a very high speed regenerative divider by four is proposed. The circuit uses a double mixer to directly divide the input frequency by four . A validation chip has been developed in a 225 GHz f_T SiGe bipolar technology. The circuit operates in a frequency range from 80 GHz to 160 GHz while consuming a 650 mW from a -5.5 V supply.**

***Index Terms* — SiGe, frequency dividers, Gilbert cell, Miller divider, regenerative divider.**

I. Introduction

High-speed frequency dividers play a critical role in measurement instruments and communication systems. For InP-based HBT technologies, a dynamic divider operating up to 150 GHz [1] has been presented. Recently, regenerative dividers in SiGe bipolar technology (HBTs) with a maximum operating input frequency of 110 GHz [2] and 100 GHz [3] have been reported. In CMOS technology an operating frequency of 40 GHz has been achieved [4].

In this paper we present a 160 GHz regenerative divider with a divide ratio of four. The divider is based on a new topology which allows to achieve very high speed, a divide ratio of four and low power consumption. To the best of our knowledge, the operating frequency of this new divider is the highest reported to date for any silicon-based technology.

II. Circuit Design

Originally proposed by Miller in 1939 [5], the dynamic divider is based on mixing the output signal of the mixer with the input signal and applying the result to a low-pass filter (LPF), as shown in Fig. 1. Under proper phase and gain conditions, the component at $\omega_{in}/2$ survives and circulates around the loop. Since the device capacitances are absorbed in the low-pass filter, this topology achieves a high speed.

The topology we present in this paper is based on a double mixer. The filtered output from this double mixer is mixed with the input signal. The signal which comes out from this first mixing is mixed again with the input signal (Fig. 2). In this way the divide ratio of the regenerative divider is four.

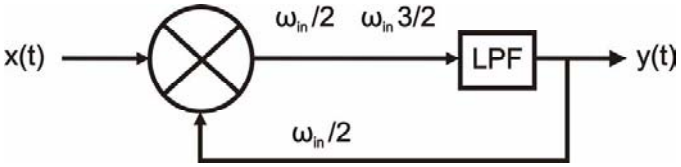

Fig. 1 Dynamic Miller divider.

The double mixer consists of two stacked Gilbert cells (Fig. 3). Supposing to have an input signal at 160 GHz, the output signal from the double mixer, under proper phase and gain conditions, will be 40 GHz. This signal is filtered and then applied to the first differential pair of the stacked mixer. The signal after the first mixing with the input signal at 160 GHz shows a frequency of 120 GHz, which is $3f_{in}/4$. Now this signal is mixed again with the input signal at 160 GHz: the output will be 40 GHz, which is $f_{in}/4$. Simulation results in Fig. 4 and 5 confirm the simply idea we have explained above.

A validation test chip of this technique has been designed in a SiGe bipolar technology. The circuit (Fig. 2) is fully differential and consists on an input stage, the double mixer, the filter and the output buffer. The input stage consists of a first pair of emitter followers (EFs), which drives the upper level of the mixer, and another two pairs of emitter followers.

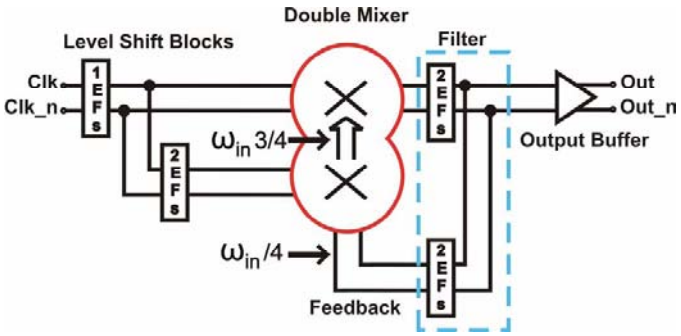

Fig. 2 New dynamic divider by four block schematic.

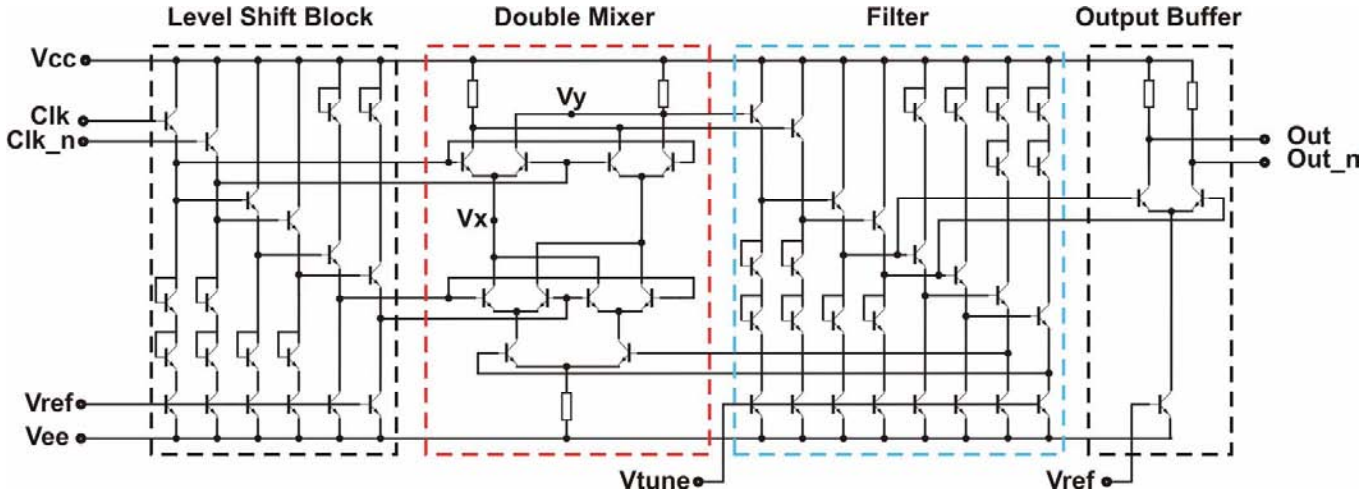

Fig. 3 Dynamic divider by four schematic.

These emitter followers shift down the level of the signal to drive properly the second input of the double mixer. Since there is not enough headroom for a current source, a resistor has been used instead of a current source for the mixer. The output of the stacked mixer is connected to the filter. This consists of four cascaded pairs of emitter followers. The filter can be tuned by adjusting Vtune (Fig. 3): in this way it is possible to set the current density for the transistors in the EFs pair. The signal from the last pair is applied to the lower differential pair of the mixer. The output from the second pair drives also the output buffer, which is a simple differential pair. In the layout (Fig. 6b) we took care to design the interconnection lines between every emitter follower as short as possible to avoid instability effects like ringing [6,7]. Moreover, in order to reduce some critical parasitic inductances in the local-ground connections (Fig. 6b), the collectors of the transistors in the EFs pairs (the same for the diodes) have been connected as close as possible with a wide ground plane [7]. The feedback lines from the filter to the lower differential pair in the double mixer and the lines which apply the input signals to the stacked mixer show exactly the same length.

III. Technology

The frequency divider is manufactured in an advanced 225 GHz f_T SiGe:C bipolar process based on the technology presented in [8]. It uses shallow and deep trench isolation. The transistors have a double-polysilicon self-aligned emitter base configuration with a SiGe:C base which is integrated by selective epitaxial growth. The transistors are fabricated using 0.3 µm lithography. The minimum effective emitter width is 0.14 µm. Except for the input stage, the transistors in the chip operate at a current density of 6.5 mA/µm^2. The chip photograph is presented in Fig. 6a. The size of the double-mixer and the filter is 75 µm x 110 µm (Fig. 6b).

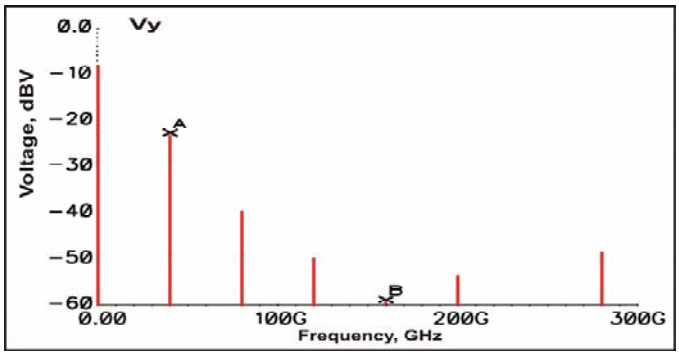

Fig. 4 Simulated spectrum response of the signal at the point Vy, f_{in} = 160 GHz (A = 120 GHz; B = 160 GHz).

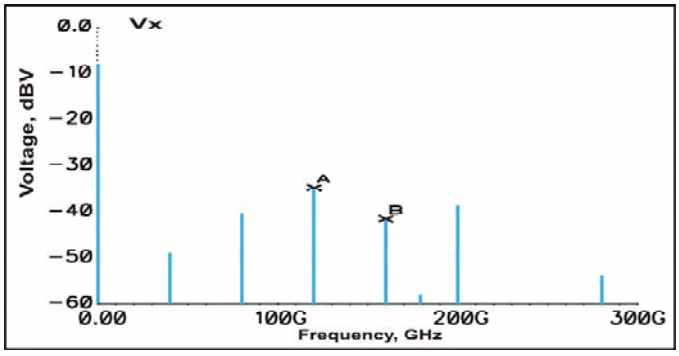

Fig. 5 Simulated spectrum response of the signal at the point Vx, f_{in} = 160 GHz (A = 40 GHz; B = 160 GHz).

IV. Test Setup

Measurements were performed on wafer, at room temperature. Two different test setups have been used to measure the input sensitivity of the divider in the W-band and D-band. We have used a single-ended clock signal to drive the circuit at all frequencies. The test setups differ only at the input port of the divider.

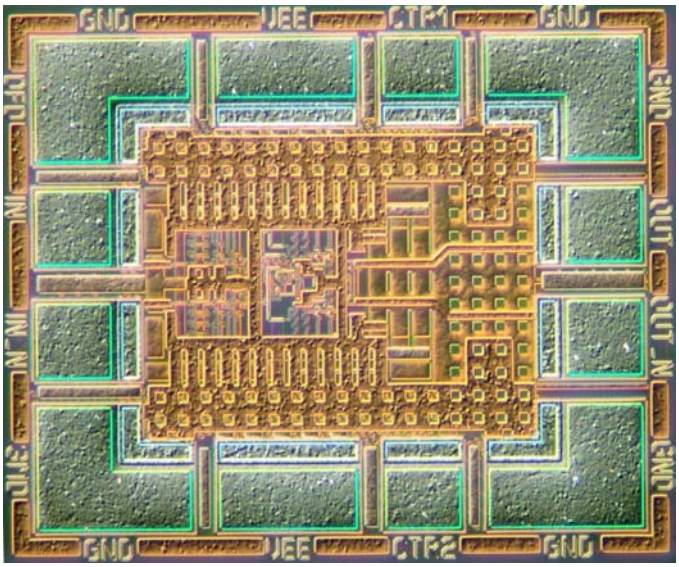

Fig. 6 a) Chip photograph of the dynamic frequency divider (size 550 µm x 450 µm).

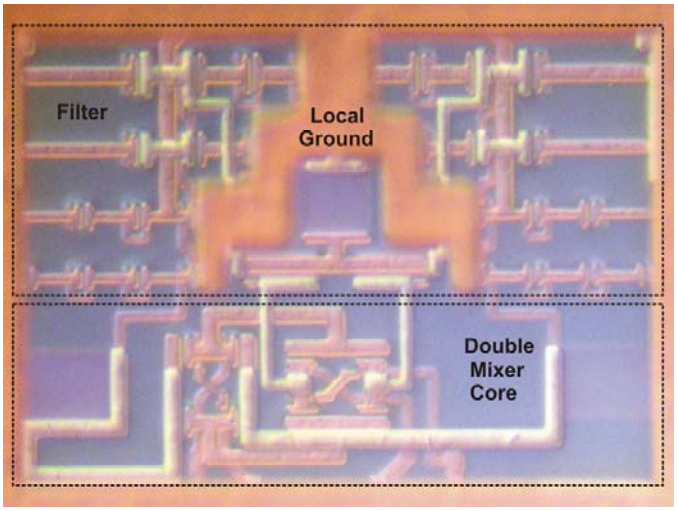

Fig. 6 b) Detail of the layout of the double mixer and the filter.

We have used a differential coaxial GSSG dc-to-67 GHz probe at the divider output in all setups. As shown in Fig. 7, one output signal was applied directly to the sampling head of the 70 GHz sampling oscilloscope; the other one has been used to drive first the spectrum analyzer and then a divider by 32 which generates the signal to trigger the oscilloscope. The complementary output from this divider by 32 was connected to a spectrum analyzer.

In the 75 to 110 GHz frequency range the input signals were generated by an Agilent millimeter-wave source module. The input probe was a 120 GHz probe connected to the source module with a W-band wave guide. After the measurement of

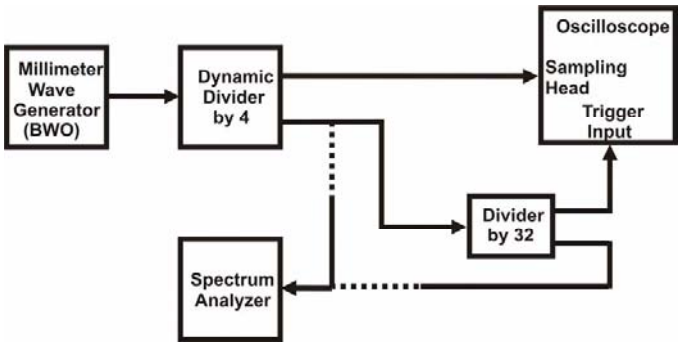

Fig. 7 Measurement setup in the 110-170 GHz frequency range.

the sensitivity in this frequency range, we have determined the effective level of the power delivered to the input probe for each measured frequency point by connecting a power meter at the end of the wave guide. The loss of the probes has not been taken into account.

For the range from 110 GHz to 170 GHz, a back wave oscillator (BWO), has been used to test the circuit. The BWO was connected with a D-band wave guide. The complete setup for the measurement in this range is shown in Fig. 7. The power levels have been extrapolated from the data sheet of the BWO. Since the BWO is not a locked source, its output signal shows a lot of jitter, which can influence the quality of the output signal from the divider under test.

V. Measurements Results

Operating with a supply voltage of -5.5 V the divider consumes 650 mW. According to simulation, the double mixer has a power consumption of 27.5 mW. Fig. 8 shows the oscilloscope screenshot of the 40 GHz output of the divider, with a 160 GHz single-ended input clock signal. The spectrum of this signal is shown in Fig. 9 and its 100 MHz span zoom in Fig. 10. The circuit has been tested also at different temperatures: at 70°C it is still operating at 160 GHz. For temperature around 0°C the maximum operating frequency observed is 170 GHz. The measured input sensitivity curve is shown in Fig. 11.

VI. Conclusion

A new design technique for regenerative divider by four has been proposed. The theory has been validated by measurement results of a dynamic divider designed in a 225 GHz f_T SiGe bipolar technology. The new topology allows very high operating frequencies, low power and a direct division by four of the input frequency. It represents the state of the art in regenerative divider design. The measurements have been performed on wafer. The total power

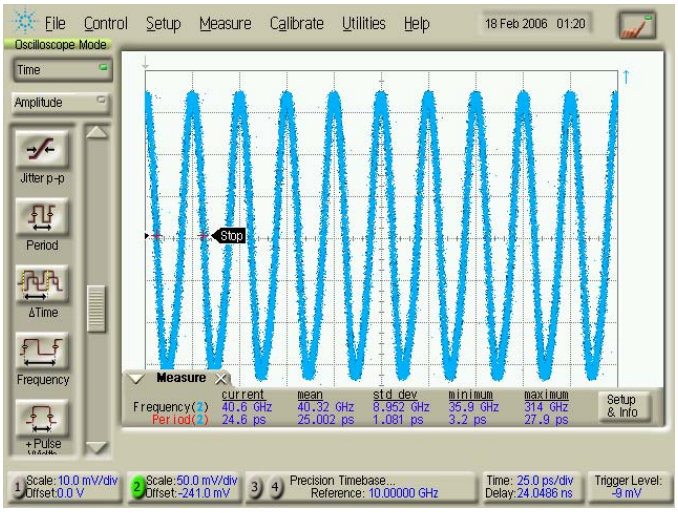

Fig. 8 Single-ended output signal (f_{in} = 160 GHz)
x-axis: 25ps/div, y-axis: 50 mV/div.

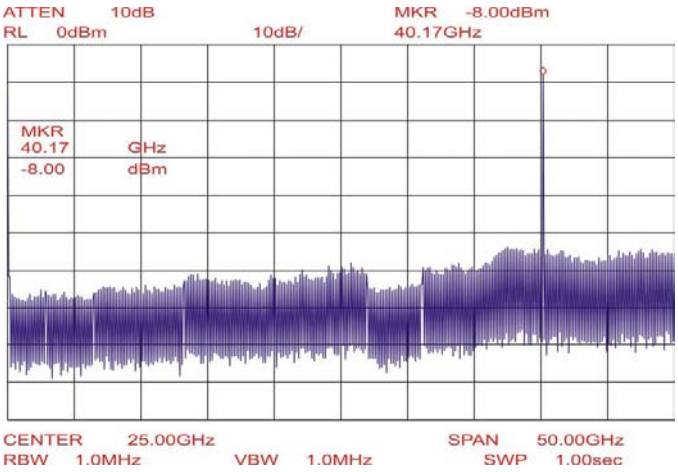

Fig. 9 Measured spectrum of the divider output signal, f_{in} = 160 GHz (50 GHz span).

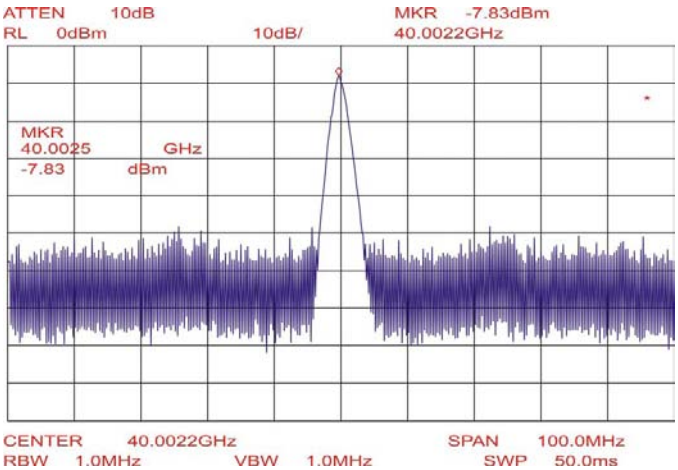

Fig. 10 Measured spectrum of the divider output signal, f_{in} = 160 GHz (100 MHz span).

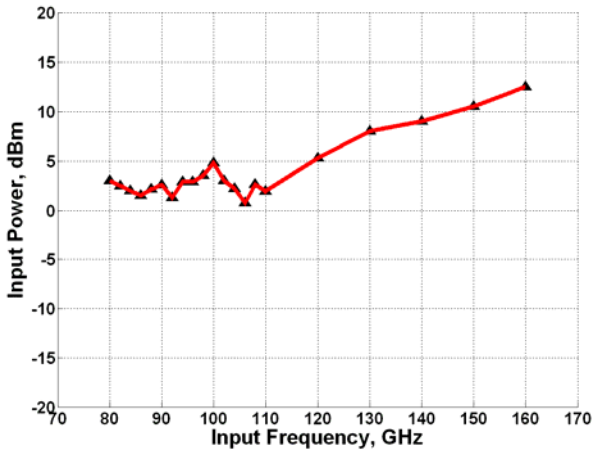

Fig. 11 Measured input sensitivity of the divider.

consumption of the chip is 650 mW. The divider operates between 80 GHz and 160 GHz. To the authors' knowledge, this is the highest frequency of operation for any silicon-based frequency divider reported to date.

REFERENCES

[1] S. Tsunashima, K. Murata, M. Ida, K. Kurishima, T. Kosugi, T. Enoki, and H. Sugahara, "A 150-GHz dynamic frequency divider using InP/lnGaAs DHBTs," *IEEE GaAs IC Symp. Dig.*, pp. 284-287, 2003.

[2] H. Knapp, M. Wurzer, T.F. Meister, J. Böck, S. Boguth, H. Schäfer, "86 GHz Static and 110 GHz Dynamic Dividers in SiGe Bipolar Technology, " *IEEE MTT-S Int. Microwave Simp. Dig.*, pp. 1067-1070, 2003.

[3] A. Rylyakov, L. Klapproth, B. Jagannathan and G. Freeman, "100 GHz Dynamic Frequency Divider in SiGe Bipolar Technology," *Electron. Lett.*, 39, No. 2, pp. 217-218, 2003.

[4] J. Lee and B. Razavi, "A 40-GHz Frequency Divider in 0.18 µm CMOS Technology," *IEEE Journal of Solid State Circuits*, vol. 39, no. 4, pp. 594-601, April 2004.

[5] R. L. Miller, "Fractional-frequency generators utilizing regenerative modulation," *Proc. Inst. Radio Eng.*, vol. 27, pp. 446–456, July 1939.

[6] H.-M. Rein, M. Möller, "Design Considerations for Very-High-Speed Si-Bipolar IC's Operating up to 50 Gb/s," *IEEE Journal of Solid State Circuits*, vol. 31, no. 8, pp. 1076-1090, August 1996.

[7] R. Schmid, T.F. Meister, M. Rest, H.-M Rein, "SiGe driver circuit with high output amplitude operating up to 23 Gb/s," *IEEE Journal of Solid State Circuits*, vol. 34, no. 6,pp. 886-891, January 1999.

[8] J. Böck, H. Schäfer, H. Knapp, K. Aufinger, M. Wurzer, S. Boguth, T. Böttner, R. Stengel, W. Perndl, T. F. Meister, "3.3 ps SiGe Bipolar Technology", *IEEE IEDM*, pp. 255-258, 2004.