IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received October 21, 2019, accepted November 27, 2019, date of current version December 16, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2957180

A New Single Phase Single Switched-Capacitor Based Nine-Level Boost Inverter Topology With Reduced Switch Count and Voltage Stress

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This work was supported in part by the QU High Impact under Grant QUHI-CENG-19/20-2 from Qatar University, and in part by the Qatar National Library, Doha, Qatar.

ABSTRACT Based on the concept of switched-capacitor based multilevel inverter topology, a new structure for a boost multilevel inverter topology has been recommended in this paper. The proposed topology uses 11 unidirectional switches with a single switched capacitor unit to synthesize nine-level output voltage waveform. Apart from the twice voltage gain, self-voltage balancing of capacitor voltage without any auxiliary method along with reduced voltage stress has been the main advantages of this topology. The merits of proposed topology have been analyzed through various comparison parameters including component counts, voltage stresses, cost and efficiency with a maximum value of 98.3%, together with the integration of switched capacitors into the topology following recent development. Phase disposition pulse width modulation (PD-PWM) technique and nearest level control PWM (NLC-PWM) have been used for the control of switches. Different simulation and hardware results with different operating conditions are included in the paper to demonstrate the performance of the proposed topology.

INDEX TERMS Multilevel inverter, boost inverter topology, switched-capacitor, single dc source, reduce switch count, PWM.

I. INTRODUCTION

With the rapid growth of the renewable energy resources and its application in high voltage applications link industrial drive, high voltage dc transmission (HVDC), electric vehicle (EV), etc., power electronic converters play an important role in the power conversion suitable for each application. Multilevel inverters have its own importance in medium and high voltage applications due to reduced voltage rating of power semiconductor devices for high voltage generation, reduced harmonic contents, the small size of the filter, reduced EMI, improved efficiency and many more. Neutral point clamped (NPC), flying capacitor (FC) and cascade H-bridge (CHB) are traditional topologies that have been extensively researched and applied in different applications. However, the major concerns with these topologies have been the higher number of components, capacitor voltage balancing and complex control for a higher number of levels [1]–[4]. Therefore, numerous topologies have been proposed with reduce switch count [5]–[14]. In [7], an optimal design of multilevel inverter topology has been discussed. The topology of [7] uses several isolated dc voltage sources which restricts its applications. Another topology based on isolated voltage sources has been proposed in [9], in which 17 level

The associate editor coordinating the review of this manuscript and approving it for publication was N. Prabaharan.

output voltage has been achieved using four voltage sources. Similar topologies have been proposed in [10], [12]. In these topologies, higher number of levels can be generated to improve the quality of the output voltage. However, most of these topologies lack the voltage boosting ability.

Voltage boosting is essential for the topologies to be used in the integration with renewable energy resources especially solar photovoltaic system due to its low voltage generation. Switched capacitor (SC) based multilevel inverter topologies with boosting feature gives a suitable approach for the low input voltage systems. In SCMLI, the switched capacitors are charged and discharged in parallel and series configurations with dc input supply voltage, respectively. Furthermore, SC-based topologies with self-voltage balancing of the capacitors without any auxiliary methods reduces the control complexity of the system [15]–[21].

An SC-based MLI has been proposed in [22], which generates five-level output voltage with unity voltage gain. An improved topology of [22] has been proposed in [23]. The topology of [23] produces seven level output voltage with a voltage gain of 1.5. However, it uses two floating capacitors with a voltage rating equal to a dc input voltage, which is underutilized due to a lower voltage gain with higher voltage ratings. Furthermore, two switches are needed to block twice the input voltage. Another seven-level SC-based topology has been suggested in [24], however, the unequal voltage step in [24] increases the harmonic content of the output voltage.

A topology with two dc-link capacitors and one floating capacitor has been proposed in [25]. It utilizes 10 switches for seven-level generations, however, the voltage gain has been limited to a value of 1.5. An improved topology of [26] has been proposed in [27] in which the voltage gain has been extended to double the value of [26] to 1.5. Similar to [26], a hybrid switched-capacitor based topology has been proposed in [28] without boosting the input voltage. Another topology with a voltage gain of 1.5 has been proposed in [29] which has a higher switch count for the seven-level output voltage.

In this paper, a new switches capacitor-based MLI topology has been proposed with the aim of increasing the voltage gain. The different merits of the proposed topologies are

- Uses a single dc voltage source with a single floating capacitor for nine-level voltage generation
- Twice voltage gain (V_o:$V_{in} = 2$)
- Maximum voltage stress of any switch is equal to input dc voltage source
- Two switches are operated at the fundamental frequency
- High voltage gain to switch ratio
- Self-capacitor voltage balancing independent of load parameters

This paper has been organized as follows: Section II gives the details of the proposed topology with capacitor value selection and modulation strategy. Section III gives a detailed comparison with other SC-based MLI topologies. Section IV elaborates the different simulation and experimental results captured in different loading conditions. Section V summarizes the paper.

II. PROPOSED NINE-LEVEL TOPOLOGY

A. DESCRIPTION OF THE PROPOSED TOPOLOGY

The circuit configuration of the proposed nine-level topology has been depicted in Fig. 1. As shown in Fig. 1, the single dc source boost topology uses nine unidirectional switches and one bidirectional switch along with two dc-link capacitors C_1 and C_2 and one switched capacitor C_3. The two dc-link capacitors C_1 and C_2 split the dc input voltage into equal half, resulting in their voltage as $V_{dc}/2$. The switched capacitor C_3 is charged up to the dc input voltage V_{dc} through switches S_3, S_4, S_7, and S_8. The switch S_6 is used to give the boosting feature of the proposed topology.

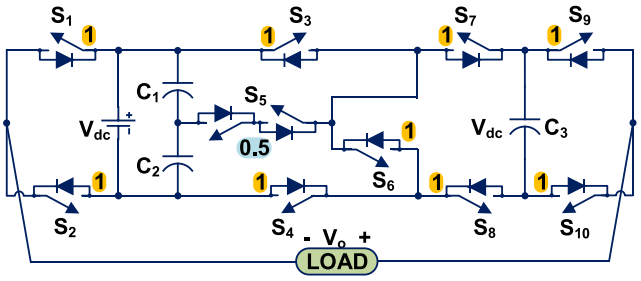

FIGURE 1. Proposed topology.

The switching table for the proposed nine-level topology is given in Table 1.

TABLE 1. Switching states of the proposed topology.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	V_o	V_{C3}
0	1	1	0	0	1	0	1	1	0	$2V_{dc}$	D
0	1	0	0	1	1	0	1	1	0	$1.5V_{dc}$	D
0	1	1	1	0	0	1	1	1	0	V_{dc}	C
0	1	0	0	1	0	1	0	1	0	$0.5V_{dc}$	—
0	1	1	1	0	0	1	1	0	1	0	C
1	0	0	0	1	0	0	1	0	1	$-0.5V_{dc}$	—
1	0	1	1	0	0	1	1	0	1	$-V_{dc}$	C
1	0	0	0	1	1	1	0	0	1	$-1.5V_{dc}$	D
1	0	0	1	0	1	1	0	0	1	$-2V_{dc}$	D

Notations: 0 = Off state of the switch, 1 = On state of the switch, — = no change in capacitor voltage, C = charging of capacitor, D = discharging of capacitor

Reverse blocking voltage of a switch is an important aspect in the design of the topology. Fig. 1 gives the maximum blocking voltage of each switch used in the topology. Out of 11 switches, all the unidirectional switches need to block a voltage equal to the input supply voltage, i.e., V_{dc}. The bidirectional switch requires two unidirectional switches with a voltage rating of $0.5V_{dc}$. Therefore the total standing voltage (TSV), which is the sum of the maximum blocking voltage of all switches, has a value of $10V_{dc}$. Fig. 2 illustrates the voltage stress of all the switches considering all voltage levels at the output.

The operation of the proposed topology is explained with the voltage states in the positive half cycle. The different

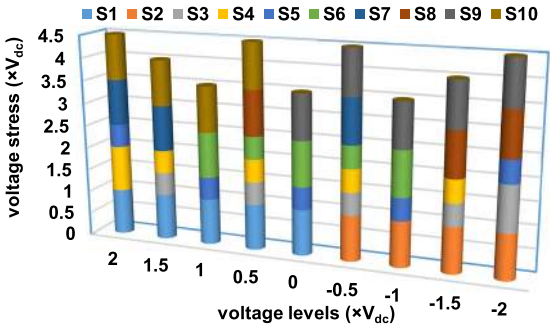

FIGURE 2. Voltage stress of all switches for all voltage levels.

voltage level generation of the proposed topology are shown in Fig. 3 (a)-(e).

- Zero Voltage State ($V_o = 0$): As shown in Fig. 3 (a), the zero voltage state across the load by turning ON switches S_2, S_4, S_8, and S_{10}. During zero voltage level, the switched capacitor C_3 is connected to the dc voltage source and gets charged to V_{dc}.
- First Voltage State ($V_o = 0.5V_{dc}$): As shown in Fig 3 (b), the capacitor link voltage is utilized in these voltage levels. The load is connected to the mid-point of the dc-link capacitor through switches S_2, S_5, S_7, and S_9. The capacitor voltage of C_3 remains unchanged.
- Second Voltage State ($V_o = V_{dc}$): In this voltage state, the entire input voltage applies to the load. Simultaneously, the capacitor is also connected in parallel to the dc voltage source to be charged. This voltage state is illustrated in Fig. 3 (c).
- Third Voltage State (($V_o = 1.5V_{dc}$): In this voltage state, as shown in Fig. 3 (d), the dc-link capacitor voltage gets added to the switched capacitor voltage to give the voltage level of $1.5V_{dc}$.
- Fourth Voltage State ($V_o = 2V_{dc}$): During this voltage state, the input dc source voltage is added to the voltage of the switched capacitor. This results in a voltage level equal to twice the input voltage. The fourth voltage state is illustrated in Fig. 3 (e).

B. MODULATION STRATEGY

For the proposed nine-level topology, phase-disposition pulse width modulation (PD-PWM) technique has been used. In this, four high-frequency carrier signals, each with a peak to peak amplitude of one, and a frequency of f_{cr} are compared with a sinusoidal reference signal having a peak value of V_{sine} to generate the pulses. Fig. 4 (a) shows the sinusoidal reference signal along with four carrier waveforms to achieve the nine-levels output voltage. To generate the gate pulses for different switches, these pulses are configured according to Table 1 and the logic for the PWM generation is depicted in Fig 4 (b). The modulation index (MI) for the nine-level PD-PWM is given as

$$MI = \frac{V_{\text{sine}}}{4V_c} \tag{1}$$

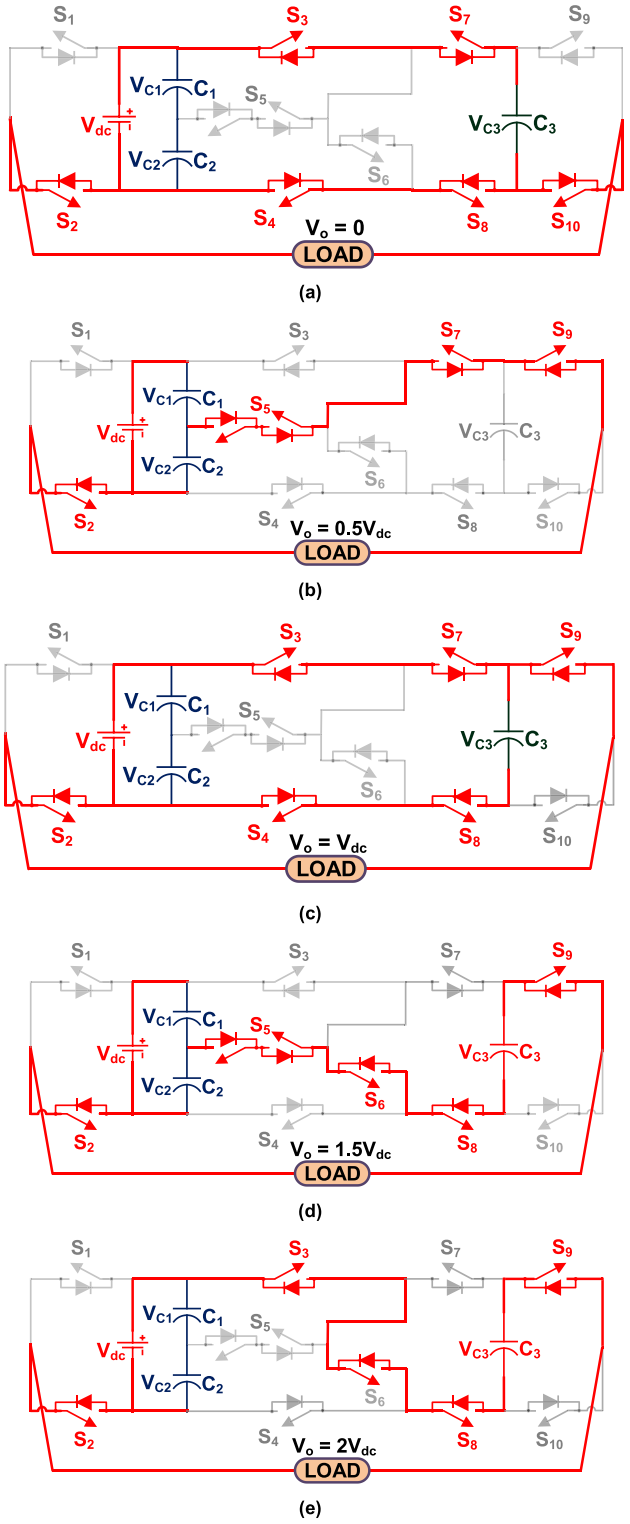

FIGURE 3. Connection diagram with the conduction state of the switches for the proposed nine-level topology for voltage levels of (a) $V_o = 0$, (a) $V_o = 0.5V_{dc}$, (a) $V_o = V_{dc}$, (a) $V_o = 1.5V_{dc}$, and (a) $V_o = 2V_{dc}$.

Furthermore, the proposed nine-level topology has also been tested with low switching frequency technique. Nearest level control PWM (NLC-PWM) has been used as a low

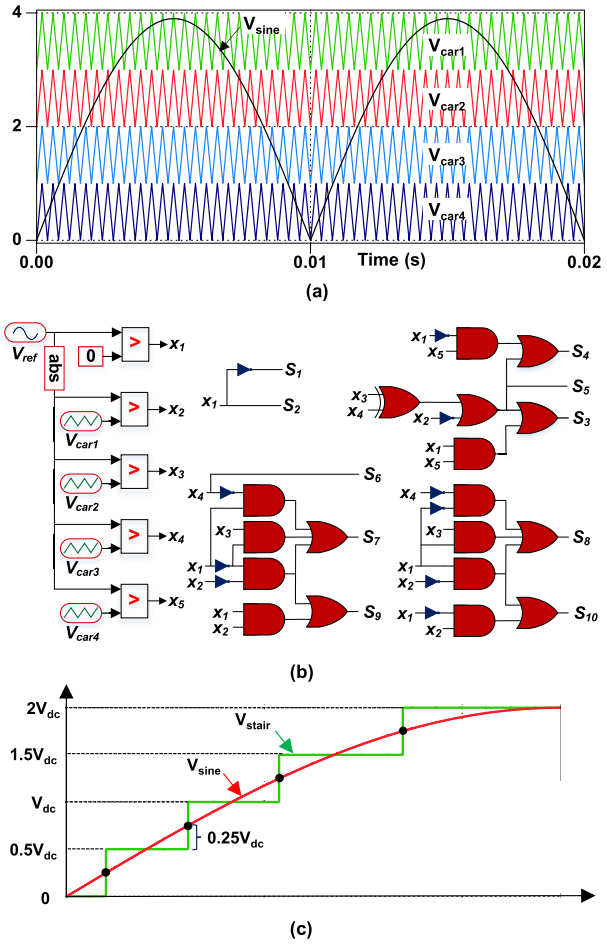

FIGURE 4. PWM control of the proposed topology with (a) PD-PWM, (b) switching logic for the gate pulse generation for the proposed topology and (c) NLCPWM.

frequency technique for the gate pulse generation. In NLC-PWM, the sinusoidal reference signal V_{sine} is compared with the staircase output voltage waveform V_{stair} as shown in Fig. 4 (c). The comparison generates the pulses and these pulses are used for the gate pulse generation based on the switching logic of the proposed topology given in Table 1.

C. SELECTION OF CAPACITOR VALUE

During the positive half cycle, as depicted in Fig. 3 (a) and (c), the capacitor C_3 is directly connected to the dc voltage source during voltage zero and V_{dc}. Similarly, during the negative half cycle with voltage levels of zero and $-V_{dc}$, capacitor C_3 gets charged by having a parallel connection with the input dc supply. For the charging loop, the time constant RC has a value which is lower than the charging duration. This results in the full charging of the capacitor C_3. During the voltage levels of $\pm 1.5V_{dc}$, and $\pm 2V_{dc}$, the energy stored in the capacitor is transferred to the load. The decrease in the stored energy level causes a drop in the capacitor voltage i.e., ripple voltage. The ripple voltage can be regulated by the proposed selection of capacitance value of the capacitor

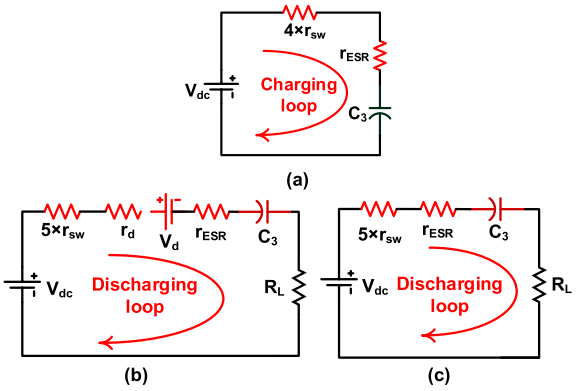

FIGURE 5. Equivalent circuit of the proposed topology for (a) charging loop (b) discharging loop for voltage level of $\pm 1.5V_{dc}$, and (b) discharging loop for voltage level of $\pm 2V_{dc}$.

which is given by

$$C_3 = \frac{I_{pk}}{(\Delta V_C \times f_o)} \tag{2}$$

where I_{pk} is the peak value of the load current, ΔV_c is the ripple voltage and f_o is the frequency of the output voltage.

D. SELF-VOLTAGE BALANCING OF THE CAPACITOR

Self-voltage balancing of the capacitor voltage C_3 has been one of the important features of the proposed topology. The capacitor C_3 is charged up to V_{dc} during the voltage states of zero and $\pm V_{dc}$. During charging, the equivalent circuit for the charging loop is shown in Fig. 5 (a). The capacitor C_3 is directly connected to the input source voltage in parallel through four switches. Therefore, in the charging loop, only the ON-state resistance of switches r_{sw} along with the equivalent series resistance (ESR) of capacitor r_{ESR} is connected to the capacitor C_3 with the voltage source. Fig. 5 (b) and (c) depicts the discharging loop during the voltage levels of $\pm 1.5V_{dc}$, and $\pm 2V_{dc}$ respectively. As the load is connected in the discharging loop, the time constant of the discharging circuit has a higher value compared to the charging circuit. The larges time constant in the discharging loop restricts the rapid voltage drop of the capacitor voltage and it gets charged to maintain the voltage drop during the next cycle of charging. Therefore, over a complete fundamental period, the charging and discharging of the capacitor is maintained to the voltage magnitude equal to the dc voltage source V_{dc}.

Fig. 6 shows the variation of capacitor voltage V_{C3} for all positive voltage levels with NLCPWM. Over a half cycle, the capacitor C_3 is charged during zero voltage level i.e., from (0 to t_1) and from (t_8 to t_9). The capacitor voltage is maintained to V_{dc} during voltage levels of $0.5V_{dc}$ and V_{dc}. As the capacitor discharged during the voltage level of $1.5V_{dc}$ and $2V_{dc}$, the capacitor voltage drops to $V_{dc} - \Delta V_{C3}$ where ΔV_{C3} is the allowed voltage ripple of capacitor as given in (2). Again from (t_6 to t_7), the capacitor C_3 is connected in parallel to the input voltage source and get charged upto V_{dc}. The same pattern is repeated during negative voltage levels.

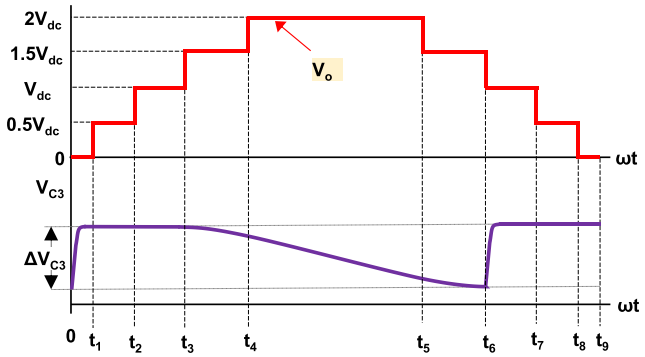

FIGURE 6. Output voltage with the variation of capacitor voltage V_{C3}.

TABLE 2. Comparison between proposed Topology and topologies with single source configuration.

Top	N_L	N_{sw}	N_{gd}	N_d	N_{cap}	$TSV_{p.u.}$	$MBV_{p.u.}$	G
[20]	9	12	12	0	3	5	1	1.0
[23]	7	10	8	0	4	7.3	1.33	1.5
[25]	7	10	8	0	3	5.3	0.67	1.5
[27]	7	9	8	1	3	6.3	1	1.5
[28]	7	12	11	0	5	5	0.33	0.5
[29]	7	9	8	0	3	5.3	0.67	1.5
[P]	**9**	**11**	**10**	**0**	**3**	**5**	**0.5**	**2**

N_L = Number of levels, N_{sw} = Number of switches, N_d = Number of diodes (excluding anti-parallel diode connected to a MOSFET), N_{dc} = Number of dc voltage sources, N_{cap} = Number of capacitors, N_{gd} = Number of gate driver circuit, $TSV_{p.u.}$ = Total standing voltage (in per unit), $MBV_{p.u.}$ = Maximum blocking voltage of an individual switch (in per unit), VB = Voltage boosting ability of the topology, [P] = Proposed

III. COMPARATIVE STUDY

In this section, a comparison between the proposed and other similar topologies has been conducted. The comparison has been carried out in terms of number of switches, number of the gate driver circuit, number of levels, number of capacitors and terms related to voltage stress and gain which are calculated as

$$\left.\begin{aligned} TSV_{pu} &= \frac{TSV}{V_{o,peak}} \\ MBV_{pu} &= \frac{MBV}{V_{o,peak}} \\ Voltage\ gain &= G = \frac{V_{o,peak}}{V_{step}} \end{aligned}\right\} \quad (3)$$

Table 2 gives the quantitative comparison of various topologies with the proposed one. The topology in [20] along with the proposed one achieves nine-level output voltage, however, the topology of [20] has a unity voltage gain and does not boost the input supply voltage, whereas the proposed topology gives twice voltage gain. Furthermore, [27] and [29] uses less number of switches compared to the proposed topology, however, the voltage gain of both topologies have a value lower than the proposed topology. In addition, both topologies have higher TSV_{pu} and MBV_{pu}. The topology proposed in [28] has same TSV_{pu} and lower MBV_{pu}, however, the voltage gain has a value of 0.5 with a higher number of switches and capacitors compared to all other topologies listed in Table 2.

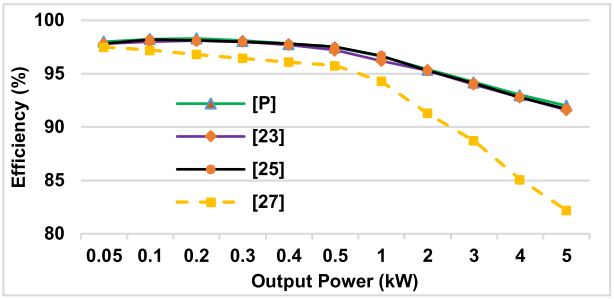

FIGURE 7. Efficiency comparison of different topologies.

A cost comparison has also been carried out with the topologies listed in Table 2. For a fair comparison, the normalized cost has been calculated by dividing the total cost with the value of voltage gain.

$$\text{Normalized Cost} = \frac{\text{Total Cost}}{\text{G}} \quad (4)$$

For the cost comparison, the input voltage has been selected as 600V and the different components of topology have been selected accordingly. Form Table 3, the proposed topology gives the lowest normalized cost with respect to all other topologies used in the comparison. The lower cost is due to the lower values of voltage stresses and higher voltage gain.

In addition to quantitative and cost comparison, efficiency has also been taken into consideration. The equal peak of output voltage is used to estimate its efficiency. Fig. 7 depicts the efficiency variation with respect to output power. The proposed topology has similar efficiency to the topologies proposed in [23] and [25] and higher than [27]. Therefore, from Table 2, Table 3 and Fig. 4, the newly proposed topology performed better compared to other topologies.

IV. RESULTS AND DISCUSSION

A. SIMULATION RESULTS

The results of the proposed topology are simulated using PLECS software. For the simulation, the dc input voltage is selected as 200V. The carrier frequency for the PD-PWM has been selected as 2.5 kHz with an output frequency of 50 Hz. The output voltage, output current and switched capacitor voltage V_{C3} for a purely resistive load of 50Ω is shown in Fig. 8 (a). With the input voltage of 200V, the peak of the output voltage has a value of 400V, which verifies the twice voltage gain of the proposed topology. The nine-level output voltage has a voltage step of 100V. For the boosting of input voltage, the capacitor C_3 is charged up to 200V and is maintained at 200V as depicted in Fig. 8 (a). Similarly, the various waveforms for the proposed nine-level topology with a series-connected resistive-inductive load of 200mH and 10Ω have been illustrated in Fig. 8 (b). With different loading conditions, the capacitor voltage for both cases

TABLE 3. Cost Comparison Between proposed 9LBI and Recently Introduced Topologies with Single Source Configuration.

Component	Part Number	Rating	Unit Price ($)	Topology						
				[20]	[23]	[25]	[27]	[28]	[29]	**Proposed**
MOSFET*	IRFP9140NPBF	100V, 23A	2.2	4	-	-	-	6	-	-
	IRFP240PBF	200V, 20A	2.68	-	-	-	-	6	-	-
	AUIRFSL6535	300V, 19A	3.32	6	2	4	2	-	2	**2**
	IXFH18N60X	600V, 18A	6.49	**2**	6	6	6	-	**7**	**9**
	IXFT18N90P	900V, 18A	9.426	-	-	-	1	-	-	-
	IXFX20N120	1200V, 20A	18.21	-	2	-	-	-	-	-
Diode*	VS-20ETF06SLHM3	600V, 20A	3.1	-	-	-	1	-	-	-
Capacitor*	ALF20G102KL600	600V, 1000µF	48.62	-	2	1	1	-	1	**1**
	ALS81H102DE350	300V, 1000µF	10.55	2	2	2	2	2	2	**2**
	ALF20G102EC200	200V, 1000µF	7.31	1	-	-	-	2		-
	ELG108M100AR2AA	100V, 1000µF	3.18	-	-	-	-	1		-
Gate Driver	IR2110	-	1.8	12	8	8	8	11	8	**10**
Total Cost ($)				91.71	214.74	136.34	129.25	79.43	136.19	**152.77**
Normalized Cost ($)				91.71	143.16	90.89	86.16	158.86	90.79	**76.38**

*www.digikey.com

remained at 200V, demonstrating the self-voltage balancing of the capacitor voltage V_{C3}.

Furthermore, the proposed topology has been tested with the dynamic loading and change of modulation index. Fig. 9 (a) shows the waveforms of the output voltage, output current and switched capacitor voltage V_{C3} with changing load type and load parameters. First, the load is of purely resistive nature with $Z_1 = 25\Omega$ and at time 0.15 sec, the value of the load is doubled to $Z_2 = 50\Omega$, reducing the load current to half of its previous value of load current (i.e., the peak of load current reduced to 8A from 16A). At time 0.2 sec, the load type is changed from resistive to series-connected resistive- inductive load with $Z_3 = 100\text{mH} + 25\Omega$. The load current now changes its nature from a staircase to almost a sinusoidal waveform with a peak value of 9.9A. Furthermore, at the time of 0.25 sec, the load parameters are changed to $Z_4 = 100\text{mH} + 25\Omega$, which results in a reduction of the peak current value from 9.9A to 6.7A. With all these variations of load parameters, the capacitor voltage V_{C3} remains balanced with the change in the ripple voltage.

In addition to variation in the load parameters, the change of modulation index has also been simulated for the proposed nine-level topology. Fig. 9 (b) illustrates the effect of change of MI on the output voltage, output current and capacitor voltage with a load of $Z = 50\text{mH} + 20\Omega$. With MI = 1.0, the rms value of output voltage has a magnitude of 281.5V. Now at time 0.3 sec, the value of MI is changed to 0.8 which reduces the rms value of output voltage to 228.6V. However, with MI = 0.8, the number of levels does not change from nine. Again, at the time of 0.35 sec, the MI is changed to 0.5, which results in the reduction of the number of levels from nine to five with a reduction in rms value to 146.3V.

Additionally, the proposed nine-level topology has been tested with the NLCPWM technique. Fig. 10 illustrates the output voltage, current and capacitor voltage waveforms for a transition of modulation technique, i.e., from PD-PWM to NLC-PWM. The parameter of the load during the change of modulation technique has been selected as $Z = 100\text{mH} + 25\Omega$. With all the simulation experiments, the proposed topology gives satisfactory results in all operating conditions with self-voltage balancing of the capacitor voltage. In addition, Fig. 10 (b) and (c) depicts the harmonic spectrum of the nine level output voltage with PD-PWM and NLCPWM respectively. With PD-PWM, the value of THD is 14.1% whereas with NLCPWM, the amout of THD is 9.4%. However, with PD-PWM, the lower order harmonics has has very low value compare to lower order harmonics of NLCPW as shown in Fig. 10 (b) and (c).

The power loss distribution for the proposed topology has been carried out by modeling the semiconductor devices in PLECS software. Table 4 gives the power loss of all switches and capacitors together with the efficiency of the proposed topology with an output power of 500W and 2000W. The switching power loss (P_{sw}) and conduction power loss (P_c) of the switches have also been given in Table 4. The maximum power loss is associated with the switch pair (S_3, S_4) and (S_7, S_8). The higher power loss of these switch pairs are due to their operation during the charging and discharging of the switched capacitor C_3.

Furthermore, the variation of efficiency against the output power with both PD-PWM and NLCPWM are shown in Fig. 11. The maximum efficiency of the proposed converter has a value of 98.6% at the output power of 100W with NLCPWM. As the output power increases, the efficiency decreases, however, the drop is low and the proposed topology gives 92.2% efficiency at the output power of 5kW. As shown in Fig. 11, the efficiency of the proposed topology has a slighter lesser value with PD-PWM compare

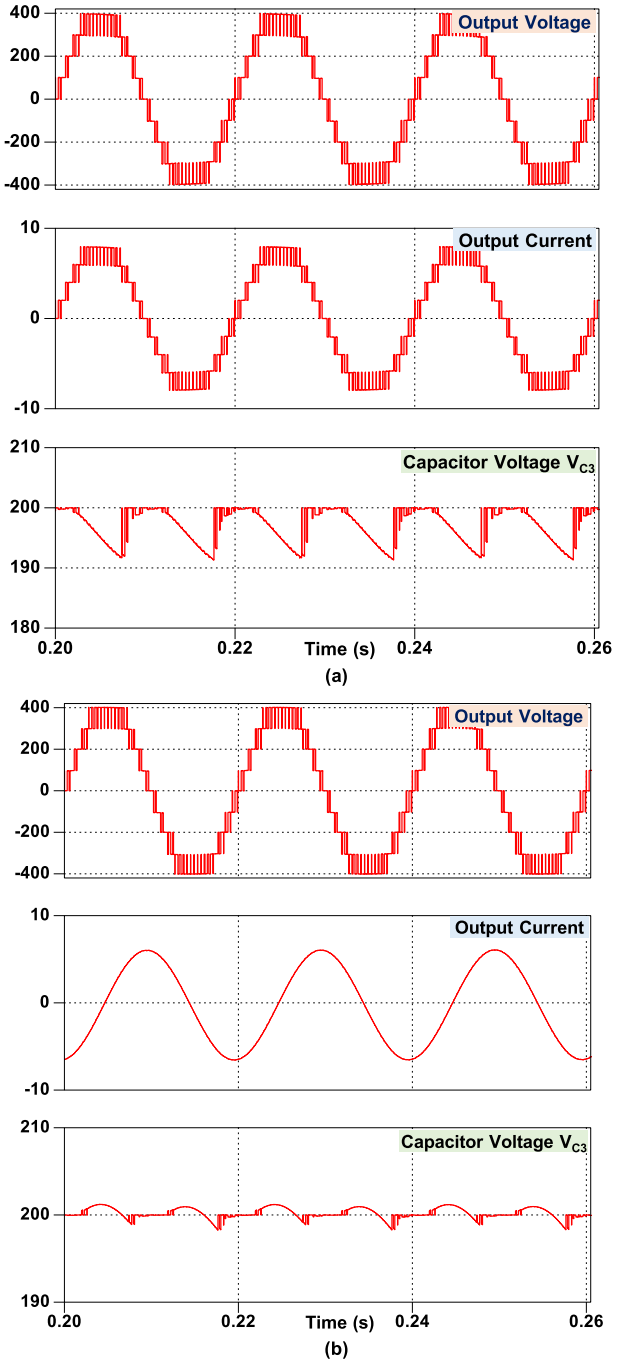

FIGURE 8. Simulation results of output voltage, current and capacitor voltage V_{C3} with (a) purely resistive load Z = 50Ω and (b) series connected resistive-inductive load Z = 200mH + 10Ω.

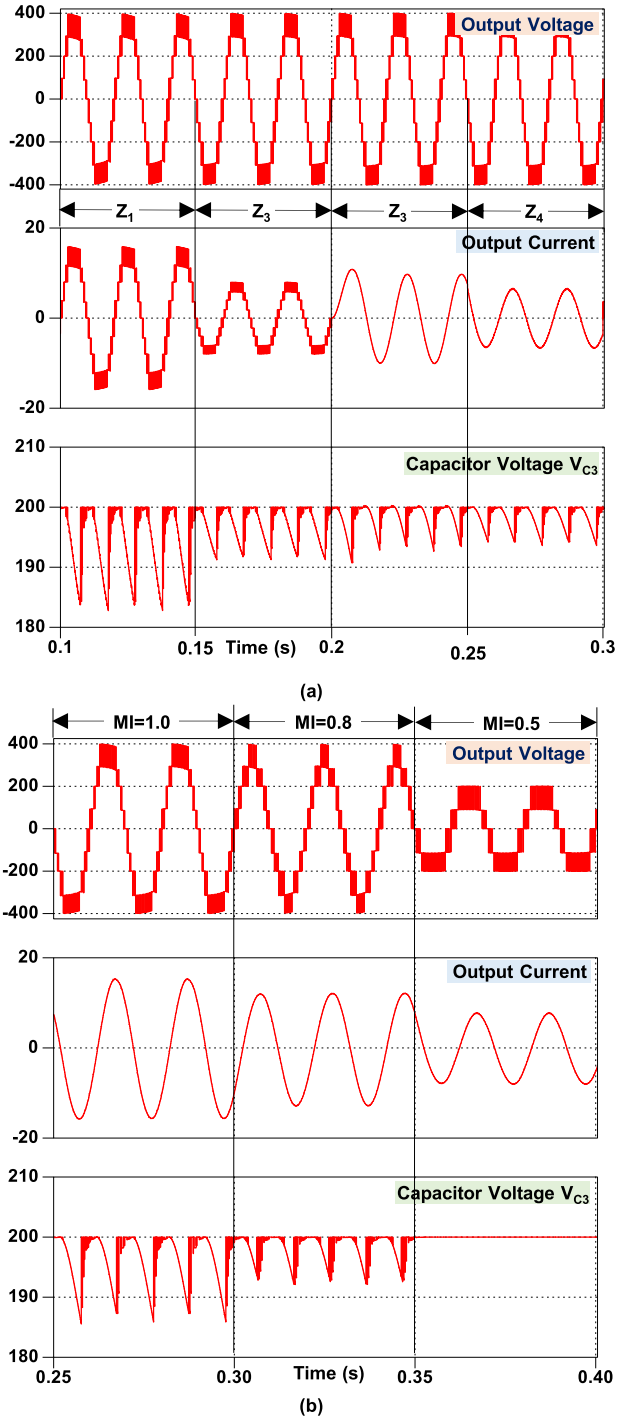

FIGURE 9. Simulation results of output voltage, current and capacitor voltage V_{C3} with (a) change of load and (b) change of modulation index (MI).

to NLCPWM. This is due to the lower switching losses due to lower number of transition of state in NLCPWM compare to PD-PWM.

B. EXPERIMENTAL VALIDATION

To validate the simulation results of the proposed nine-level topology, a prototype experimental setup has been developed in the laboratory as shown in Fig. 12. For the generation of gate pulses for different switched, dSPACE has been used with the PD-PWM technique with a carrier frequency of 2.5kHz. NLC-PWM has also been used for the output voltage generation with fundamental switching frequency. The different parameters used for obtaining the experimental results are listed in Table 5.

As the proposed topology generates nine-level output voltage with twice voltage gain, with the input dc voltage source of 70V, the peak of the output voltage has a magnitude

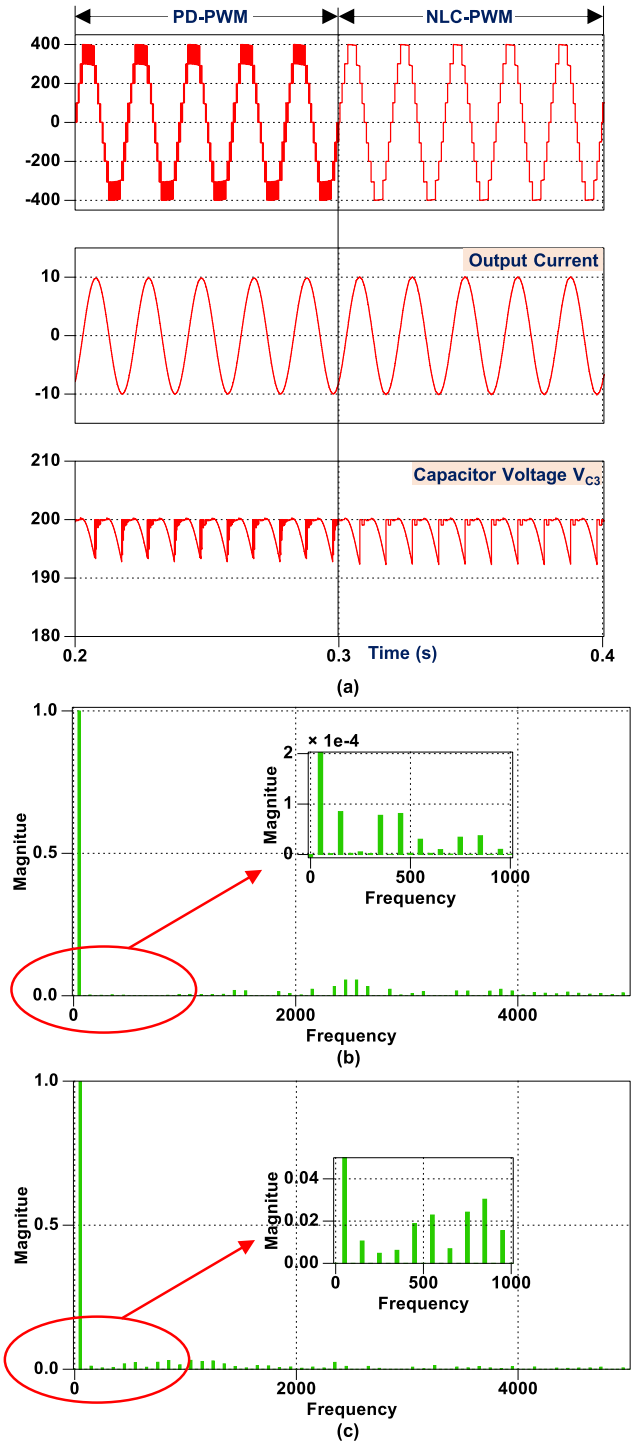

FIGURE 10. Simulation results of (a) output voltage, current and capacitor voltage V_{C3} with change of modulation technique, (b) harmonic spectrum of output voltage with PD-PWM and (c) harmonic spectrum of output voltage with NLCPWM.

TABLE 4. Power loss distribution of the proposed topology.

Power Loss of	Output Power (W)					
	500			2000		
	P_{sw}	P_c	P_{loss}	P_{sw}	P_c	P_{loss}
Switch S_1	0.0043	0.6023	0.6066	0.0048	3.1969	3.2017
Switch S_2	0.0043	0.6019	0.6062	0.0048	3.1969	3.2017
Switch S_3	0.1353	1.5550	1.6903	0.3103	9.224	9.5343
Switch S_4	0.1126	1.5565	1.6691	0.3136	9.2464	9.5600
Switch S_5	0.0477	1.1092	1.1569	0.1041	5.8553	5.9594
Switch S_6	0.0481	0.7436	0.7917	0.0751	5.9561	6.0312
Switch S_7	0.0738	0.5523	0.6261	0.531	9.4268	9.9578
Switch S_8	0.0755	0.4443	0.5198	0.4217	9.4944	9.9161
Switch S_9	0.0144	0.6019	0.6163	0.017	3.1969	3.2139
Switch S_{10}	0.0144	0.6022	0.6166	0.017	3.1969	3.2139
Capacitor C_1	0.04			0.6		
Capacitor C_2	0.04			0.6		
Capacitor C_3	1.96			31.98		
Total Losses	**10.90**			**99.97**		
Efficiency (%)	**97.8**			**95.4**		

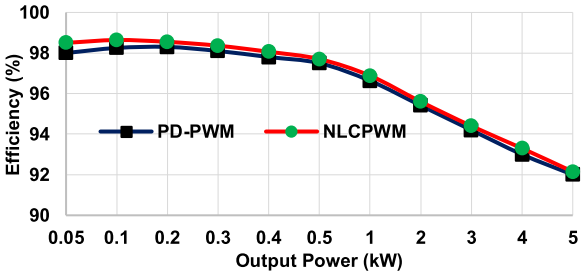

FIGURE 11. Efficiency vs output power curve of the proposed topology.

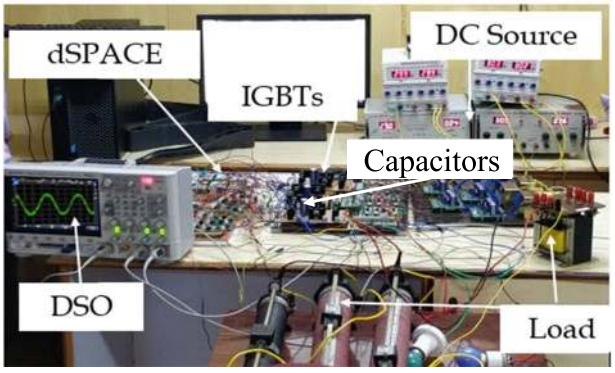

FIGURE 12. Experimental setup of the proposed topology.

of 140V with a step voltage of 35V. Fig. 13 (a) shows the output voltage and current waveform for a series-connected resistive-inductive load with PD-PWM. Fig. 13 (b) illustrates the waveforms of voltage, current and capacitor voltage V_{C3} with a dynamic load condition. The load is changed from a purely resistive load having a magnitude of 100Ω to an RL load of 30Ω+ 30mH. As the load changes, the change of load current from a peak value of 1.4A to 4.8A takes place. However, with the change of load current and load type, the capacitor voltage remain balanced with an increase in the ripple voltage. This shows the self-voltage balancing

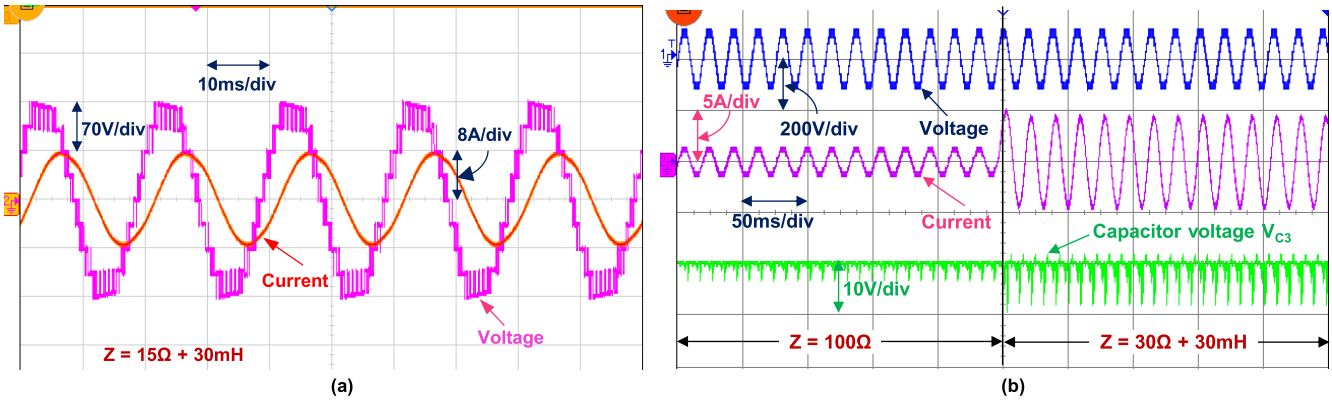

FIGURE 13. Experimental results with PD-PWM (a) output voltage and current waveform with Z = 15 Ω + 30mH and (b) output voltage, current and capacitor voltage waveform for change of load from purely resistive load to series connected resistive-inductive load.

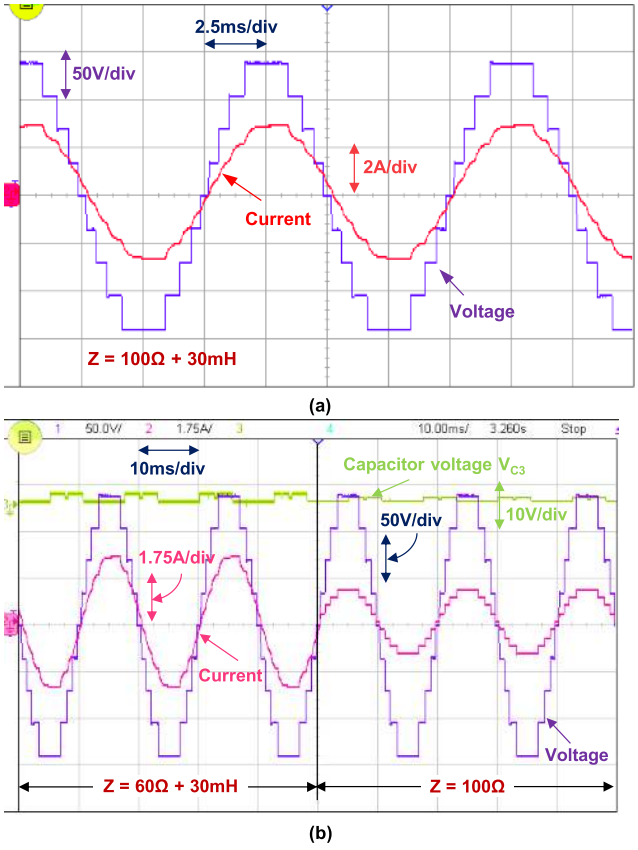

FIGURE 14. Experimental results with NLC-PWM (a) output voltage and current waveform with Z = 15Ω + 30mH and (b) output voltage, current and capacitor voltage waveform for change of load from a series connected resistive-inductive load to purely resistive load.

TABLE 5. Experimental parameters.

Parameter	Value
Input voltage	70V
Outupt voltage	140V peak
Output frequency	50Hz
Carrier frequency	2.5 kHz
Dead band	2μs
Capacitor	Electrolytic capacitor, 2200 μF, 100V
Resistive load (R)	15Ω, 30Ω, 60Ω, and 100 Ω,
Inductive load (L)	30mH

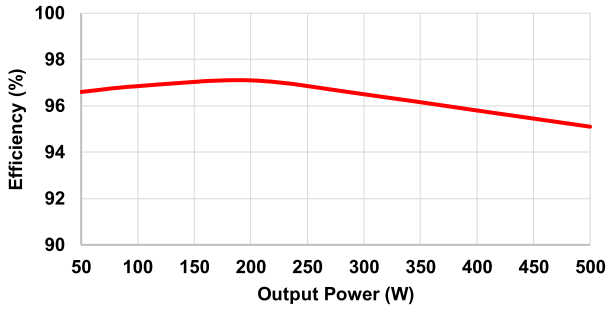

FIGURE 15. Experimental efficiency curve of the proposed topology.

of the capacitor voltage without any auxiliary circuit or any sensors.

Furthermore, the proposed nine-level topology has been tested with the NLC-PWM technique. Similar to Fig. 143 (a), the output voltage and current waveform with series- connected RL load are shown in Fig. 14 (a). A change in loading conditions has also been considered with the NLC-PWM technique. Fig. 14 (b) shows the voltage and current waveforms along with the capacitor voltage with a change of load parameters from series-connected RL load to a purely resistive load. All these experimental results with different loading and modulation technique give the satisfactory performance of the proposed topology with the self-voltage balancing of the capacitor voltage.

Fig. 15 illustrates the efficiency curve of the proposed obtained from the experimental setup using PD-PWM with 2.5kHz. With a load of 100 Ω, the output power measured was 100W, at which the measured efficiency was 97.8%.

Similarly, by varying the load, the efficiency for different output power has been shown in Fig. 15.

V. CONCLUSION

A new multilevel inverter topology has been proposed in this paper. The proposed topology has a better performance parameters in terms of the number of switches, capacitor voltage rating for higher voltage gain, self-voltage balancing of capacitor voltage along with lower cost and higher efficiency compare to other topologies. Above merits of the proposed topology have been proven through a detailed comparative analysis. The proposed topology has been simulated using PD-PWM and NLCPWM modulation techniques considering different loading parameters. Lastly, the simulated results have been verified through the results obtained from the hardware experimental setup.

ACKNOWLEDGMENT

The statements made herein are solely the responsibility of the authors.

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