A new single-photon avalanche diode in 90nm standard CMOS technology

Mohammad Azim Karami,[1,*] Marek Gersbach,[2] Hyung-June Yoon[1], and Edoardo Charbon[1,2]

[1]*Faculty of EEMCS, Technical University of Delft, Mekelweg 4, 2628 CD, Delft, Netherlands*
[2]*School of Engineering, Ecole Polytechnique Fédérale Lausanne (EPFL), 1015 Lausanne, Switzerland*
**m.a.karami@tudelft.nl*

Abstract: We report on the first implementation of a single-photon avalanche diode (SPAD) in 90nm complementary metal oxide semiconductor (CMOS) technology. The detector features an octagonal multiplication region and a guard ring to prevent premature edge breakdown using a standard mask set *exclusively*. The proposed structure emerged from a systematic study aimed at miniaturization, while optimizing overall performance. The guard ring design is the result of an extensive modeling effort aimed at constraining the multiplication region within a well-defined area where the electric field exceeds the critical value for impact ionization. The device exhibits a dark count rate of 8.1 kHz, a maximum photon detection probability of 9% and the jitter of 398ps at a wavelength of 637nm, all of them measured at room temperature and 0.13V of excess bias voltage. An afterpulsing probability of 32% is achieved at the nominal dead time. Applications include time-of-flight 3D vision, fluorescence lifetime imaging microscopy, fluorescence correlation spectroscopy, and time-resolved gamma/X-ray imaging. Standard characterization of the SPAD was performed in different bias voltages and temperatures.

OCIS codes: (000.2700) General science.

References and links

1. S. Takeuchi, J. Kim, Y. Yamamoto, and H. H. Hogue, "Development of a high-quatum efficiency single-photon counting system," Appl. Phys. Lett. **74**(8), 1063–1065 (1999).
2. S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa, "Avalanche photodiodes and quenching circuits for single-photon detection," Appl. Opt. **35**(12), 1956–1976 (1996).
3. C. Niclass, A. Rochas, P. A. Besse, and E. Charbon, "Design and Characterization of a CMOS 3-D Image Sensor Based on Single Photon Avalanche Diodes," J. Solid-State Circuits **40**(9), 1847–1854 (2005).
4. C. Niclass, M. Sergio, and E. Charbon, "A single Photon Avalanche Diode Array Fabricated in 0.35µm CMOS and based on an Event-Driven Readout for TCSPC Experiments," Proc. SPIE Optics East (2006).
5. M. Gersbach, J. Richardson, E. Mazaleyart, S. Hardillier, C. Niclass, R. Henderson, L. Grant, and E. Charbon, "A low-noise single-photon detector implemented in a 130nm CMOS imaging process," Solid-State Electron. **53**(7), 803–808 (2009).
6. M. A. Karami, M. Gersbach, and E. Charbon, "A New Single-photon Avalanche Diode in 90nm Standard CMOS Technology", SPIE Optics and Photonics, (2010).
7. H. Finkelstein, M. J. Hsu, and S. C. Esener, "STI-Bounded Single-Photon Avalanche Diode in a Deep-Submicrometer CMOS Technology," Electron. Device Lett. **27**(11), 887–889 (2006).
8. C. Niclass, M. Gersbach, R. Henderson, L. Grant, and E. Charbon, " A Single Photon Avalanche Diode Implemented in 130-nm CMOS Technology," IEEE Sel. Top. Quantum, Electronics. **13**(4), 863–869 (2007).
9. D. Stoppa, L. Pancheri, M. Scandiuzzio, L. Gonzo, G.-F. Dalla Betta, and A. Simoni, "A CMOS 3-D Imager Based on Single-Photon Avalanche Diode," IEEE Trans. Circ. Syst. **54**(1), 4–12 (2007).
10. A. Rochas, M. Gosch, A. Serov, P. A. Besse, R. S. Popovic, T. Lasser, and R. Rigler, "First Fully Integrated 2D-Array of Single Photon Detectors in Standard CMOS Technology," IEEE. Photon. Tech, **15**(7), 963–965 (2003).
11. H. Kwon, M. Kang, B. Park, J. Lee, and S. Park, "The Analysis of Dark Signals in CMOS APS Imagers from the Characterization of Test Structures," IEEE Trans. Electron. Dev. **51**(2), 178–184 (2004).

#134338 - $15.00 USD Received 31 Aug 2010; revised 23 Sep 2010; accepted 23 Sep 2010; published 5 Oct 2010

1. Introduction

Photon counting devices are being used in a wide range of applications from quantum key distribution systems to single molecule detection [1,2]. In the last few years, a flurry of activity has led to the development of a family of solid-state single-photon detectors, known as single-photon avalanche diodes (SPADs), in a number of CMOS technologies for different applications of science and engineering. CMOS SPADs have demonstrated their usefulness in applications where low-noise, high timing resolution, and high dynamic range are important or even critical [3]. Moreover thanks to CMOS-mediated miniaturization, the integrations of millions of pixels with single-photon detection capability on a single chip is becoming feasible [4]. Hence, the reduction of pixel pitch which is bounded by the scalability of the pixels would facilitate having more electronics on a single imager chip thus putting more functionality for sensing applications [5].

Generally speaking, SPADs are characterized by photon detection probability (PDP), dark count rate (DCR), timing resolution, afterpulsing probability, dead time, and the overall speed of operation [5]. Although the smaller CMOS feature size advantageously enables smaller pitch, the integration of smaller electronics on-pixel may result in higher fill factor, which, in turn, enables better photon statistics and higher quality imaging. Unfortunately, using standard deep-submicron CMOS processes involves higher doping, thinner profiles and thicker optical stacks, thus increasing noise and decreasing photon sensitivity.

In this paper we describe the implementation of a SPAD in 90nm standard CMOS technology that was announced for the first time in [6]. To the best of our knowledge, this is the first SPAD implemented in a feature size smaller than 130nm [3,7,8]. By implementing different SPAD structures in this technology we could study the geometric trade-offs involved in the design of deep-submicron SPADs. 162 different SPADs with different arrangements of doping layers and different guard ring sizes were implemented. Among them, 45 different structures work properly in the single photon counting mode with different breakdown voltages and different characteristics.

The paper is organized as follows. After describing the fundaments of CMOS SPADs and the simulation results at the basis of the guard ring model, we outline the optical characterization of the device in terms of the various parameters.

2. SPAD principle, structure and simulation

A SPAD is based on a p-n junction biased in the reverse mode of operation above breakdown voltage, in the so-called Geiger mode [9]. In this mode, electron and holes generated by photon absorption may initiate a process known as avalanche multiplication, whereby each free electron or hole causes a large number of free electrons and holes by impact ionization. The avalanche caused by photon or noise sources must be quenched, in order to restore the SPAD for sensing new incoming photons; this process is known as avalanche quenching and it can be performed using passive or active methods [3]. In this work, a passive quenching resistor is being used for simplicity to explore the highest levels of miniaturization possible in this technology. The avalanche pulse is converted to a digital signal by using a simple inverter. Again, in order to explore miniaturization trade-offs, more complex circuits are intentionally avoided [8].

The noise performance of SPADs is mainly characterized by dark counts which are spurious pulses quantified in terms of mean frequency, or dark count rate (DCR), and afterpulsing [10]. In order to reduce the DCR of a SPAD, different methods have been employed to decrease the Shockley-Read-Hall (SRH) generation and Tunneling [10]. The sensitivity of SPADs is evaluated by the probability that an impinging photon triggers an avalanche, known as photon detection probability (PDP) as a function of impinging wavelength. Finally, the timing resolution or timing jitter is defined as the uncertainty of the time delay between the photon impingement and the leading edge of the pulse generated by the sensor.

#134338 - $15.00 USD Received 31 Aug 2010; revised 23 Sep 2010; accepted 23 Sep 2010; published 5 Oct 2010

Figure 1 shows the cross-section of the SPAD family implemented in 90nm CMOS technology. *Note that in designing this family of devices only standard masks were used*. A combination of Shallow Trench Isolation (STI) and n-well is used as guard ring for preventing premature edge breakdown. Different types of guard ring with different size and depths were integrated and fully characterized. The purpose of using a guard ring is to shape the electric field in the active area so as to maximize the high electric field present in the design at the center of the multiplication region and to decrease it at the corners. However, the introduction of some annealing steps near the STI structures which are used in this design can lead to detrimental effects to the noise performance [11].

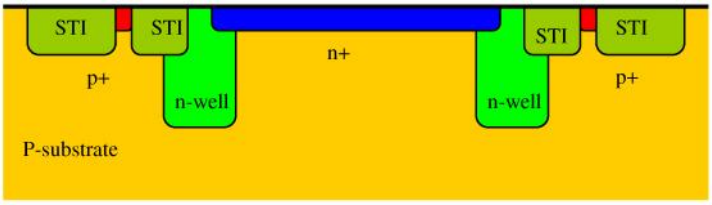

Fig. 1. Cross-section of one of the structures implemented for this family of SPADs.

Figure 2 shows the photomicrograph of the SPAD farm implemented in the target CMOS technology. In the inset, a detail of a SPAD is shown. The photon sensitive area is in the center of the octagonal shape and the other parts are covered with metal in order to reduce the side effect of the absorption of photons in the guard ring area. For this prototype, we used several sizes; in this paper we focus on a structure with an edge of 8μm.

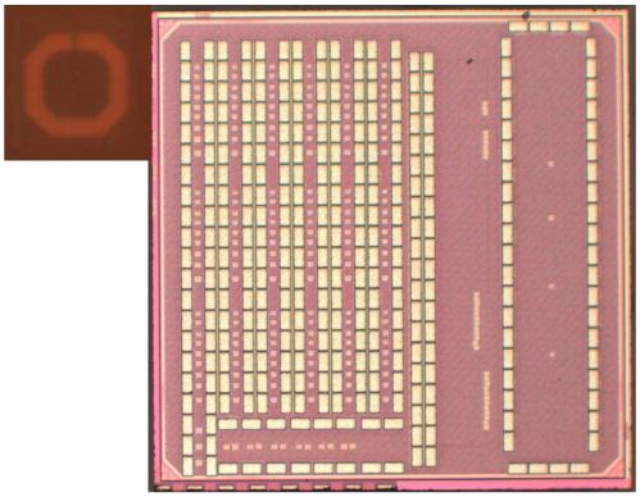

Fig. 2. Photomicrograph of the SPAD farm and a detail of the octagonal SPAD in the inset.

In order to achieve single-photon counting capability, the electric field must be uniform in the planar junction region where the multiplication occurs. All free carriers generated by photons will trigger the avalanche breakdown while free carriers in the guard ring would not gain enough energy by the electric field to initiate the breakdown. In other words, to sustain an avalanche process at a given excess bias voltage, the planar region must be biased above the breakdown voltage whereas the rest of the diode voltage is lower than the breakdown [5]. Figure 3 shows the electric field distribution of the SPAD at 0.2V of excess bias voltage. The combination of different doping layers with different sizes is arranged in such a way to form a proper guard ring in order to confine the highest electric field to the planar active area. The simulation of the designed SPAD is carried out by importing the doping profiles from the 90nm technology using the SPECTRA® imager simulator.

#134338 - $15.00 USD Received 31 Aug 2010; revised 23 Sep 2010; accepted 23 Sep 2010; published 5 Oct 2010

It should be noted that, by forming a proper guard ring is a major challenge due to the high doping concentration profiles of shallower layers available in the technology.

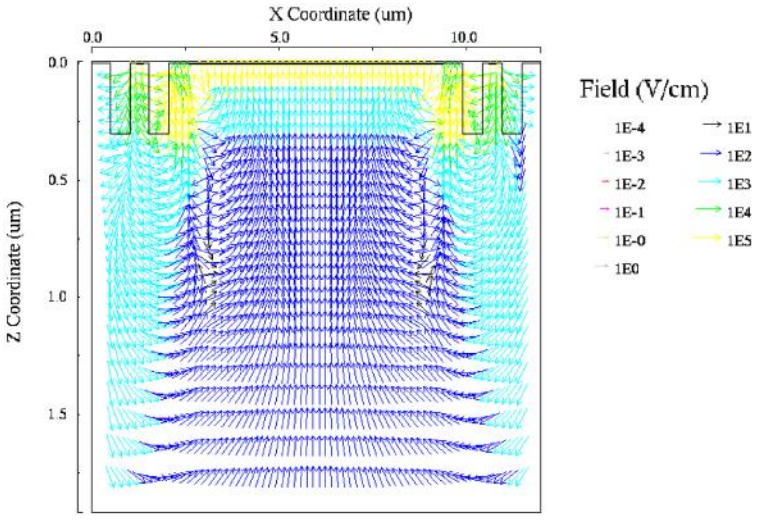

Fig. 3. Electric field distribution of the SPAD above breakdown.

Figure 4. shows the value of the electric field being simulated in different depths of the device. The picture shows that the guard ring is mostly effective near the surface of SPAD, where most of the photon absorption takes place.

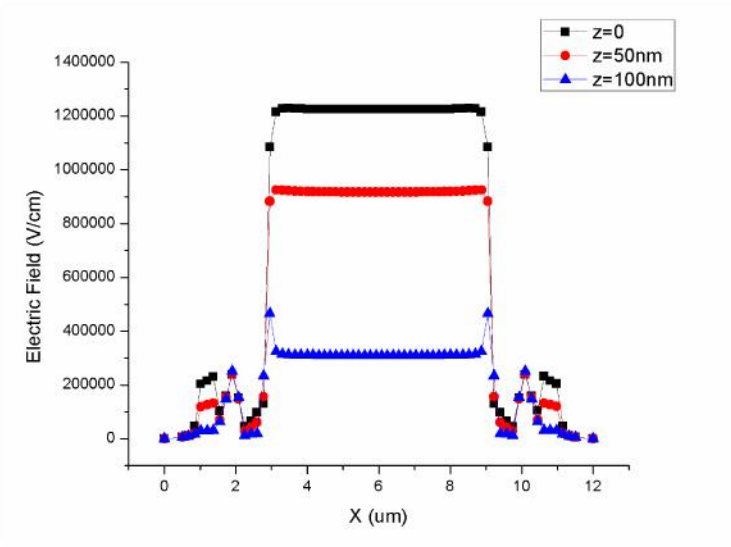

Fig. 4. Electric field value in a cross-section of SPAD in different depths.

While the diameter of the anode part is kept to the constant value of 8µm, different combinations of n + and n-wells are examined as anode. The thickness of n-wells are constrained by the DRC (design and rule check) of the standard CMOS technology, and starts from 500nm to 2µm. While, different distances are being used as the penetration depth of STI in the n-well guard ring starting from 100 to 500nm, the penetration depth of anode in the guard ring changes from 200 to 500nm. Among the simulated and implemented structures, thicker and deeper guard ring shows better performance. It should be noted that the deep n-

#134338 - $15.00 USD Received 31 Aug 2010; revised 23 Sep 2010; accepted 23 Sep 2010; published 5 Oct 2010

well with the low doping concentration played an important role in the guard ring formation in the reported SPAD.

The reported device has no isolation technique being used to separate the potential of the anode from the ground. With this design indeed there is a need for introducing decoupling between the cathode and the input to the next stage if this is to be used in an array of detectors. The obvious techniques to solve this problem are (1) a capacitive decoupler or resistive partitor that require more area and possibly introduce noise, especially in time-resolved imaging; (2) placing the electronics in a deep n-well with a contained p-well and bias the entire substrate at a high negative voltage. This is a non-standard approach and may interfere with a conventional semi-custom design flow. In addition, a p-well/deep n-well option may not always be available in standard deep-submicron CMOS technologies. If that were not the case, NMOS digital circuitry may be used as a workaround, with the consequences in terms of leakage and power consumption; (3) use of SOI process. This solution is a valuable one and could actually offer other advantages in terms of noise isolation and PDP boosting.

3. Experimental results

Figure 5. shows the I-V characteristic of the SPAD in the reverse bias mode of operation. Although in some of the integrated SPADs in this technology the series resistance affects the I-V curve, the breakdown behavior of the diode in this figure is proper for the photon counting applications.

The breakdown indicates that tunneling is high in these devices. This is to be expected due to the relatively high doping levels of the substrate. That is why the excess bias has to be kept low to avoid high DCR while PDP still has acceptable levels. The pre-breakdown current is in the nA range which is indeed a large dark current, however, this does not present a problem since it is not related to the DCR mechanisms. It only implies a slightly larger power dissipation especially in regimes of high illumination.

In order to characterize the number of spurious pulses being generated by tunneling and SRH process the Dark Count Rate (DCR) is being measured. Designing the low DCR SPAD is important for photon-starved applications. However, medium or high range noise SPADs can be used in commercial imaging systems, e.g. 3D vision systems. These systems can sustain relatively high DCRs (in the order of a few tens of kilohertz) using noise rejection algorithms well -adapted to pulsed and modulation-based time-of-flight cameras [3].

#134338 - $15.00 USD Received 31 Aug 2010; revised 23 Sep 2010; accepted 23 Sep 2010; published 5 Oct 2010

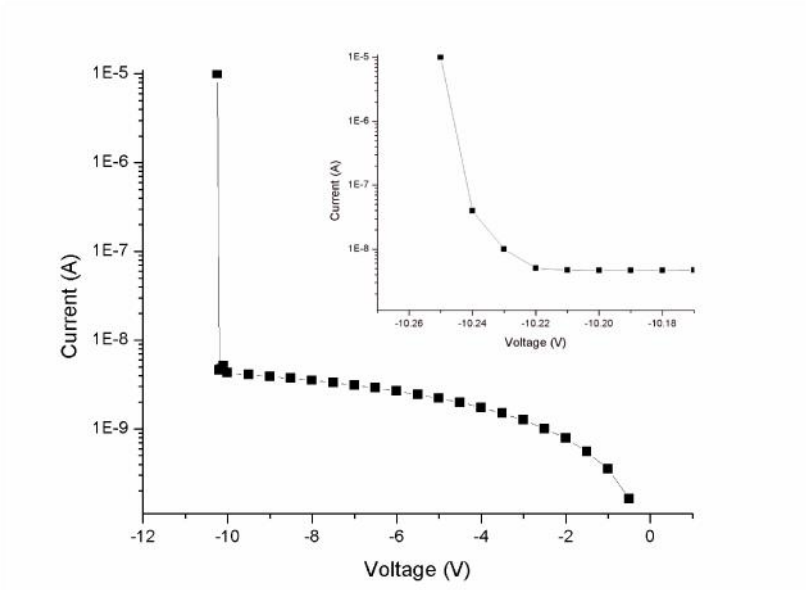

Fig. 5. The I-V characteristic of the 90nm diode which shows photon counting ability.

Figure 6 shows the DCR of the fabricated SPAD at different temperatures and excess bias voltages. Passive quenching is being used in the first prototype of the implemented SPAD. Although tunneling effects increase the DCR with the temperature, the major temperature-dependent DCR contribution is SRH. The SPADs being introduced in this paper exhibit 8.1 kHz of DCR noise at room temperature with 0.13 Volts of excess bias voltage. The DCR can be decreased by further decreasing temperature and/or excess bias voltage. Due to relatively large dead time, the SPAD enters saturation relatively early. The DCR in the plot of Fig. 6 is not shown after saturation is reached. Higher DCR is to be expected due to higher tunneling.

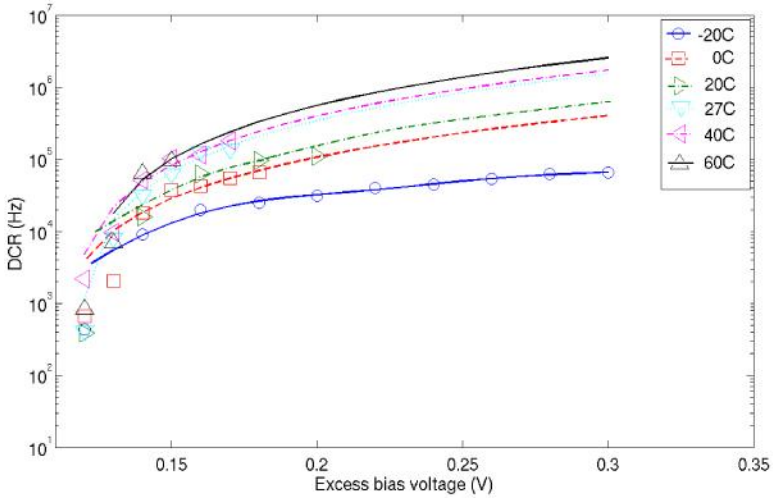

Fig. 6. DCR vs. excess bias voltage for different temperatures.

The PDP is measured for the entire spectrum of interest (360-800 nm). Figure 7 shows the PDP at room temperature at different bias voltages. The figure shows that the detection probability can be as high as 15% at 520nm wavelength. The shallow doping profile of the n + layer in the 90nm CMOS technology is resulting in higher PDP in the ultraviolet region and

#134338 - $15.00 USD Received 31 Aug 2010; revised 23 Sep 2010; accepted 23 Sep 2010; published 5 Oct 2010

a shift of the PDP maximum. The overall lower PDP if compared with the literature [5] is predictable due to the shallower multiplication region. In addition, a thicker optical stack with worse refraction index matching among fabrication layers, causes more attenuation and a higher ripple in the PDP profile.

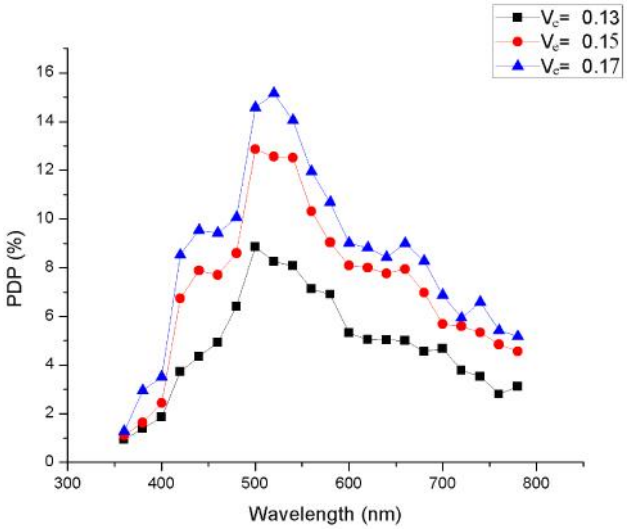

Fig. 7. Photon Detection Probability (PDP) at room temperature.

Timing jitter is characterized using two fast laser sources with a pulse width of 40ps and repetition rate of 40 MHz emitting a beam of light with the wavelength of 637nm and 405nm, respectively. The time interval between the laser output trigger and the leading edge of the SPAD signal is measured via a high performance oscilloscope operating as a TDC. A histogram is constructed from the time difference of the edges of the laser light and sensing signal. Figure 8 shows the histogram of this time difference at wavelength of 405nm. In order to measure the timing behavior the SPAD is biased 0.13V above the breakdown at the room temperature.

The Full Width at Half Maximum (FWHM) of the time difference histogram was measured to 398ps for 637nm and 435ps for 405nm. The jitter on this technology is higher than previous reports [5]. Since the doping concentration of the p-substrate in this technology is lower than the previous deep n-wells, the depletion region extends deeper into the substrate. As a result, photocarriers generated relatively deep into the substrate may be captured, after diffusing, through the substrate, in the multiplication region, thus increasing the uncertainty of the timing of electron-hole pair generation [5]. The higher jitter on the higher wavelength is expectable due to the fact that there is no n-well to restrict the absorption region of the SPAD and, by increasing the wavelength the photon is going to be absorbed in a region with more depth. The high distance between the absorption region and the multiplication region will cause higher jitter for higher wavelength in this case.

#134338 - $15.00 USD Received 31 Aug 2010; revised 23 Sep 2010; accepted 23 Sep 2010; published 5 Oct 2010

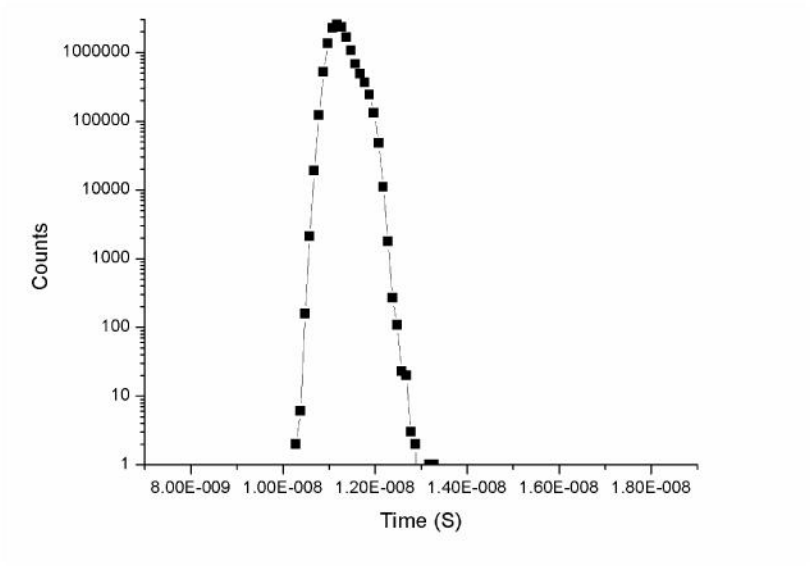

Fig. 8. Histogram of the time between the laser pulse and the SPAD receiving digital pulse at 405nm wavelength.

Figure 9 shows the result of afterpulse probability measurement as a function of dead time. The afterpulsing measurement was carried out by the discrete autocorrelation measurement of the signal.

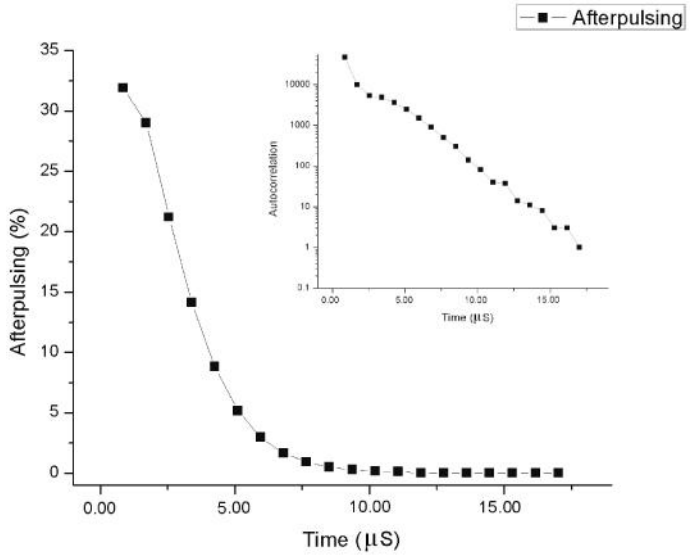

Fig. 9. Afterpulse probability as a function of dead time. In the inset the corresponding autocorrelation.

The main reason for the afterpulsing generation is the traps in the depletion region that add a history effect by initiating the avalanche independently. Since the depletion region in the substrate side is thicker the probability of having traps in the depletion region would be higher and the afterpulsing probability would increase correspondingly. The dead time of the detector is 1.2 μs. A large parasitic capacitance in parallel to the anode of the device is largely responsible for a long recharge time that, in turn, dominates the dead time. High afterpulsing probability is due to a relatively large charge of approximately 17.85pC involved in each

#134338 - $15.00 USD Received 31 Aug 2010; revised 23 Sep 2010; accepted 23 Sep 2010; published 5 Oct 2010

avalanche. Large numbers of carriers are undesirable in SPADs as they result in higher probability of trapped carriers that are prone to the generation of secondary spurious avalanches. The active quenching circuitry is being implemented with the SPAD to overcome the large dead time in the next design.

Table 1. Summary of experimental results. All measurements were conducted at room temperature.

Performance	Min	Typ	Max	Unit	Comments
SPAD diameter		8		µm	
DCR		8.1		kHz	$V_e = 0.13$, T = 293K
Timing jitter		398		ps	FWHM at 637nm wavelength
		435		ps	FWHM at 405nm wavelength
PDP		12	15	%	$0.15V_e$ changing with depth and doping of guard ring
Afterpulse probability		32		%	At nominal dead time
Breakdown voltage	10.28	10.4	10.43	V	
Wavelength range	360		800	nm	

The performance of the SPAD implemented in the 90nm standard CMOS technology is summarized in Table 1. While the high DCR is expected because of the tunneling and high doping profiles, the PDP is lower due to high, unoptimized optical stack.

4. Conclusions

To the best of our knowledge, the device reported in this paper is the first SPAD fabricated in 90nm standard CMOS technology; it comprises a multiplication region and a guard ring to prevent premature edge breakdown, all implemented using standard layers. The breakdown voltage of the SPAD is well-controlled and in a range of 10.28V to 10.43V, while the dark count rate tops 8.1 kHz at room temperature and 0.13V of excess bias voltage, but it can be reduced significantly by cooling. A maximum photon detection probability of 9% was measured while a 398nm FWHM of jitter was achieved in the standard temperature range (−20°C – + 60°C), at the same biasing condition. Applications include time-of-flight 3D vision, non-photon-starved fluorescence lifetime imaging microscopy, fluorescence correlation spectroscopy, and time-resolved gamma/X-ray imaging.

Acknowledgements

The authors are thankful to Martin Lanz for his technical support.

#134338 - $15.00 USD Received 31 Aug 2010; revised 23 Sep 2010; accepted 23 Sep 2010; published 5 Oct 2010