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# A New Six-Level Transformer-Less Grid-Connected Solar Photovoltaic Inverter with Less Leakage Current

**Naser Vosoughi Kurdkandi[1], Milad Ghavipanjeh Marangalu[2], Shamim Mohammadsalehian[3], Hadi Tarzamni[4] *(Student Member, IEEE)*, Yam Siwakoti[5], (*Senior Member, IEEE)*, Md Rabiul Islam[6], (*Senior Member, IEEE)*, and Kashem M. Muttaqi[6], (*Senior Member, IEEE)***

[1]Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology, Tallinn, Estonia.
[2]Faculty of Electrical and computer engineering, University of Tabriz, Tabriz, Iran.
[3]Department of Electrical and computer engineering, Western University, London, ON, Canada.
[4]Department of Electrical Engineering and Automation, Aalto University, 02150 Espoo, Finland.
[5]Faculty of Engineering and Information Technology, University of Technology Sydney, Australia.
[6] School of Electrical, Computer and Telecommunications Engineering, Faculty of Engineering and Information Sciences, University of Wollongong, NSW 2522, Australia.

Corresponding author: Hadi Tarzamni (hadi.tarzamni@aalto.fi)

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**ABSTRACT** This paper presents a novel structure of the transformer-less grid-connected inverters. The proposed inverter is combined with six power switches and two power diodes which can generate six voltage levels at the output. Furthermore, the proposed inverter can overcome the leakage current issue in the photovoltaic (PV) system, which is the major problem in grid-tied PV applications. Additional significant features include- reduced filter size, lower total harmonic distortion (THD) of the injected current to the grid, and voltage boosting ability. Moreover, the proposed topology provides full reactive power support to the grid. A control strategy is designed and implemented to provide a voltage boost ability without using any additional dc-dc boost converter. Finally, the performance of the proposed inverter is validated by the 770 $W$ laboratory prototype.

**INDEX TERMS** Transformer-less inverter, voltage boosting ability, leakage current limitation, and photovoltaic application.

## I. INTRODUCTION

Owing to the massive shortage in the conventional fuel-based sources, environmental pollution, and government power regulation incentives, the use of renewable energy sources (RES) like photovoltaic (PV) modules has been more attractive in the novel power conversion systems. In the low scaled single-phase grid-connected topologies, a PV panel can be tied to a power converter directly with a single power conversion stage or two stages. Single-stage power conversion systems prevent wasting extra energy and power losses [1, 2].

On the other hand, inverters without transformers are very important for achieving the proper voltage gain from relatively low solar panels and providing the power grid's proper voltage peak. The grounding issue point is the main challenge in developing a property transformer-less grid-connected inverters.

Higher efficiency, lower cost, proper power density, and meeting some grid code necessities of numerous distributed generation systems are the merits of the transformer-less inverters over the transformer-based systems [1-8]. Voltage fluctuation across the stray capacitor, which emerges between the photovoltaic (PV) panel and the ground, generates the leakage current [9-11]. The mentioned injected leakage current produces a noisy dc offset to the grid, so it is essential to control the same magnitude. Variation in common-mode voltage (CMV), which emerges across the stray capacitor, leads to leakage current. So, by keeping the common-mode voltage constant, the leakage current can be mitigated. For the constant CMV, a bipolar pulse width modulation (PWM) method or half-bridge (HB) inverter instead of the full-bridge (FB) inverter could be used [5, 12, 13]. In [9], the CMV is almost fixed under any condition of loading performance; however, due to the low quality of injected power, the output voltage not able to face strict grid codes standards.

Furthermore, an additional front-end boost converter in HB-based inverters leads to high cost, low power density, and a less efficient system. The unipolar PWM method can mitigate dv/dt, filter size, and power losses, but it causes CMV variation with the switching frequency. Variable high-frequency CMV emerges by producing a zero voltage level at the inverter's output [14, 15]; however, to remove the leakage current and electromagnetic interference (EMI), the PV module should be disconnected from the ac grid during the freewheeling mode. In order to achieve this goal, H5 [16], optimized H5 (OH5) [17], a various family of H6 [18, 19] and HB-ZVRB [20] have been presented by adding some additional switches to the conventional FB topology and isolation between the photovoltaic source and the grid in dc or ac side during the freewheeling period. In [21], the highly efficient and reliable inverter concept (HERIC) topology was presented to reduce the power loss and the leakage

current. This structure generates zero voltage level at the ac side through a bidirectional switch and therefore not only the power loss reduces but also improves the reliability of the system. However, the HERIC topology cannot control the reactive power. The constant CMV across the parasitic capacitors can be achieved using the neutral point clamp (NPC) or active neutral point clamp inverters [22-25]. The central point of two capacitors connected across the PV cells is linked to the neutral/ground terminal of the grid leads to a constant common-mode voltage at each interval of time. But the main disadvantage of this technique is additional dc-dc topologies requirement to increase the output voltage range to connect with the ac grid [13]. The use of those inverters based on common grounded topologies play an important role to maintain the system from the leakage current issue [26]. Two bipolar-PWM-based transformer-less inverters have been introduced inverters by employing the extra inductors common grounding method [27, 28]. When the solar cell's negative terminal is directly linked to the grid's null, the total CMV is appropriately bypassed and presented as a virtual dc link [29]. Recently, to further improve the quality of the injected current to the grid by these common grounded transformer-less inverters, some modified versions of the three-level and five-level based topologies have been introduced, which are based on the flying capacitor (FC) and switched-capacitor (SC) structures [2, 30-32]. In [30, 31], in order to balance the voltage of the FC cell, the additional charge balancing control circuits should be applied.

Applying the switched capacitor strategy into the conventional gird-tied inverters can provide a voltage boosting capability while the charging and discharging operation of the utilized capacitors can be inherent [2, 32].

Another classification of the SC-based MLI topologies are the common grounded inverters that have received more attention from researchers due to CMV reduction feature. In the common grounded inverters, the null of grid is directly tied to negative terminal of the input dc source. In order to establish the common point between ac side and dc side of the inverter, the presented topology in utilizes an electrolytic capacitor to create the concept of virtual dc-bus. Note that, during both positive and zero levels the virtual dc-bus is charged to input voltage. By reversing the polarity of virtual dc-bus the negative voltage level will be generated. It should be noted that in the negative half cycle of output voltage waveform the input dc power supply is not used to supply the output load. So that, the negative polarity of input dc source can remain tied to the null of power grid. In all of the common-grounded SC-based structure, the input dc source is isolated from the output in the negative half cycle. Also, the output levels in the negative half cycle are created only by discharging of the switched capacitors. The ripple voltage of switched capacitors can increase the harmonic distortion of output voltage waveform in the negative half cycle.

Recently, some transformer-less common grounded grid-tied inverter to eliminate leakage current and provide voltage boosting feature during single stage power conversion [33-38]. Also, a new switched capacitor-based common grounded grid-tied five-level inverter has been presented in [39]. This topology can operate with a dynamic voltage conversion and wide input voltage range. Another kind of SC-MLI topology that integrates SC with T-type inverter [40] NPC-based inverter to overcome to dc offset problem during reducing high frequency CMV has been presented in [41]. A new SC-based five-level inverter is presented in [42]. Note that, this topology cannot generate the zero-level of output voltage waveform. Ref [43] presents a new switched capacitor seven-level NPC-based by adding a flying capacitor to the five-level switched capacitor NPC-based presented in [41]. Also, some switched capacitor NPC-based topologies are introduced in [44] and [45]. The NPC-based or T-type switched capacitor inverters provide the best performance compared with other structures. The mentioned topologies utilize a single dc source for producing a seven-level output voltage in both single-phase and three-phase states. The feature of high frequency CMV reduction without any change in the output voltage waveform is very important.

This paper introduces a novel NPC-based transformer-less grid-connected inverter using the switched-capacitor concept, which provides a six-level voltage through a simple structure. The attractive merits of the proposed inverter are boosting output voltage, reducing leakage current capabilities, filter size, and total harmonic distortion (THD) in grid-connected PV applications. The proposed grid-tied inverter's main goal is to reduce filter size and total harmonic distortion (THD) in grid-connected PV applications. Moreover, the leakage current issue is the main problem in grid-tied PV applications, which is solved in the proposed inverter. Indeed, the leakage current on circuits causes unnecessary and irregular tripping also mainly leads to a rise in voltage on accessible conductive parts; thus, it should be solved.

The paper is organized as follows: Section II shows the circuit topology of the proposed grid-connected inverter. Section III discuss the operational principles of the presented inverter. Analyses of the proposed inverter are presented in Section IV. Section V introduces a control scheme and power loss analysis and compares the proposed topology with existing transformer-less grid-connected inverters presented in Section VI and VII, respectively. To validate the proposed grid-tied inverter's performance, the experimental results are presented in Section VIII and finally concludes is in Section IX.

## II. CIRCUIT TOPOLOGY OF THE PROPOSED INVERTER

Fig. 1 shows the proposed inverter's circuit schematic, consisting of two power diodes, four capacitors, and six power switches. $V_{dc}$ is the input voltage, and the switches $S_1$, $S_2$, $S_3$, and $S_4$ are power switches that are located on two legs, and the $S_5$ is the bi-directional power switch. The proposed inverter consists of two switch-legs. The first switch-leg includes switches $S_1$, $S_2$ and the second switch-leg consist of $S_3$ and $S_4$. The capacitors $C_1$ and $C_2$ connected to the input source, which are charged to 0.5 $V_{dc}$ spontaneously. Also, $C_3$ and $C_4$ associated with the second switch-leg and are charged to $V_{dc}$.

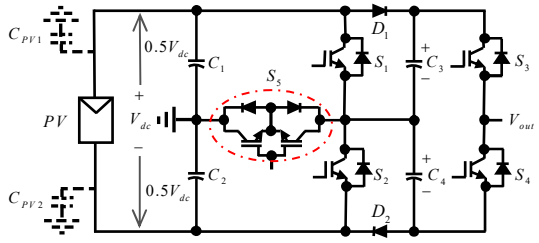



FIGURE 1. **Circuit topology of the proposed inverter.**

TABLE I
SWITCHING STATES OF THE SIX-LEVEL GRID-TIED INVERTER SHOWING CHARGING/DISCHARGING STATE OF THE CAPACITORS

| State | Switching states | | | | | Diode states | | Capacitor states | | Output voltage |
|---|---|---|---|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $D_1$ | $D_2$ | $C_3$ | $C_4$ | $V_{Out}$ |
| III | 1 | 0 | 1 | 0 | 0 | 0 | 1 | ↓ | ↑ | 1.5 $V_{dc}$ |
| II | 0 | 0 | 1 | 0 | 1 | 0 | 0 | ↓ | - | $V_{dc}$ |
| I | 0 | 1 | 1 | 0 | 0 | 1 | 0 | ↑ | - | 0.5 $V_{dc}$ |
| IV | 1 | 0 | 0 | 1 | 0 | 0 | 1 | - | ↑ | -0.5 $V_{dc}$ |
| V | 0 | 0 | 0 | 1 | 1 | 0 | 0 | - | ↓ | -$V_{dc}$ |
| VI | 0 | 1 | 0 | 1 | 0 | 1 | 0 | ↑ | ↓ | -1.5 $V_{dc}$ |

The bidirectional switch $S_5$ is located between the midpoint of $C_1$, $C_2$, and the first leg. The operation of each switching state, diode, and charging/discharging modes of the capacitors is mentioned in Table I. In this table, "1" and "0" show the switches and diodes' in on and off-state, respectively. Also, the non-connecting, charging, and discharging states of the $C_3$ and $C_4$ are indicated by "-", "↑" and "↓", respectively.

## III. OPERATIONAL PRINCIPLES OF THE PROPOSED INVERTER

As indicated in Fig. 2, the proposed grid-connected inverter has six operational modes to generate six different voltage levels (±0.5 $V_{dc}$, ±1 $V_{dc}$ and ±1.5 $V_{dc}$). This figure shows the reactive current path, active current path, and capacitor charging path with green, red, and blue dashed lines. Since $C_1$ and $C_2$ in the first leg are linked to the input voltage, they are charged to 0.5 $V_{dc}$ ($V_{C1} = V_{C2} = 0.5\ V_{dc}$) in the whole of the operational modes. The corresponding switching states are discussed in detail as below:

***Mode* I:** In this mode, the capacitor $C_3$ in the second leg is charged to $V_{dc}$, and $C_4$ is disconnected as $D_2$ is reversed biased, as seen in Fig. 2(a). Furthermore, $C_1$ supplies the grid power and 0.5 $V_{dc}$ is developed at the output by turning on switch $S_3$. The related equations of this mode can be written as:

$$V_{C3} = V_{dc} \tag{1}$$

$$V_{out} = V_{C1} = 0.5 V_{dc} \tag{2}$$

Considering Fig. 2(a), the power switches $S_1$, $S_4$, and $S_5$ are in OFF-state, the voltage stress of these switches can be calculated as follows:

$$V_{S1} = V_{C3} \tag{3}$$

$$V_{S5} = V_{C2} \tag{4}$$

***Mode* II:** In this mode, the $C_3$ is discharged to supply the grid power as shown in Fig. 2(b). However, $C_4$ at the end of the mode is connected to start charging in the third operational mode. The output voltage in this mode can be written as:

$$V_{out} = V_{C3} \tag{5}$$

During this operating mode, the power switches $S_1$, $S_2$, and $S_4$ are in OFF-state.

The voltage stress of these power switches can be given as follows:

$$V_{S1} = V_{C1} \tag{6}$$

$$V_{S2} = V_{C2} \tag{7}$$

***Mode* III:** As illustrated in Fig. 2(c), the series connection of $C_1$ and $C_3$ supply the power to the grid. By turning on $S_1$ and turning off $S_5$, voltage level 1.5 $V_{dc}$ is generated at the inverter output. The equation of this mode can be written as:

$$V_{out} = V_{C1} + V_{C3} \tag{8}$$

The voltage stress of the involved switches of this mode can be calculated as follows:

$$V_{S5} = V_{C1} \tag{9}$$

$$V_{S2} = V_{C4} \tag{10}$$

$$V_{S4} = V_{C3} + V_{C4} \tag{11}$$

***Mode* IV:** In Fig. 2(d), $C_3$ is disconnected, and $C_4$ is charging. Besides, grid power is provided by $C_2$ in this mode. According to Fig. 2(d), -0.5 $V_{dc}$ is provided at the output by turning on switch $S_4$. The related equations of this mode can be written as:

$$V_{out} = -V_{C2} \tag{12}$$

***Mode* V:** This operational mode of the proposed inverter is illustrated in Fig. 2(e). Considering this figure, the stored energy of the $C_4$ is discharged to the grid. Moreover, by turning off $S_1$ and turning on $S_5$ output voltage reaches to -$V_{dc}$.

***Mode* VI:** This operation mode of the proposed inverter is shown in Fig. 2(f). During this mode, the switches $S_2$ and $S_4$ are in on-state. By turning on the switch $S_2$, the capacitor $C_3$ is connected to the input source in series. Therefore, the capacitor $C_3$ is in charging mode and $C_4$ in discharging mode. Thus, a series connection of $C_2$ and $C_4$ supply the power to the grid. In this mode, the output voltage level can be obtained as:

$$V_{out} = -(V_{C2} + V_{C4}) \tag{14}$$

So, the output voltage of the inverter can be written as:

$$V_{out} = -V_{C4} \tag{13}$$

Also, during this operational mode, the switches $S_1$, $S_3$ and $S_5$ are in off-state; therefore, the voltage stress of switch $S_3$ can be calculated as follows:

$$V_{S3} = V_{C3} + V_{C4} \tag{15}$$

From the above-obtained equations, it can be understood that the maximum blocked voltage (MBV) of the switches and total standing voltage (TSV) of the proposed inverter can be written as:

$$MBV = 2V_{dc} \tag{16}$$

$$TSV = \sum_{i=1}^{5} MBV_{Si} = V_{dc} + V_{dc} + 2V_{dc} + 2V_{dc} + 0.5V_{dc} = 6.5V_{dc} \tag{17}$$

Besides, the duty cycle of the different operational modes of the proposed topology are calculated in (18) to (27). The positive half cycle of the output voltage waveform of the inverter and grid voltage with three operational zones (Zone 1 ~ Zone 3) of the inverter is depicted in Fig. 3. Regarding this figure, the control technique of the proposed topology can be provided. The maximum switching frequency of the inverter is $f_S$, also, the sampling frequency is $f_{SA}$. It should be mentioned that the sampling frequency is two times of the maximum switching frequency. By implementing the inductor volt-second balanced (IVSB) law to the inductor's voltage in a full operation period ($T_S$), the switching duty cycle of the three mentioned zones of the inverter are calculated in (18) to (27). It should be noted that, $V_{out}$ and $V_g$ are the output voltages of inverter and grid,

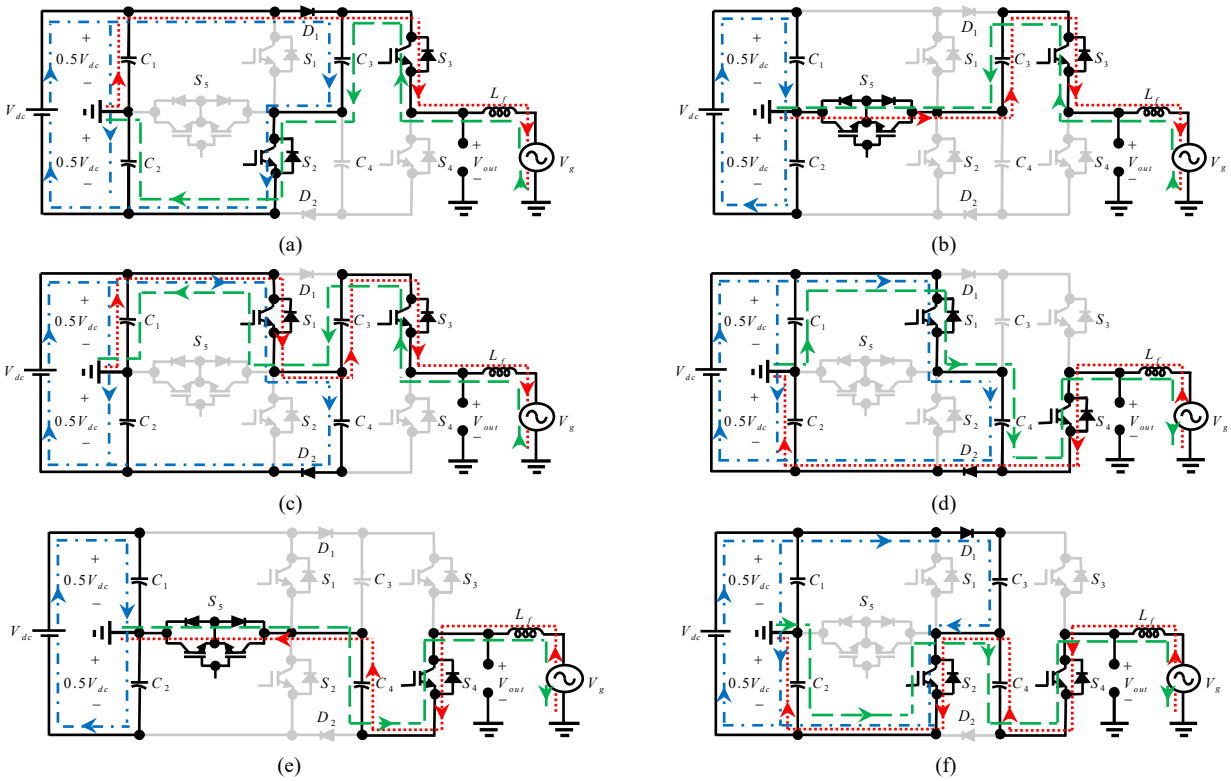



FIGURE 2. **The equivalent circuits of the presented converter in different operational modes: (a) Mode I, (b) Mode II, (c) Mode III, (d) Mode IV, (e) Mode V, and (f) Mode VI.**

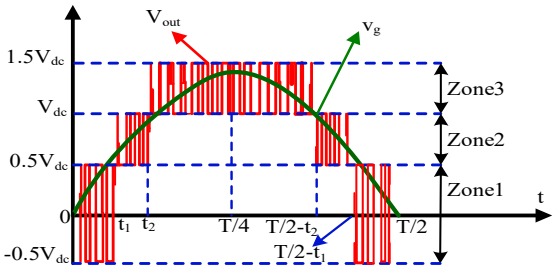



FIGURE 3. **The output voltage waveform of the inverter, grid voltage, and three operation zone of the proposed inverter.**

respectively. The equations for voltage and current of the grid can be written as (18) and (19).

$$v_g = V_{mg}\sin(\omega t) \tag{18}$$

$$i_g = I_{mg}\sin(\omega t) \tag{19}$$

**Zone 1:**

Considering Fig. 3, the inverter's output voltage is between -0.5 $V_{dc}$ and 0.5 $V_{dc}$ during this zone. Therefore, by applying the IVSB principle for the voltage across the output inductor during zone 1 for the switching period, the switching duty cycle of the inverter ($d_1$) can be obtained as (20)-(22).

$$\int_0^{d_1T_S}\left(0.5V_{dc}-v_g\right)dt+\int_{d_1T_S}^{T_S}\left(-0.5V_{dc}-v_g\right)dt=0 \tag{20}$$

$$d_1(t)=0.5+\frac{v_g}{V_{dc}} \tag{21}$$

By substituting (18) in (21), the duty cycle of zone 1 can be written as:

$$d_1(t)=0.5+\frac{V_{mg}}{V_{dc}}\cdot\sin(\omega t) \quad ; \quad 0\le t<t_1 \tag{22}$$

The average value of $d_1(t)$ can be calculated as follows:

$$D_{1,ave}=\frac{1}{\omega t_1}\int_0^{\omega t_1}\left(0.5+\frac{V_{mg}}{V_{dc}}.\sin(\omega t)\right)d\omega t=0.5+\frac{V_{mg}}{\omega t_1.V_{dc}}.\left(1-\cos(\omega t_1)\right) \tag{23}$$

**Zone 2:**

With respect to Fig. 3, it can be seen that during zone 2 the output voltage of inverter is between 0.5 $V_{dc}$ and $V_{dc}$. By applying the IVSB rule for the voltage across of the inductor filter during zone 2 for the switching period, the switching duty cycle of the inverter ($d_2$) can be calculated as (24)-(26).

$$\int_0^{d_2T_S}\left(V_{dc}-v_g\right)dt+\int_{d_2T_S}^{T_S}\left(0.5V_{dc}-v_g\right)dt=0 \quad ; \quad t_1\le t<t_2 \tag{24}$$

$$d_2(t)=\frac{2v_g}{V_{dc}}-1=\left(\frac{2V_{mg}}{V_{dc}}\sin(\omega t)-1\right) \quad ; \quad t_1\le t<t_2 \tag{25}$$

Considering (22), the equation (26) can be rewritten as:

$$d_2(t)=2d_1(t)-2 \quad ; \quad t_1\le t<t_2 \tag{26}$$

The average value of $d_2(t)$ can be calculated as follows:

$$D_{2,ave} = \frac{1}{\omega t_2 - \omega t_1}\int_{\omega t1}^{\omega t2}\left(\frac{2V_{mg}}{V_{dc}}\sin(\omega t) - 1\right)d\omega t = \frac{1}{\omega t_2 - \omega t_1}\left(\frac{2V_{mg}}{V_{dc}}\left(\cos(\omega t_1) - \cos(\omega t_2) + \omega t_1 - \omega t_2\right)\right) \quad (27)$$

**Zone 3:**

As shown in Fig. 3, in zone 3 the inverter's output voltage is between $V_{dc}$ and 1.5 $V_{dc}$. Therefore, by using IVSB law for the voltage across of the inductor filter during zone 3 for the switching period, the switching duty cycle of the inverter ($d_3$) can be written as (28)-(29).

$$\int_0^{d_3T_S}\left(1.5V_{dc} - v_g\right)dt + \int_{d_3T_S}^{T_S}\left(V_{dc} - v_g\right)dt = 0 \;;\; t_2 \le t < \frac{T}{2} - t_2 \quad (28)$$

$$d_3(t) = 2\left(\frac{v_g}{V_{dc}} - 1\right) = \frac{2V_{mg}}{V_{dc}}\cdot\sin(\omega t) - 2 \;;\; t_2 \le t < \frac{T}{2} - t_2 \quad (29)$$

The average value of $d_3(t)$ can be calculated as follows:

$$D_{3,ave} = \frac{1}{\pi - 2\omega t_2}\int_{\omega t_2}^{\pi - \omega t_2}\left(\frac{2V_{mg}}{V_{dc}}.\sin(\omega t) - 2\right)d\omega t = \frac{1}{\pi - 2\omega t_2}\left(\frac{4V_{mg}}{V_{dc}}.\cos(\omega t_2) - 2(\pi - 2\omega t_2)\right) \quad (30)$$

Considering (25), the equation (29) could be written as:

$$d_3(t) = 2d_2(t) - 3 \quad (30)$$

The equations of $t_1$ and $t_2$ can be obtained as:

$$t_1 = \frac{1}{\omega}\sin^{-1}\left(\frac{0.5V_{dc}}{V_{mg}}\right) \quad (31)$$

$$t_2 = \frac{1}{\omega}\sin^{-1}\left(\frac{V_{dc}}{V_{mg}}\right) \quad (32)$$

## IV. ANALYSIS OF THE PROPOSED INVERTER

### A. LEAKAGE CURRENT AND THE VOLTAGE ACROSS THE STRAY CAPACITOR

According to Fig. 1 and 2, the voltage across the stray capacitors is equal to the voltage across $C_1$ and $C_2$. Therefore, the voltage across stray capacitors is calculated in the following:

$$V_{C1} = 0.5V_{dc} - \Delta V_{C1}(t) \quad (39)$$

$$V_{C2} = 0.5V_{dc} - \Delta V_{C2}(t) \quad (40)$$

$$\Delta V_{C1}(t) = -\Delta V_{C2}(t) = \frac{I_{mg}\cos(\omega t)}{\omega(C_1 + C_2)} \quad (41)$$

Where $I_{mg}$ is the maximum value of the grid current waveform. It is to be noted that $\omega = 2\pi f$ in equation (41). According to equation (33), the voltage across the capacitor is combined of ac (ripple) and dc component. Since ($|\Delta V_{C1}| = |\Delta V_{C2}| = |\Delta V_C|$), calculation of the leakage current as given in (42).

$$I_{Leakage} = (C_{PV1} + C_{PV2})\frac{d(\Delta V_C)}{dt} \quad (42)$$

By putting equation (41) into (42), the expression of the leakage current can be written as:

$$I_{Leakage} = \frac{(C_{PV1} + C_{PV2})}{(C_1 + C_2)}I_{mg}\sin(\omega t) \quad (43)$$

As given in equation (43), the leakage current is not affected by the dc component but is affected only by the ac component. Considering that $C_{pv1}$ and $C_{pv2}$ are smaller than $C_1$ and $C_2$, and because the ac element fluctuates with grid frequency, the leakage current in the proposed grid-tied inverter is negligible.

### B. DESIGN OF PASSIVE UTILIZED CIRCUIT COMPONENTS

In this section the capacitance of the capacitors and output inductor filter is calculated. The capacitors $C_1$ and $C_2$ regarding to equations (39)-(31) and considering maximum voltage ripple across $C_1$ and $C_2$ in the first leg ($|\Delta V_{C1}| = |\Delta V_{C2}|$), are calculated as:

$$C_1 = C_2 = \frac{I_{mg}}{2\omega\Delta V_{C1}} \quad (44)$$

The capacitance values of capacitors ($C_3$ and $C_4$) in the proposed inverter are calculated based on each capacitor's longest discharging cycle (LDC). The LDC happens during the positive and negative half-cycles for utilized capacitors $C_3$ and $C_4$, respectively. The peak discharging value of each capacitor during the mentioned LDC can be calculated as:

$$\begin{cases} I_C = \dfrac{dQ_C}{dt} \\ Q_C = \int I_C dt \end{cases} \quad (45)$$

It should be noted that the output voltage waveform has only odd order of harmonics. So that, the LDC for capacitors ($C_3$ and $C_4$) will be the same. Regarding Fig. 3, if $t_2 \le t \le \frac{T}{2} - t_2$ the current passing through the capacitor $C_3$ will be equal to injected grid current ($i_g(t)$). Therefore, the equation (45) can be written as:

$$\begin{cases} t_2 \le t < \dfrac{T}{2} - t_2 \\ i_{C3} = i_g(t) = I_{mg}\sin(\omega t) \end{cases} \Rightarrow Q_{C3} = \int_{t_2}^{\frac{T}{2}-t_2} i_g(t)dt \quad (46)$$

The value for capacitor $C_3$ can be obtained as follow:

$$\Delta Q_{C3} = Q_{C3} \times \Delta V \quad (47)$$

$$C_3 = \frac{\Delta Q_{C3}}{\Delta V} = \frac{Q_{C3}}{\Delta V} \quad (48)$$

Where, $\Delta V$ is the maximum permittable value of the capacitor $C_3$ voltage ripple, and it can be defined as:

$$\Delta V = N \times V_{dc} \quad (49)$$

With respect to equations (47) and (49), the value of capacitor $C_3$ can be written as:

$$C_3 = \frac{Q_{C3}}{N \times V_{dc}} \quad (50)$$

Also, the capacitance of capacitor $C_4$ is calculated in the same way as capacitor $C_3$.

The current of the output filter inductor can be calculated as follows:

$$i_{Lf}(t)=\frac{1}{L_f}\int_0^t V_{Lf}\,dt+i_{Lf}(0) \quad ; \quad t_2\le t<\frac{T}{2}-t_2 \tag{51}$$

Also, the current ripple of the inductor can be calculated as:

$$\Delta I_{Lf}=i_{Lf}(t=d_3T_S)-i_{Lf}(0)=\frac{\left(1.5V_{dc}-v_g\right)d_3}{L_f f_S} \;;t_2\le t<\frac{T}{2}-t_2 \tag{52}$$

Therefore, using (44), the final value of $L_f$ can be calculated as:

$$L_f=\frac{1}{\Delta I_{Lf}f_S}\left[5V_{mg}\sin(\omega t)-\frac{2V_{mg}^2}{V_{dc}}\sin^2(\omega t)-3V_{dc}\right] \tag{53}$$

The value of $L_f$ for maximum value of the inductor current ripple could be calculated as:

$$L_f=\frac{1}{\Delta I_{Lf,\max}f_S}\left[5V_{mg}-\frac{2V_{mg}^2}{V_{dc}}-3V_{dc}\right] \tag{54}$$

## V. CONTROL SYSTEM OF THE PROPOSED INVERTER

A peak current controller method is used to trigger the gate of power switches to control both active and reactive powers. The control system block diagram of proposed grid-tied inverter is illustrated in Fig. 4. A phase-locked loop (PLL) as the synchronous block is utilized to find the local grid's proper amplitude and phase, as shown in Fig. 4. In the suggested control system, a filter-based phase-locked loop system like second-order generalized integrator (SOGI) [46] or enhanced phase-locked loop (E-PLL) [29] is suggested. With respect to Fig. 4, unit $\frac{2\sqrt{P_{ref}^{\ 2}+Q_{ref}^{\ 2}}}{V_{mg}}$ generates the peak value of the injected current into the grid ($I_{mg}$), which depends on the reference value of active and reactive power injected into the grid. Also, by block $\tan^{-1}\left(\frac{Q_{ref}}{P_{ref}}\right)$, the value of the phase angle of the injected current to the grid is produced. The PLL unit generates the angular velocity of grid. Also, by multiplying the peak value of injected current to the grid in the unit $\sin(\omega t-\varphi)$, the reference value of injected current to the grid ($i_{ref}$) is generated. Finally, the reference value of injected current to the grid, the injected current to the grid, and the grid voltage are sent to the current controller block, which generates the required PWM gate pulses of the power switches of the proposed inverter. Note that, in the control system the required amplitude and phase angle of the reference current ($i_{ref}$) are calculated according to the reactive and active power values. The measured instantaneous slope of the inductor $L_f$ current, named L-type filter, is compared with the current waveform reference. In the current controller unit, the switching pattern of the implemented power switches has been achieved by comparing the reference current with the measured grid current. The reference and measured current waveforms with the generated gate pulses have been illustrated in Fig. 5. Considering this figure, the

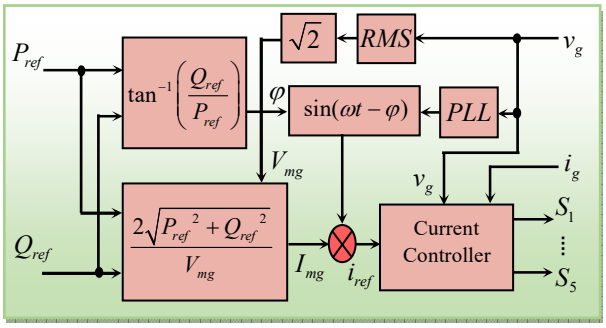



FIGURE 4. **Control system of the suggested grid-connected six-level inverter.**

TABLE II
APPLIED PCC STRATEGY AND SWITCHING GATE PULSES PATTERN

| | Active power mode | | | | Reactive power mode | | | |
|---|---|---|---|---|---|---|---|---|
| | Positive half cycle | | Negative half cycle | | Positive half cycle | | Negative half cycle | |
| | $V_g>0$ & $i_{ref}>0$ | | $V_g<0$ & $i_{ref}<0$ | | $V_g>0$ & $i_{ref}<0$ | | $V_g<0$ & $i_{ref}>0$ | |
| | $i_g<i_{ref}$ | $i_g>i_{ref}$ | $i_g<i_{ref}$ | $i_g>i_{ref}$ | $i_g<i_{ref}$ | $i_g>i_{ref}$ | $i_g<i_{ref}$ | $i_g>i_{ref}$ |
| Zone 1: -0.5 $V_{dc}$< $V_g$ <0.5 $V_{dc}$ | $S_2$, $S_3$ | $S_1$, $S_4$ | $S_2$, $S_3$ | $S_1$, $S_4$ | $S_2$, $S_3$ | $S_1$, $S_4$ | $S_2$, $S_3$ | $S_1$, $S_4$ |
| Zone 2: 0.5 $V_{dc}$< $V_g$ < $V_{dc}$ | $S_3$, $S_5$ | $S_2$, $S_3$ | - | - | $S_3$, $S_5$ | $S_2$, $S_3$ | - | - |
| Zone 3: $V_{dc}$< $V_g$ <1.5 $V_{dc}$ | $S_1$, $S_3$ | $S_3$, $S_5$ | - | - | $S_1$, $S_3$ | $S_3$, $S_5$ | - | - |
| Zone 4: -0.5 $V_{dc}$< $V_g$ < -$V_{dc}$ | - | - | $S_1$, $S_4$ | $S_4$, $S_5$ | - | - | $S_1$, $S_4$ | $S_4$, $S_5$ |
| Zone 5: -$V_{dc}$< $V_g$ <-1.5 $V_{dc}$ | - | - | $S_4$, $S_5$ | $S_2$, $S_4$ | - | - | $S_4$, $S_5$ | $S_2$, $S_4$ |

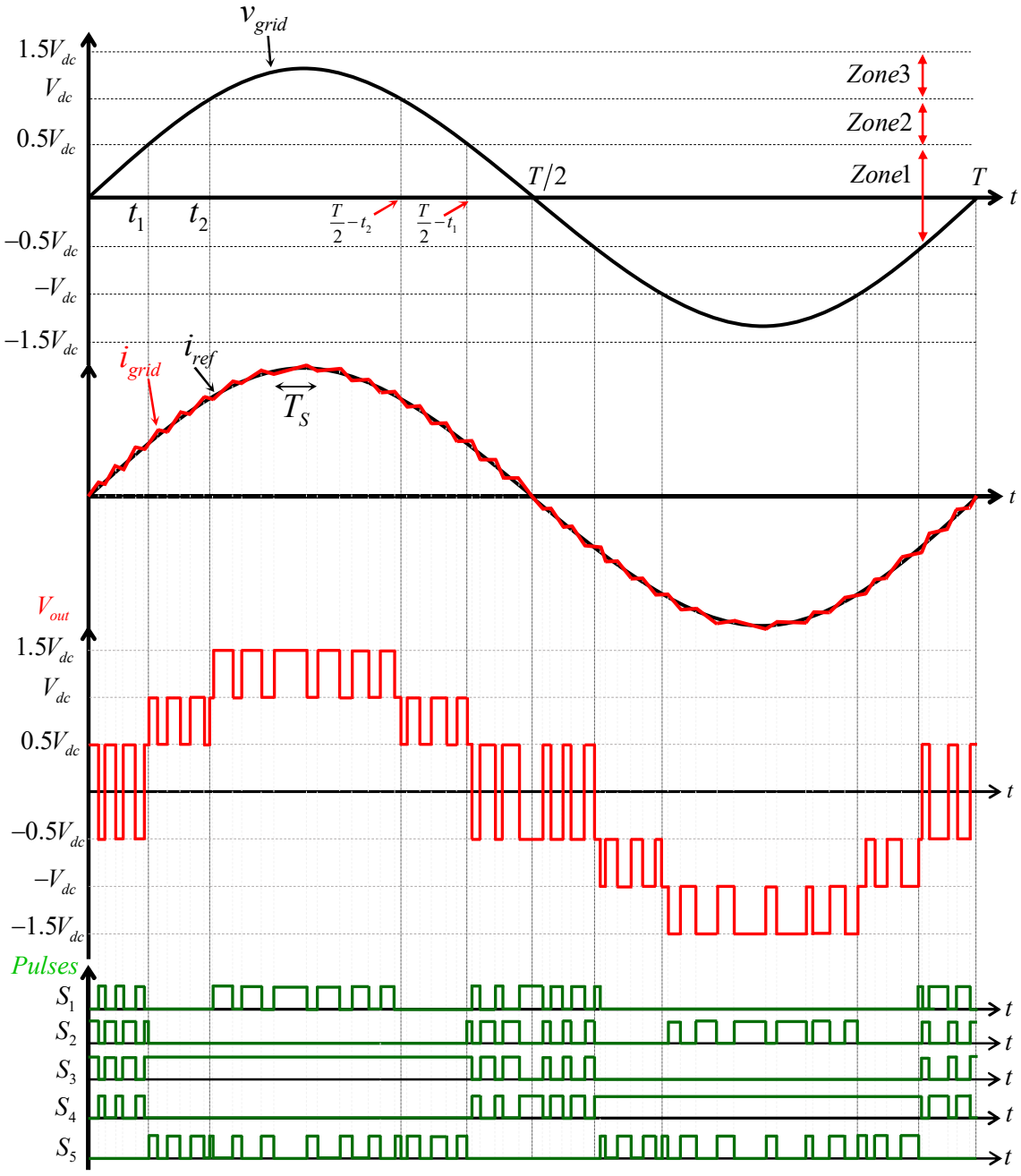



FIGURE 5. **The reference and measured current waveforms with the generated gate pulses.**

performance of the proposed inverter is affected by the polarity of the instantaneous value of the grid voltage ($v_g$) and instantaneous value of the injected grid current ($i_g$). In addition, Fig. 6 shows the logic-based circuit diagram of applied peak current controller for generating the gate pulses of switches. Also, Table II shows the applied peak current controller operation pattern of switching pulses. In order to investigate the accurate performance of the applied control system, a number of simulation results have been performed in MATLAB/Simulink software and are shown in Fig. 7 and Fig. 8. Fig. 7(a) and Fig. 7(b) show the output voltage along with the injected current to the grid under applied current step change at unity PF and lag PF, respectively. Based on these figures, as the amplitude of injected current to the grid increases from 2.5 *A* to 5 *A* the injected power increases from 380 W to 770 W in the Fig. 7(a) and 380 *VA* to 770 *VA* in the Fig. 7(b).

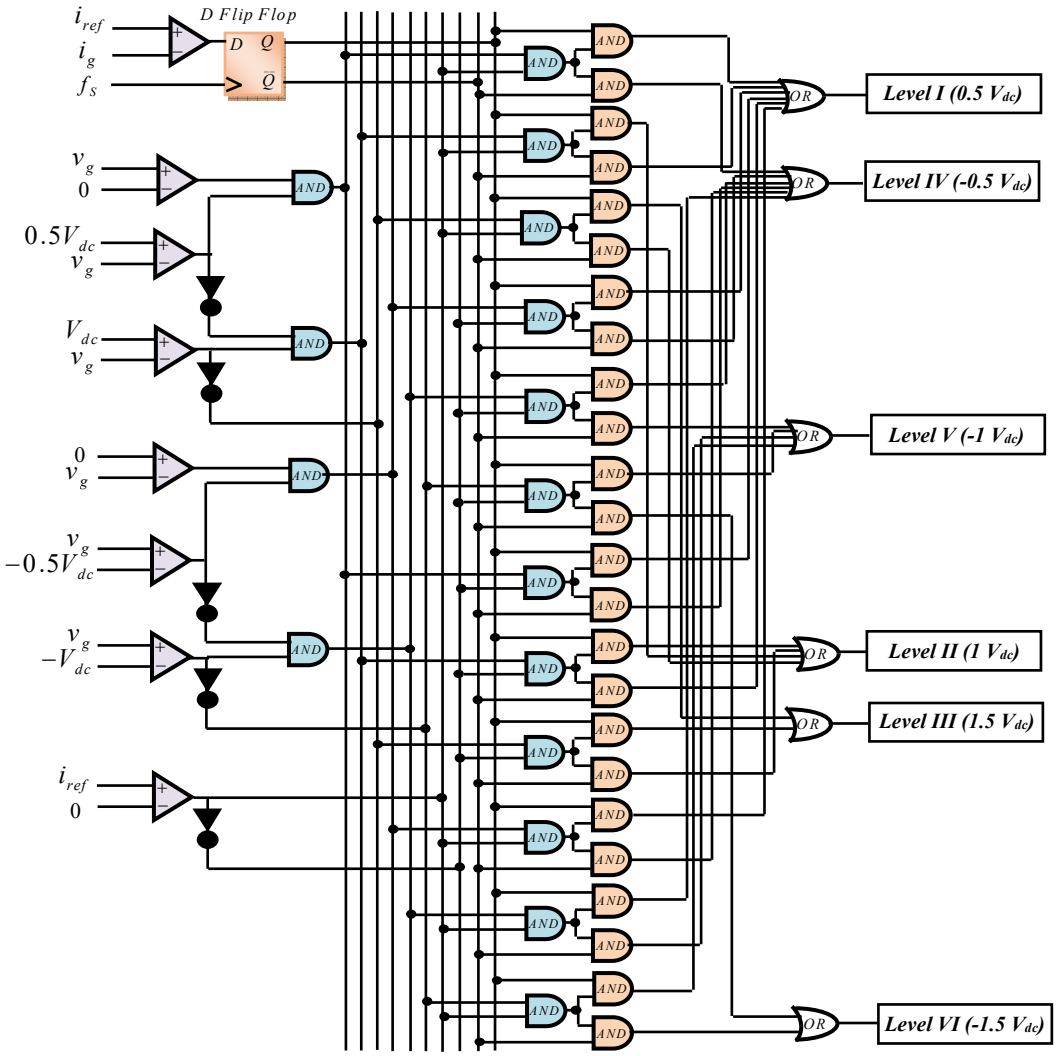



FIGURE 6. **Logic-based diagram for the switching pulse generation.**

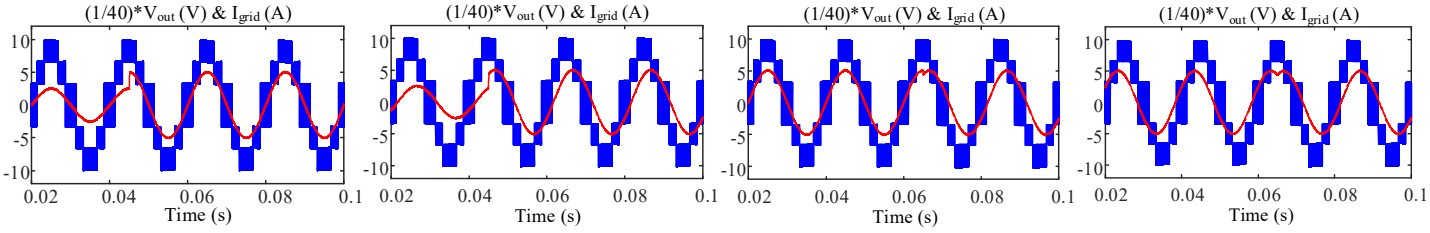



FIGURE 7. **Simulation results of output voltage and injected grid current under step changes; (a) current step change under unity PF, (b) current step change under lag PF, (c) PF step change (unity to lag), (d) PF step change (lead to lag).**

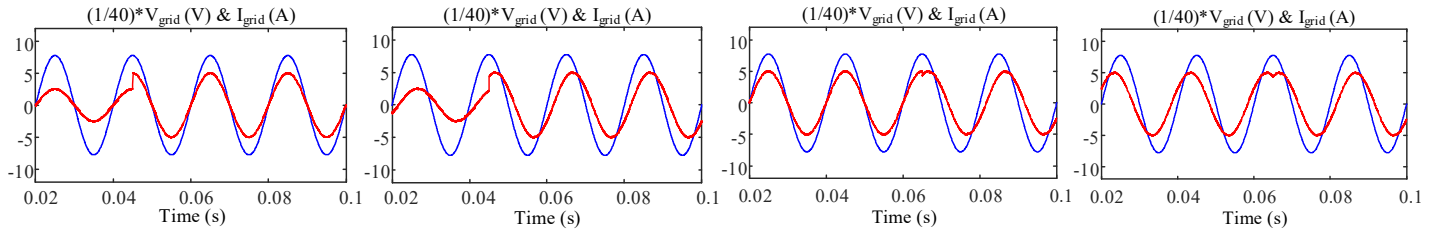



FIGURE 8. **Simulation results of grid voltage and injected grid current under step changes; (a) current step change under unity PF, (b) current step change under lag PF, (c) PF step change (unity to lag), (d) PF step change (lead to lag.).**

Fig. 7(c) and Fig. 7(d) illustrate the output voltage and injected grid current under PF changing such as unity PF to lag PF and lead PF to lag PF, respectively. Considering these figures, the amplitude of injected current to the grid is constant. So that, the amplitude of the injected power to the grid is constant. The simulation results of the grid voltage and injected current to the grid waveforms are presented in Fig. 8. Figs. 8(a) and (b) show that by applying the step change in the amplitude of the injected current to the grid (from 2.5 *A* to 5 *A*) the injected power to the grid can follow this step change under unity PF and lag PF. Furthermore, Fig. 8(c) and Fig. 8(d) indicate the grid voltage and injected grid current under PF changing such as unity PF to lag PF and lead PF to lag PF, respectively. With respect to Fig. 7 and Fig. 8, it can be concluded that the applied control system can performed good under different step changes such as amplitude step change and PF changing.

## VI. POWER LOSS ANALYSIS OF THE PROPOSED INVERTER

Here, switching and conduction power losses of the utilized power switches are calculated by analyzing their current stresses. To calculate the power losses of the proposed inverter, the injected current to the grid can be considered as Fig. 9(a) and can be written as follows:

$$i_g = I_{mg}.\sin(\omega t) \tag{55}$$

In order to calculate the RMS current of grid in each of the operating intervals, Fig. 9(b) is considered. Based on this figure, the values of $I_{o1}$, $I_{o2}$ and $I_{o3}$ can be calculated as follows:

$$I_{o1} = \left[\frac{1}{\omega t_1}\int_0^{\omega t_1} I^2{}_{mg}\sin^2(\omega t).d\omega t\right]^{1/2} = I_{mg}\sqrt{\frac{1}{2}-\frac{1}{4\omega t_1}\sin(2\omega t_1)} \tag{56}$$

$$I_{o2} = \left(\frac{1}{\omega t_2-\omega t_1}\int_0^{\omega t_1} \mathrm{I}^2{}_{mg}.\sin^2(\omega t).d\omega t\right)^{1/2}$$
$$= \mathrm{I}_{mg}.\left(\frac{1}{\omega t_2-\omega t_1}\left(\frac{1}{2}\omega t_2-\frac{1}{4}\sin(2\omega t_2)-\frac{1}{2}\omega t_1+\frac{1}{4}\sin(2\omega t_2)\right)\right)^{1/2} \tag{57}$$

The times $t_1$ and $t_2$ can be calculated from (31) and (32). The number of switching times from moment zero to $\pi/2$ can be calculated as follows:

$$I_{o3} = \left[\frac{1}{\pi-2\omega t_2}\int_{\omega t_2}^{\pi-\omega t_2} I^2{}_{mg}\sin^2(\omega t)d\omega t\right]^{1/2}$$
$$= I_{mg}\sqrt{\frac{1}{\pi-2\omega t_2}\left(\frac{\pi}{2}-\omega t_2+\frac{1}{2}\sin(2\omega t_2)\right)} \tag{58}$$

$$\begin{cases} N_{SW1} = \dfrac{t_1}{T_s} & ;\quad 0 \le \omega t < \omega t_1 \\ N_{SW2} = \dfrac{t_2-t_1}{T_s} & ;\quad \omega t_1 \le \omega t < \omega t_2 \\ N_{SW3} = \dfrac{500\mu s - t_2}{T_s} & ;\quad \omega t_2 \le \omega t < \dfrac{\pi}{2} \end{cases} \tag{59}$$

Where, $T_s$ is the switching period time and can be written as:

$$T_s = \frac{1}{f_s} \tag{60}$$

Where, $f_s$ is the switching frequency of the proposed inverter.

Due to the fact that each switch has different losses in different operating intervals, so the power losses of each switch in different intervals are calculated separately.

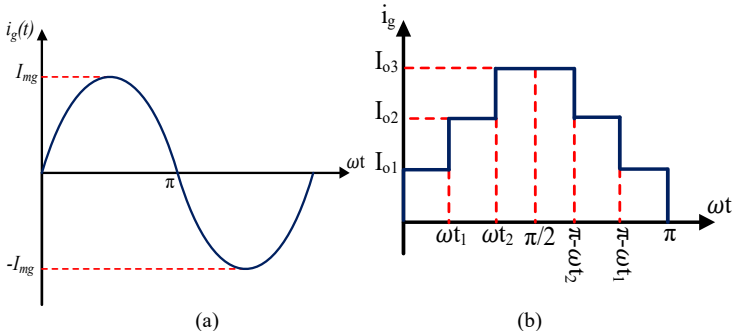



FIGURE 9. **(a) Injected current to the grid waveform (b) modelled of grid current waveform.**

*Operating interval* $(0, \omega t_1)$ *:*

The current equation of switch $S_3$ during interval $(0, \omega t_1)$ in the positive half cycle is calculated as follows:

$$i_{S3,(0,\omega t_1)} = \begin{cases} I_{o1} & ;\quad 0 \le t < d_1 T_s \\ 0 & ;\quad d_1 T_s \le t < T_s \end{cases} \tag{61}$$

This operating interval happens twice during a full cycle of the grid current. Therefore, the RMS current value of switch $S_3$ can be calculated as follows:

$$I_{S_3,rms,(0,\omega t_1)} = \left[\frac{2\omega t_1}{2\pi}.\frac{1}{T_s}\int_0^{d_1 T_s} I^2{}_{o1}.dt\right]^{1/2} = I_{o1}.\sqrt{\frac{d_1.\omega t_1}{\pi}} \tag{62}$$

The switching loss and conduction loss of the switch $S_3$ during interval $(0, \omega t_1)$ can be calculated as:

$$P_{SW,S_3,(0,\omega t_1)} = \frac{1}{6}V_{S_3}.I_{S_3}.\left(t_{on}+t_{off}\right).\left(2\times N_{SW_1}\right)$$
$$= \frac{1}{6}\times 2V_{dc}.I_{o1}.\left(t_{on}+t_{off}\right).\left(2.N_{SW_1}\right) \tag{63}$$

$$P_{Con,S_3,(0,\omega t1)} = r_{DS_3}I^2_{S_3,rms,(0,\omega t1)} = \frac{r_{DS_3}I^2{}_{o1}d_1\omega t_1}{\pi} \tag{64}$$

*Operating interval* $(\omega t_1, \omega t_2)$ *:*

In this interval $(\omega t_1, \omega t_2)$, switch $S_3$ is in on-state continuously. So that, the switching losses of this switch is zero, and it has only conduction losses. The current equation of switch $S_3$ in this interval can be calculated as follows:

$$i_{S_3,(\omega t_1,\omega t_2)} = \begin{cases} I_{o2} & ;\quad 0 \le t < d_2 T_s \\ I_{o2} & ;\quad d_2 T_s \le t < d_2 \end{cases} \tag{65}$$

The RMS current value of switch $S_3$ during interval $(\omega t_1, \omega t_2)$ can be calculated as follows:

$$I_{S_3,rms(\omega t_1,\omega t_2)}=\left[\frac{2(\omega t_2-\omega t_1)}{2\pi}\cdot\frac{1}{T_s}\int_0^{Ts} I^2_{o2}.dt\right]^{1/2}=I_{o2}\cdot\sqrt{\frac{\omega t_2-\omega t_1}{\pi}} \quad (66)$$

The conduction losses of switch $S_3$ can be calculated as:

$$P_{Con,S_3,(\omega t_1,\omega t_2)}=\frac{r_{DS3}.I^2_{o2}.(\omega t_2-\omega t_1)}{\pi} \quad (67)$$

*Operating interval* $(\omega t_2,\pi/2)$

In this interval, the switch $S_3$ is in on-state continuously. So, switching losses is zero, and it has only conduction loss.

The current equation of switch $S_3$ in this interval can be calculated as follows:

$$i_{S_3,(\omega t_2,\pi/2)}=\begin{cases}I_{o3} & ;\quad 0\le t<d_3T_s\\ I_{o3} & ;\quad d_3T_s\le t<d_3\end{cases} \quad (68)$$

The RMS current value of switch $S_3$ during interval $(\omega t_2,\pi/2)$ can be calculated as follows:

$$I_{S_3,rms(\omega t_2,\pi/2)}=\left[\frac{2(\pi/2-\omega t_2)}{2\pi}\frac{1}{T_s}\int_0^{Ts} I^2_{o3}dt\right]^{1/2}=I_{o2}\sqrt{\frac{\pi/2-\omega t_2}{\pi}} \quad (69)$$

The conduction losses of switch $S_3$ during this interval can be calculated as:

$$P_{Con,S_3,(\omega t_2,\pi/2)}=\frac{r_{DS3}I^2_{o3}(\pi/2-\omega t_2)}{\pi} \quad (70)$$

*Operating interval* $(\pi,\pi+\omega t_1)$ :

In the negative half cycle of the grid voltage, the switch $S_3$ is in on-state only during the interval $(\pi,\pi+\omega t_1)$. In this interval, the current equation of switch $S_3$ can be calculated as:

$$i_{S3,(\pi,\pi+\omega t_1)}=\begin{cases}0 & ;\quad 0\le t<d_1T_s\\ I_{o1} & ;\quad d_1T_s\le t<T_s\end{cases} \quad (71)$$

The RMS current value of switch $S_3$ during interval $(\pi,\pi+\omega t_1)$ can be calculated as follows:

$$I_{S_3,rms(\pi,\pi+\omega t_1)}=\left[\frac{2\omega t_1}{2\pi}.\frac{1}{T_s}\int_{d_1T_s}^{Ts}(-I_{o1})^2.dt\right]^{1/2}=I_{o1}.\sqrt{\frac{\omega t_1.(1-d_1)}{\pi}} \quad (72)$$

The switching and conduction power losses of the switch $S_3$ can be calculated as follows:

$$P_{SW,S_3,(\pi,\pi+\omega t_1)}=\frac{1}{6}\times 2V_{dc}\times I_{o1}\times\left(t_{on}+t_{off}\right)\times\left(2N_{SW1}\right) \quad (73)$$

$$P_{Con,S_3,(\pi,\pi+\omega t_1)}=\frac{r_{DS}.I^2_{o1}.\omega t_1\left(1-d_1\right)}{\pi} \quad (74)$$

The total power loss of the switch $S_3$ during a full period cycle of grid voltage waveform can be obtained as:

$$P_{S_3}=P_{SW,S_3,(0,\omega t_1)}+P_{SW,S_3,(\pi,\pi+\omega t_1)}+P_{Con,S_3,(0,\omega t_1)}+P_{Con,S_3,(\omega t_1,\omega t_2)}+P_{Con,S_3,(\omega t_2,\pi/2)}+P_{Con,S_3,(\pi,\pi+\omega t_1)} \quad (75)$$

Also, the losses of other switches and diodes are calculated in the same way. The detailed values of switching and conduction losses of used semiconductors in the proposed topology under different output power (100 *W*~1900 *W*) are presented in Table III. Fig. 10(a) illustrates the pie chart of the semiconductors' power losses and capacitor's power losses distribution. Also, the simulation, calculation and experimental efficiency curves of the proposed inverter versus output power can be illustrated in Fig. 10(b). With respect to this figure, it can be seen that at output powers 500 *W* and 800 *W*, the maximum values of experimental efficiency are around 97.5% and 97%, respectively.

## VII. COMPARISON

An extensive comparison between the suggested inverter and other previous grid-connected inverters to demonstrate the advantages of the proposed grid-tied structures is shown in Table IV. As seen, these topologies are compared with different aspects such as the number of passive and active elements, input voltage, the value of leakage current, number of on-state switches, number of generated voltage levels, reactive power support capability, the value of the output filter elements, reported efficiency and voltage boosting ability. As evident from Table V, all conventional topologies, except [3] and [29], lacks voltage boosting ability and require additional power conversion stages to boost the output voltage. Regarding the points mentioned above, the input of the active neutral point clamp inverter requires more than 750 *V* dc voltage, while the other topologies request 400 *V* dc voltage. Furthermore, all the mentioned grid-connected inverters

TABLE III
DETAILS OF EFFICIENCY AND POWER LOSSES OF THE PROPOSED INVERTER IN THEORY

| $P_{out}(W)$ | $P_{S1}$ | $P_{S2}$ | $P_{S3}$ | $P_{S4}$ | $P_{S5}$ | $P_{D1}$ | $P_{D2}$ | $P_{C1}+P_{C2}$ | $P_{C3}+P_{C4}$ | Total losses | Efficiency % |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 | 0.0282 | 0.0282 | 0.0074 | 0.0074 | 0.0197 | 0.1511 | 0.1511 | 0.012 | 0.1304 | 0.5355 | 99.46 |
| 300 | 0.2497 | 0.2497 | 0.0655 | 0.0655 | 0.1760 | 0.5968 | 0.5968 | 0112 | 1.006 | 3.118 | 98.97 |
| 500 | 0.6917 | 0.6917 | 0.1815 | 0.1815 | 0.4878 | 1.23 | 1.23 | 0.313 | 1.935 | 6.948 | 98.63 |
| 700 | 1.35 | 1.35 | 0.35 | 0.35 | 0.95 | 2.06 | 2.06 | 0.611 | 2.98 | 12.081 | 98.3 |
| 900 | 2.24 | 2.24 | 0.587 | 0.587 | 1.57 | 3.08 | 3.08 | 1.012 | 4.26 | 18.652 | 97.96 |
| 1100 | 3.34 | 3.34 | 0.87 | 0.87 | 2.35 | 4.29 | 4.29 | 1.513 | 5.73 | 26.613 | 97.63 |
| 1300 | 4.66 | 4.66 | 1.22 | 1.22 | 3.29 | 5.69 | 5.69 | 2.112 | 7.05 | 35.612 | 97.33 |
| 1500 | 6.21 | 6.21 | 1.63 | 1.63 | 4.38 | 7.28 | 7.28 | 2.814 | 8.2 | 45.634 | 97.04 |
| 1700 | 7.97 | 7.97 | 2.09 | 2.09 | 5.62 | 9.06 | 9.06 | 3.613 | 9.65 | 57.153 | 96.74 |
| 1900 | 9.95 | 9.95 | 2.61 | 2.61 | 7.03 | 11.04 | 11.04 | 4.512 | 11.25 | 70.012 | 96.44 |

**Switches:** SPW47N60C3, **Diodes:** RURP3060, $V_{dc}$=267 *V*, $V_{grid}$= 220 *Vrms*, $f_S$= 20*kHz*, $r_{ESRC1}=r_{ESRC2}=0.121\Omega$, $r_{ESRC3}=r_{ESRC4}=0.116\Omega$.

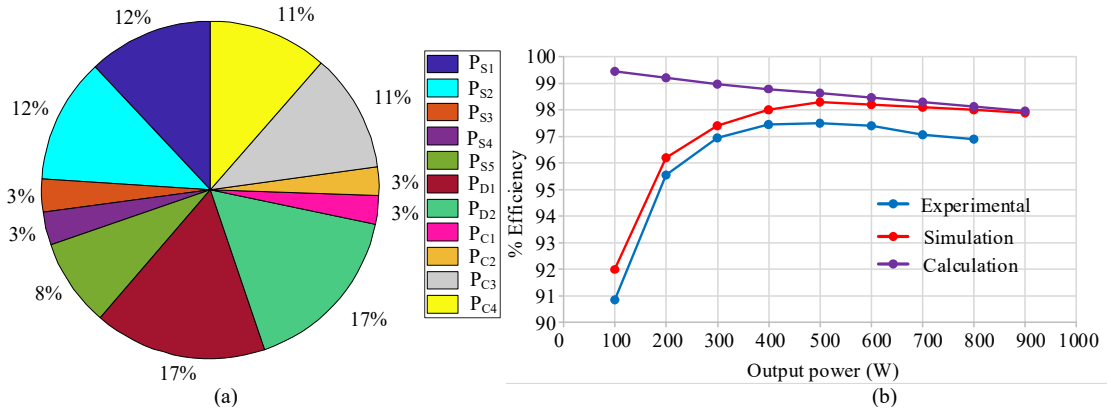



FIGURE 10. **(a) Pie chart of the semiconductors' and capacitors' power losses distribution, (b) The simulation, calculation and experimental efficiency curves of the proposed inverter versus output power.**

TABLE IV
COMPARISON OF THE PROPOSED CONVERTER WITH OTHER PRESENTED CONVERTERS

| Topology | Number of | | | | $V_{in}$ (V) | Output Filter | | | Leakage current | Number of ON-state Switches | Number of voltage levels | Efficiency (%) | Voltage boosting |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | *S* | *D* | *C* | *L* | | $L_{f1}$ | $L_{f2}$ | $C_f$ | | | | | |
| OH5 [17] | 6 | 0 | 2 | 0 | 400 | 4 mH | 4 mH | 6.6 uF | 44 mA | 3 | 3 | 97.2%@0.1 kW | No |
| H6 [18, 19] | 6 | 2 | 2 | 0 | 400 | 3 mH | 3 mH | 0.47 uF | 45 mA | 3 | 3 | 97.4%@1 kW | No |
| MH6 [47] | 7 | 0 | 2 | 0 | 400 | 3 mH | 3 mH | 6 uF | 9 mA | 3 | 3 | 92.18% | No |
| Active NPC [48] | 6 | 0 | 2 | 0 | 800 | NA | NA | NA | Reduced (NA) | 2 | 3 | 97.34%@10 kW | No |
| Common ground type [49] | 2 | 0 | 2 | 2 | 400 | 1 mH | 1 mH | 2.2 uF | About Zero | 2 | 2 | 96.0%@0.2 kW | No |
| HB-ZVR | 5 | 5 | 2 | - | 400 | 1.8 mH | 1.8 mH | 2 uF | 27 mA | 2 | 3 | 94.88%@2.8 kW | No |
| [29] | 6 | 1 | 3 | 0 | 200 | 3 mH | - | - | Zero | 2 or 3 | 3 | 98.1@0.51 kW | Yes |
| [3] | 6 | 2 | 3 | 0 | 200 | 3 mH | - | - | Zero | 2 or 3 | 5 | 98.1%@0.51 kW | Yes |
| [50] | 7 | 2 | 2 | 0 | | 2.9 mH | - | - | About zero | 2 or 3 | 5 | 99.02@0.62 kW | Yes |
| [51] | 6 | 3 | 3 | 0 | 200 | 3.2 mH | - | - | About zero | 3 | 3 | 97.9@0.5 kW | Yes |
| [52] | 8 | - | 3 | 2 | 200 | 2.3 mH | - | - | Zero | 4 or 5 | 5 | 98.3%@0.6 kW | Yes |
| [32] | 6 | 1 | 3 | 0 | 100 | 2.3 mH | - | - | Zero | 2 or 3 | 5 | 98.1%@0.6 kW | Yes |
| [53] | 7 | 2 | 1 | 0 | 100 | 3 mH | - | - | Zero | 3 | 5 | 98.1%@0.5 kW | Yes |
| [5] | 9 | 0 | 2 | 0 | 200 | 0.5 mH | - | 4 uF | Zero | 5 | 5 | 98.5 % @0.9 kW | Yes |
| [54] | 8 | 1 | 2 | 0 | 200 | 3 mH | - | - | Zero | 3 | 5 | 98.5 % @0.59 kW | Yes |
| [4] | 6 | 1 | 2 | 0 | 180 | 2.9 mH | - | - | Zero | 2 or 3 | 3 | 98.10 %@0.51kW | Yes |
| [55] | 6 | 3 | 3 | 0 | 180 | 3.2 mH | - | - | Zero | 3 | 3 | 97.9 % @ 0.5kW | Yes |
| [56] | 8 | 1 | 2 | 0 | 100 | 3 mH | - | - | Zero | 3 | 5 | 98. %@0.55kW | Yes |
| Proposed Inverter | 6 | 2 | 4 | 0 | 267 | 3 mH | - | - | About zero | 2 | 6 | 97.5%@0.5 kW | Yes |

Where, *S* = Switch, *D* = Diode, *C* = capacitor, *L* = Inductor, NA = Not available in the publication and $V_{in}$ = Input voltage.

except common ground type inverters introduced in [3, 26, 29] cannot eliminate the unpleasant leakage current totally and only can reduce it. Hence, the proposed inverter without an extra dc-dc stage has a boosting ability of 1.5 times the input voltage. Also, the proposed grid-connected inverter can generate six voltage levels and mitigate the leakage current. Moreover, the reported efficiency of the proposed inverter is acceptable in comparison with other topologies. Hence, the proposed inverter exhibits more merits than the conventional inverter in terms of voltage boost ability, minimizing leakage current, reactive power supporting ability, reducing the required dc-link voltage, and reducing the voltage stress on the devices.

In addition, Table V provide comparison results of the proposed topology with some other conventional grid-tied inverters. Considering Table V, it can be seen that the comparison is done in terms of total cost ($), cost/$P_{out}$ (PU), output power ($P_{out}$), total volume ($cm^3$), power density ($W/cm^3$), voltage stress and current stress of utilized switches. Based on this table, the per-unit value of total cost (P.U.) is less than all of the compared topologies except topologies [18], [19] and [50]. Therefore, compared to other proposed structures, the proposed topology is cost-effective. Compared other presented topologies in Table V except [17], [18], [37], [3] and [33], the proposed topology has the best value of the power density. Although the power density of the proposed topology is lower than topologies

TABLE V
COMPARISON RESULTS

| Topology | Total Cost ($) | $P_{out}$ (W) | P.U.= Cost/$P_{out}$ | Total volume ($cm^3$) | Power density ($W/cm^3$) | $V_{in}$(V) | Voltage stress | Current stress |
|---|---|---|---|---|---|---|---|---|
| OH5 [17] | 305.432 | 1000 | 0.31 | 194.5 | 5.14 | 400 | $V_{in}$ | $I_{o,max}$ |
| [18] | 39.7 | 1000 | 0.04 | 12.7 | 79 | 400 | $V_{in}$ | $I_{o,max}$ |
| [19] | 111.908 | 1200 | 0.093 | 297.1 | 4 | 400 | $V_{in}$ | $I_{o,max}$ |
| MH6 [47] | 203.14 | 300 | 0.68 | 2717 | 11 | 400 | $V_{in}$ | $I_{o,max}$ |
| Active NPC [48] | 185.27 | 750 | 0.30 | 699.1 | 1.1 | 400 | $V_{in}$ | $I_{o,max}$ |
| Common ground type [49] | 64.55 | 200 | 0.33 | 215.7323 | 9.3 | 250 | $2V_{in}$ | $I_{o,max}$ |
| HB-ZVR | 552.22 | 1000 | 0.552 | 454.3 | 2.2 | 400 | $V_{in}$ | $I_{o,max}$ |
| [29] | 241.4 | 510 | 0.50 | 68.9 | 7.4 | 200 | $2V_{in}$ | $I_{ch}$ |
| [3] | 115.12 | 513 | 0.23 | 89.1 | 5.76 | 200 | $2V_{in}$ | $I_{ch}$ |
| [50] | 53.81 | 620 | 0.087 | 198.9 | 3.12 | 180 | $2V_{in}$ | $I_{o,max}$ |
| [51] | 196.972 | 500 | 0.40 | 215.1 | 2.32 | 200 | $4V_{in}$ | $I_{ch}$ |
| [52] | 331.646 | 600 | 0.56 | 315.81 | 1.89 | 200 | $V_{in}$ | $I_{ch}$ |
| [32] | 190.503 | 600 | 0.32 | 105.66 | 5.76 | 100 | $V_{in}$ | $I_{ch}$ |
| [53] | 85.09 | 500 | 0.17 | 161.59 | 3.09 | 100 | $2V_{in}$ | $I_{ch}$ |
| [5] | 113.18 | 900 | 0.126 | 347.52 | 2.58 | 200 | $2V_{in}$ | $I_{ch}$ |
| [54] | 234.3 | 590 | 0.39 | 302.5 | 2.51 | 200 | $2V_{in}$ | $I_{ch}$ |
| [4] | 165.07 | 510 | 0.33 | 193.24 | 2.63 | 180 | $2V_{in}$ | $I_{ch}$ |
| [55] | 180.3 | 500 | 0.36 | 201.92 | 2.47 | 180 | $2V_{in}$ | $I_{ch}$ |
| [56] | 234.3 | 550 | 0.42 | 302.5 | 1.81 | 100 | $2V_{in}$ | $I_{ch}$ |
| Proposed | 88.66 | 770 | 0.12 | 200.1 | 3.49 | 267 | $V_{in}$ | $I_{ch}$ |

Where, $I_{o,max}$ = The maximum injected current to the grid, $I_{ch}$ = Charging current of capacitors and $V_{in}$ = Input voltage

[17], [18], [37], [3] and [33], it nevertheless has a higher overall efficiency. Although the power density of the proposed structure is less than structures [17], [18] and [29], but in comparison with these structures the proposed structure has the ability to eliminate the leakage current. Also, the proposed structure, unlike structures [18] and [19], can provide voltage boosting feature. Although the power density of the proposed topology is lower than that of structures [3] and [37], it nevertheless has a high efficiency. Also, unlike topology [37], the proposed topology can provide the voltage boosting capability. ($W/cm^3$), voltage stress and current stress of utilized switches. Based on this table, the per-unit value of total cost (P.U.) is less than all of the compared topologies except topologies [18], [19] and [50]. Therefore, compared to other proposed structures, the proposed topology is cost-effective. Compared other presented topologies in Table V except [17], [18], [37], [3] and [33], the proposed topology has the best value of the power density.

## VIII. EXPERIMENTAL RESULTS

In this part, to confirm the suggested grid-tied inverter's operation, the experimental results according to a 770 $W$ laboratory prototype have been provided, as shown in Fig. 11. A 267 $V$ input voltage source has been employed as the inverter's voltage source in this laboratory prototype. Table VI illustrates the specifications of the implemented laboratory prototype. At 770 $W$ output power, the peak value of output current is 5 $A$. Also, capacitors $C_1$ and $C_2$ are charged to half the input voltage or 133 $V$. Taking into account 6% voltage ripple for each of the capacitors, using equation (44) their capacitance is calculated as follows:

$$C_1 = C_2 = \frac{I_{mg}}{2\omega\Delta V_{C1}} = \frac{5}{2\times(2\pi\times 50)\times(0.06\times 133)} \simeq 1000\,\mu F \quad (76)$$

Capacitors $C_3$ and $C_4$ are each charged to the input voltage. Using equations (46) and (48) and considering the 6% voltage ripple for these capacitors, their capacitance is obtained as:

$$Q_{C3} = \int_{t_2}^{\frac{T}{2}-t_2} 5\sin\omega t dt = 0.0163\ C \quad (77)$$

$$t_2 = \frac{1}{100\pi}\sin^{-1}\left(\frac{267}{220\sqrt{2}}\right) = 3.3ms \quad (78)$$

$$C_4 = C_3 = \frac{0.0163}{0.06\times 267} = 1000\,\mu F \quad (79)$$

Equations (51) to (54) have explained how to design the output filter inductor value. As mentioned in the paper, the maximum ripple of the output inductor current occurs at a single power factor and $\omega t = \frac{\pi}{2}$. According to considering 10% of the current ripple value, the output filter inductance is calculated as follows:

$$L_f = \frac{1}{\Delta I_{Lf,\max}\cdot f_S}\left[5V_{mg} - \frac{2V_{mg}^2}{V_{dc}} - 3V_{dc}\right]$$
$$= \frac{1}{(0.1\times 5)\times 20\times 10^3}\left[5\times 220\sqrt{2} - \frac{2\left(220\sqrt{2}\right)^2}{267} - 3\times 267\right] = 3\,mH \quad (81)$$

Fig. 12 (a) indicates the output six-level voltage with 400 $V$ peak value and the sinusoidal grid injected current with the unity power factor. Therefore, in this respect, the maximum amplitude of the injected current to the grid is approximately 5 $A$. Moreover, Fig. 12(b) indicates the grid's voltage waveform plus the six-level output voltage of the suggested grid-connected inverter. As illustrates, the system

tracks the reference current through the filter-side inductor correctly. Therefore, the proposed inverter and its corresponding peak current controller method are capable of operating together properly. Utilizing the NPC-based method makes more limitation of leakage current. The voltage across of utilized capacitors are indicated in Fig. 12(c)-(d). Considering Fig. 12(c), the capacitor's voltage $V_{C1}$ and $V_{C2}$ are balanced to half of the input dc source ($V_{C1} = V_{C2} = 0.5\ V_{dc} = 133\ V$). Also, from Fig. 12(d), the voltage of capacitor $C_3$ and $C_4$ is balanced to the input voltage ($V_{C3} = V_{C4} = V_{dc} = 267\ V$). Based on Fig. 12(c)-(d), it can be understood that the voltage ripple of the mentioned capacitors is acceptable. The mentioned grid-tied inverter regarding reactive power supportability and by the usage of the PCC method can inject the sinusoidal current in various conditions of required power factor (PF) such as the grid voltage and injected current under the unity power factor, leading and lagging which are illustrated in Fig. 12 (a)-(c), respectively. As shown in this figure, there is no limitation to having the output reverse current. In addition, the grid voltage and injected current to the grid waveforms are shown in Fig. 13(d) to verify the proposed inverter's performance under output power changing condition. Based on Fig. 13(d), it can be seen that the amplitude of the injected current to the grid is changed from 4 A to 5 A. So that this issue leads to that the injected power to the grid has changed from 620 $W$ to 770 $W$. Figs. 14(a)-(d) show the voltage stress waveform across the utilized power switches and diodes. The voltage stress of the switch $S_1$ and diode $D_1$ are shown in Fig. 14(a) by blue and red waveforms, respectively. The switch $S_2$ and diode $D_2$ stress voltage is illustrated in Fig. 14(b) by blue and red waveforms, respectively. Fig. 14(c) illustrates the voltage stress waveform of the switches $S_3$ and $S_4$, and Fig. 14(d) shows the voltage stress waveform of the switch $S_5$. Based on this figure, it can be seen that the voltage stress of this switch consists of both positive and negative half cycle. Therefore, the switch $S_5$ is a bidirectional switch. In the PV systems, the total value of the parasitic capacitor is around 100 $nF$/1 $kW$. In the proposed inverter, the capacitance value of each parasitic capacitor is considered 50nF. The leakage current of parasitic capacitors $C_{PV1}$ and $C_{PV2}$ are illustrated in Fig. 15(a). Regarding this figure, the amplitude of $I_{CPV1}$ and $I_{CPV2}$ is less than 5 $mA$. Based on the IEEE standard (VDE 0216-1-1 IEEE), the maximum allowed value of leakage current for transformer less grid-tied inverters is 300 $mA$. So that the proposed inverter can pass the leakage current limitation of IEEE standard. Figs. 15(b)-(d) show the current stress of utilized power switches. Fig. 15(b) shows the current stress of the switches $S_1$ and $S_2$. Considering this figure, it can be seen that these switches pass the injected grid current along with capacitor charging current ($I_{S1} = I_{S2} = I_{mg} + I_{ch}$). With respect to this figure, peak value of capacitor charging current is 14 $A$ and peak value of injected grid current is 5 A. So that, the capacitor charging current is limited to 2.8 times of the injected grid current. The current stress of the switches $S_3$ and $S_4$ are presented in Fig. 15(c). Based on this figure, the peak value of current stress of these switches is equal to a peak value of injected grid current. The current stress of the switch $S_5$ is shown in Fig. 15(d). Considering this figure, it can be seen that the switch $S_5$ passes the injected grid current. In order to further investigate the performance of the proposed grid-tied inverter and its applied control system, the injected current into the grid, and the grid voltage at different values of the injected power to the grid have been measured. Regarding Figs. 16(a)-(c), the proposed inverter's injected power into the grid is 310 $W$, 460 $W$ and 620 $W$, respectively. In order to investigate the dynamic performance of the proposed structure, step changes of the reference current ($i_{ref}$) have been applied. Based on Fig. 16(d), the step change of the injected grid current is a change from 2.5 A to 5 A. So that, the injected power changes from 380 W to 770 W.

Concerning Fig. 17(a), the step change of the injected grid current is a change from 5 $A$ to 2.5 $A$. Based on this step change, the amplitude of active power decreases from 770 $W$ to 380 $W$. Fig. 17(b) shows the inverter output voltage along with the injected current to the grid under step change of the reference current. Considering this figure, the step change of the injected grid current is a change from 2.5 $A$ to 5 $A$. Therefore, the injected active power increases from 380 $W$ to 770 $W$. Fig. 17(c) illustrates the inverter output voltage and the injected current to the grid waveform under step change of the injected grid current is a change from 5 A to 2.5 $A$. Regarding Fig. 17(c), it can be seen that the injected power to the grid decreases from 770 $W$ to 380 $W$. The inverter output voltage and injected grid current under step change of the input voltage have been illustrated in Fig. 17(d). The

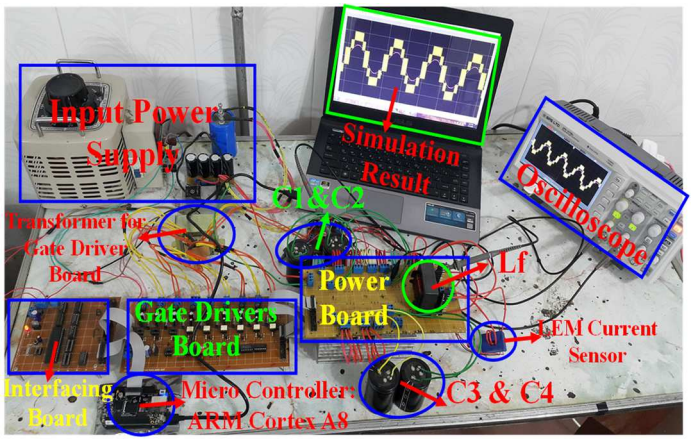
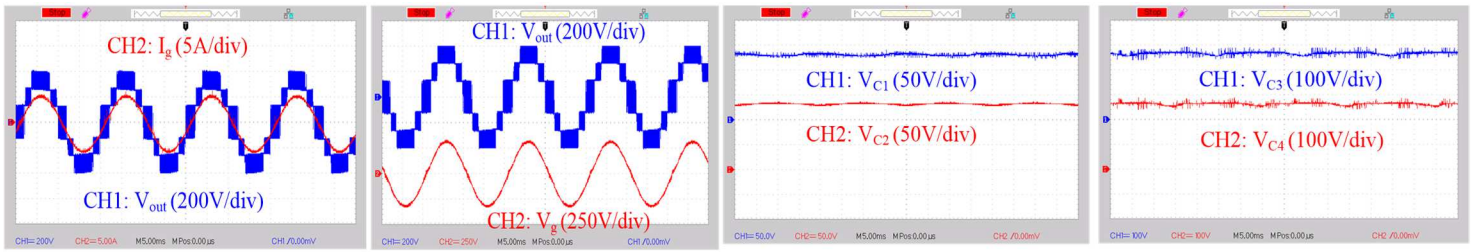



FIGURE 11. **Experimental prototype of the proposed grid-tied inverter.**

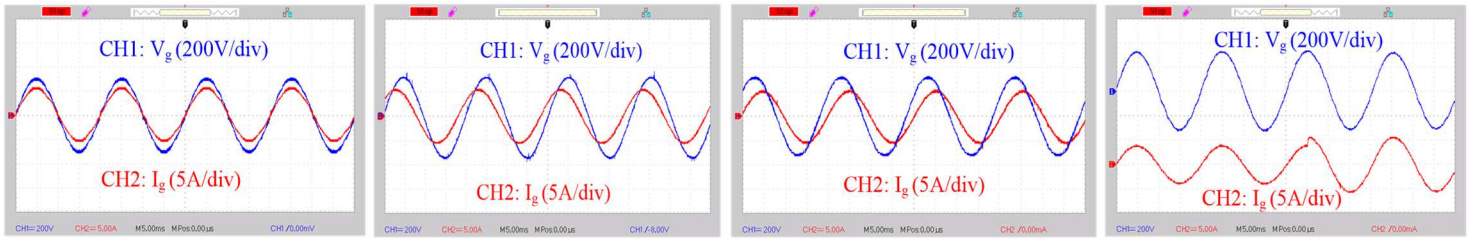
TABLE VI
LISTED OF SPECIFICATIONS OF THE UTILIZED LABORATORY PROTOTYPE

| Element | Type | Description |
|---|---|---|
| $S_1$, $S_2$, $S_3$, $S_4$ and $S_5$ | SPW47N60C3 | 650 V/47 $A$ |
| $D_1$ and $D_2$ | RURP3060 | 600 V/30 $A$ |
| microcontroller | Beagle Bone Black | ARM |
| Gate Driver | TLP-250 | IC |
| local grid's frequency | 50 Hz | - |
| Sampling frequency | 40 kHz | - |
| Switching frequency | 20 kHz | - |
| Input voltage | 267 V | - |
| Output voltage | 400 V | - |
| $C_1$ and $C_2$ | 200 V | 1000 $uF$ |
| $C_3$ and $C_4$ | 350 V | 1000 $uF$ |
| $L_f$ | Ferrite core | 3 $mH$ |



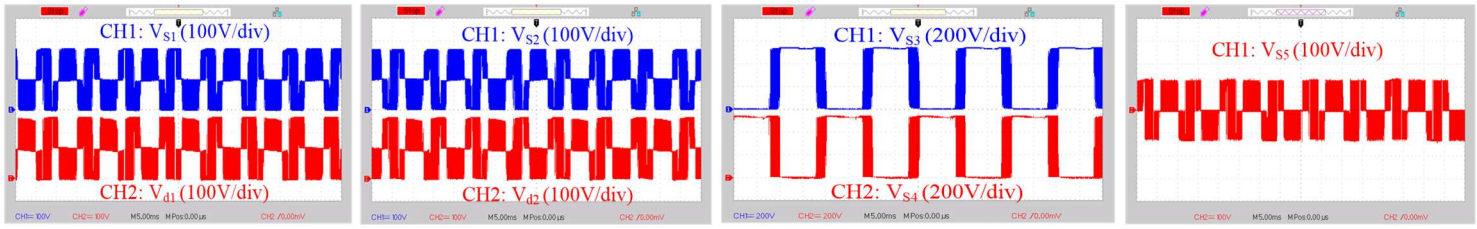

(a) (b) (c) (d)

FIGURE 12. **The Experimental results (a) inverter output voltage waveform (200 V/div) and the injected grid current (5 A/div), (b) inverter output voltage waveform (200 V/div), the local grid voltage (250 V/div), (c) voltage across of $C_1$ and $C_2$ (50 V/div), (d) voltage across of $C_3$ and $C_4$ (100 V/div).**



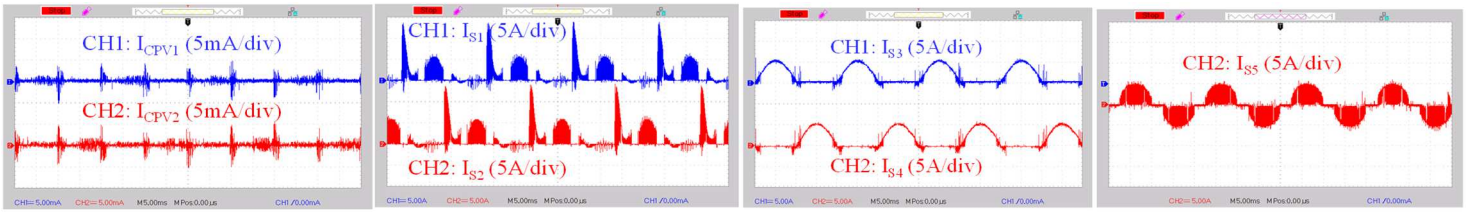

(a) (b) (c) (d)

FIGURE 13. **The experimental results: (a) the grid voltage (200 V/div) and the injected grid current (5 A/div) waveforms under unity PF, (b) the grid voltage (200 V/div) and the injected grid current (5 A/div) waveforms under leading PF, (c) the grid voltage (200 V/div) and the injected grid current (5 A/div) waveforms under lagging PF, (d) grid voltage (200 V/div) and the injected current to the grid (5 A/div) on the output power changing condition.**



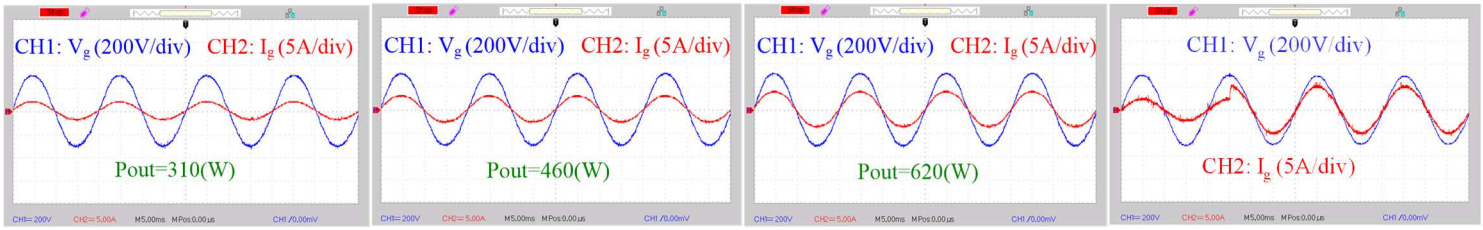

(a) (b) (c) (d)

FIGURE 14. **The experimental results: (a) the voltage stress of $S_1$ and $D_1$ (100V/div), (b) the voltages stress of $S_2$ and $D_2$ (100V/div), (b) the voltage across of switches $S_3$ and $S_4$ (200V/div), (d) the voltage across of switch $S_5$ (100V/div).**



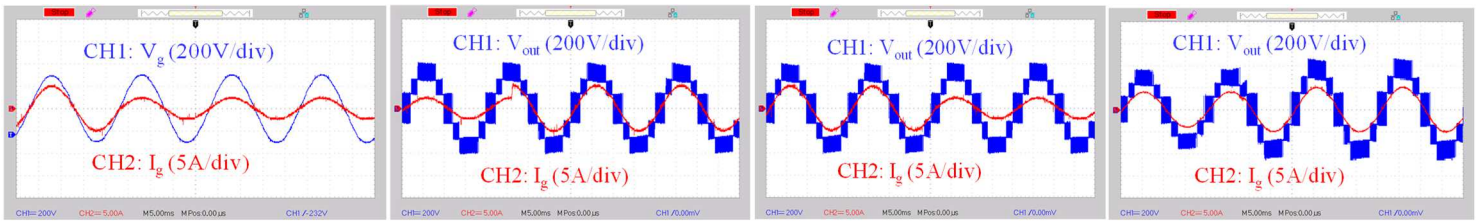

(a) (b) (c) (d)

FIGURE 15. **Experimental results: (a) leakage current of $C_{PV1}$ and $C_{PV2}$ (5mA/div), (b) the current stress of switches $S_1$ and $S_2$ (5A/div), (c) the current stress of switches $S_3$ and $S_4$ (5A/div), (d) the current stress of switch $S_5$ (5A/div).**



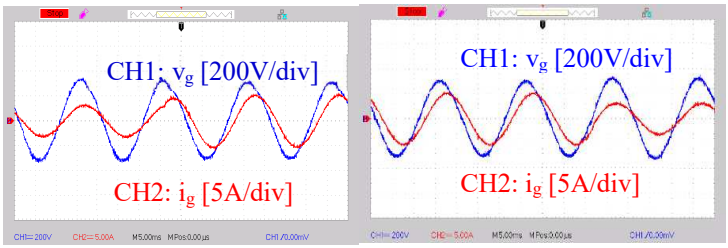

(a) (b) (c) (d)

FIGURE 16. **Experimental results: the grid voltage (200 V/div) and the injected grid current (5 A/div) waveforms at the output power of (a) 310 W, (b) 460 W, and (c) 620 W, (d) grid voltage (200 V/div) and injected grid current (5 A/div) under a step change in the amplitude of reference current ($i_{ref}$).**




(a) (b) (c) (d)

FIGURE 17. **Dynamic performance of the proposed inverter under a step change in the amplitude of reference current ($i_{ref}$): (a) grid voltage (200 V/div) and injected grid current (5A/div) (b) output voltage (200V/div) and injected grid current (5A/div) (c) output voltage (200 V/div) and the injected grid current (5A/div) (d) inverter output voltage (200V/div) waveform along with injected current to the grid (5A/div) under changing the voltage in the input source.**




(a) (b)

FIGURE 18. **Experimental results of the grid voltage and injected grid current under step change in the reactive power modes. The output power changes (a) from 550 VA with PF=0.95 lag to 770 VA with PF=0.81 lag (b) from 770 VA with PF=0.81 lag to 550 VA with PF=0.95 lag.**

step-change of the input voltage changes from 240 *V* to 300 *V*. Since the proposed topology has a voltage gain of 1.5, by applying this step change, the peak value of output voltage will increase from 360 V to 450 *V*. The applied step change will affect the injected grid power, and the output power changes from 620 *W* to 770 *W*. In order to validate the step change in the reactive power operation of the proposed inverter the related experimental results are presented in Fig. 18. Regarding Fig. 18(a), the amplitude of the reference current increase from 3.2 *A* to 5 *A*. Therefore, the value of the injected power to the grid increases from 500 *VA* (at PF = 0.95 lag) to 770 *VA* (at PF=0.81 lag). Considering Fig. 18(b), the amplitude of the reference current decrease from 5 *A* to 3.2 *A*. So that, the value of the injected power to the grid decreases from 770 *VA* (at PF = 0.81 lag) to 500 *VA* (at PF = 0.95 lag). Based on Fig. 18, it can be concluded that the proposed topology provides reactive power support to the grid under step change conditions. Furthermore, Fig. 19 shows the harmonic spectrum with THD of injected current to the grid at 770 *W* output power. According to this figure, the THD of injected current into the grid is about 2.05%. Based on IEC 61000-3-2 and IEEE 1547.2-2008 standards the limit of THD of injected current to the grid is less than 5%. Therefore, the proposed structure can pass these mentioned standards.

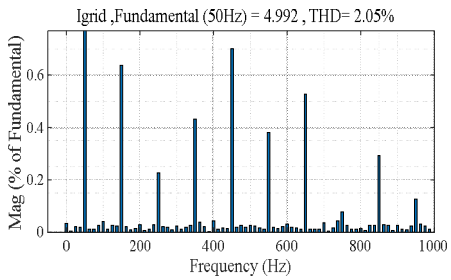



FIGURE 19. **Harmonic spectrum with THD of injected current to the grid at 770 W output power**

## IX. CONCLUSION

A novel transformer-less six-level grid-connected inverter with reduced leakage current abilities is presented in this paper. The proposed inverter's advantages can be mentioned as reduced leakage current, voltage boosting ability, reactive power supporting feature, and high efficiency. Without an extra dc-dc stage, the proposed inverter has a boosting ability of 1.5 times the input voltage and reduces the system's overall weight, loss, and cost. Moreover, this topology generates six levels of voltages, including ±0.5 $V_{dc}$, ±1 $V_{dc}$, and ±1.5 $V_{dc}$, which reduces the size of the filter and total harmonic distortion. To control both active and reactive powers, the PCC strategy is applied. Besides, using the PCC method, the injected grid current has a suitable quality under any PF conditions. The design of utilized circuit components is developed in this paper. Also, in order to highlight the benefits of the proposed inverter, it has been compared with some other grid-connected inverters. Finally, to validate the characteristics mentioned above and the proposed inverter's performance, experiments are carried out using a 770 W laboratory prototype.

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**NASER VOSOUGHI KURDKANDI** was born in Bostanabad, East Azerbaijan Province, Iran, in 1989. He received the B.Sc. degree in electrical engineering from the Islamic Azad University, South Tehran Branch, Tehran, Iran, in 2011, and the M.Sc. and Ph.D. degrees in electrical engineering and power electronics from University of Tabriz, Tabriz, Iran, in 2014 and 2019, respectively. His current research interests include multilevel inverters, grid-connected PV inverters, dc–dc switched-capacitor and switched-inductor converters, fast charge station for electric vehicles, battery-based energy storage systems, and induction motor drives.

**MILAD GHAVIPANJEH MARANGALU** was born in Urmia, Iran, 1992. He received the B.Sc. from Urmia University, Urmia, Iran, in 2014, and M.Sc. degree in power electrical engineering from the University of Urmia, Urmia, Iran, in 2018. He is currently working toward the Ph.D. degree in the Electrical and Computer Engineering Department, University of Tabriz, Tabriz, Iran. His current researches include multilevel inverter, grid-tied photovoltaic inverter, High step-up power electronic converters, control system of the multilevel inverter and renewable energy systems.

**SHAMIM MOHAMMADSALEHIAN** was born in Mahabad, Iran, 1993. She received the B.Sc. degree in power electrical engineering from the University of Tabriz, Tabriz, Iran, the M.Sc. degree in power electronics and electrical machines from Mohaghegh Ardabili University, Ardabil, Iran, in 2015 and 2018, respectively. Her research interests include the design and analysis of power electronic converters/inverters and their specific applications. Also, interconnection of renewable energies with power electronic converters and their control methods appeals to her.

**HADI TARZAMNI** (Student Member, IEEE) was born in Tabriz, Iran, in 1992. He received the B.Sc. and M.Sc. degrees with first class honors in power electrical engineering from the Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran, in 2014 and 2016, respectively. He is currently working toward the Ph.D. degree in power electronics engineering under a dual-degree doctoral program at the Department of Electrical Engineering, Sharif University of Technology, Tehran, Iran, and the Department of Electrical Engineering and Automation, Aalto University, Finland. He has authored and coauthored more than 25 journal and conference papers. He also holds 6 patents in the area of power electronics. He is the recipient of best paper award in 10th International Power Electronics, Drive Systems and Technologies Conference (PEDSTC) in 2019. He has received a three-year Aalto ELEC Doctoral School grant in 2021. Since Jan. 2021, he has been a researcher at the Department of Electrical Engineering and Automation; and the Department of Electronics and Nanoengineering, Aalto University, Finland. His research interests include power electronic converters analysis and design, DC-DC and DC-AC converters, high step-up power conversion, soft-switching and resonant converters, and reliability analysis.

**YAM P. SIWAKOTI** (S'10–M'14–SM'18) received the B.Tech. degree in electrical engineering from the National Institute of Technology, Hamirpur, India, in 2005, the M.E. degree in electrical power engineering from the Norwegian University of Science and Technology, Trondheim, Norway, and Kathmandu University, Dhulikhel, Nepal, in 2010, and the Ph.D. degree in Electronic Engineering from Macquarie University, Sydney, Australia, in 2014. He was a postdoctoral fellow at the Department of Energy Technology, Aalborg University, Denmark (2014-2016). He was a visiting scientist at the Fraunhofer Institute for Solar Energy Systems, Freiburg, Germany (2017/2018). He is also a recipient of the prestigious Green Talent Award from the Federal Ministry of Education and Research, Germany in 2016. Currently he is a Senior Lecturer in the Faculty of Engineering and Information Technology, University of Technology Sydney, Australia. He serves as an Associate Editor of three major journals of IEEE (IEEE Transactions on Power Electronics, IEEE Transactions on Industrial Electronics and IEEE Journal of Emerging and Selected Topics in Power Electronics) and the IET Power Electronics. He is also a peer review college member of Engineering and Physical Science Research Council (EPSRC), UK.

**MD. RABIUL ISLAM** (Senior Member, IEEE) received the Ph.D. degree from University of Technology Sydney (UTS), Sydney, Australia, in 2014 in electrical engineering. He was appointed a lecturer at RUET in 2005 and promoted to full professor in 2017. In early 2018, he joined at the School of Electrical, Computer, and Telecommunications Engineering (SECTE), University of Wollongong (UOW), Wollongong, Australia. He is a Senior Member of IEEE. His research interests are in the fields of power electronic converters, renewable energy technologies, power quality, electrical machines, electric vehicles, and smart grid. He has authored or co-authored 160 papers (including 46 IEEE Transactions/IEEE Journal papers) in international journals and conference proceedings. He has written or edited 4 technical books published by Springer. He has served as a Guest Editor for IEEE Transactions on Energy Conversion, IEEE Transactions on Applied superconductivity and IET Electric Power Applications. He has been serving as an Editor for IEEE Transactions on Energy Conversion and IEEE Power Engineering Letters, and Associate Editor for IEEE Access. He has received several funding from Government and Industries including Australian Government ARC Discovery Project 2020 entitled "A Next Generation Smart Solid-State Transformer for Power Grid Applications".

**KASHEM M. MUTAQI** (M'01, SM'05) received the B.Sc. degree in electrical and electronic engineering from Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh in 1993, the M. Eng. Sc. degree in electrical engineering from University of Malaya, Kuala Lumpur, Malaysia in 1996 and the Ph.D. degree in Electrical Engineering from Multimedia University, Selangor, Malaysia in 2001. Currently, he is a full Professor and the Discipline Leader – Electrical Engineering at the School of Electrical, Computer, and Telecommunications Engineering at the University of Wollongong, Wollongong, Australia. He was associated with the University of Tasmania, Hobart, Australia as a Research Fellow/Lecturer/Senior Lecturer from 2002 to 2007, and with the Queensland University of Technology, Brisbane, Australia as a Research Fellow from 2000 to 2002. Previously, he also worked for Multimedia University as a Lecturer for three years. He has more than 22 years of academic experience and authored or coauthored 410 papers in international journals and conference proceedings. He has been cited highly for his work in the control of renewable and distributed power generation. His research interests include distributed generation, solid state transformer, power converters, power electronic applications, renewable energy, solar PV, wind turbines, wave energy, electrical vehicles, smart grids, micro-grids, standalone power supply, power grids, power system planning and control. He is a Fellow of the Institution of Engineers Australia (FIEAust). He is also a Fellow of the UK Institution of Engineering and Technology (FIET).