

ment; R. D. Moyer, Sandia, for guidance in microwave and preliminary slot-line evaluation; and T. W. McKinney, Sandia, for assistance in design and fabrication.

REFERENCES

- [1] B. D. Josephson, "Possible new effects in superconductive tunneling," *Phys. Lett.*, vol. 1, p. 251, 1962.
- [2] A. Hartland, "A new system for monitoring the national standard of voltage at the NPL," presented at Euromeas, London, Sept. 1977.
- [3] V. Kose, "Recent advances in Josephson voltage standards," *IEEE Trans. Instrum. Meas.*, vol. IM-25, no. 4, pp. 483-489, Dec. 1976.
- [4] B. F. Field and V. W. Hesterman, "Laboratory voltage standard based on $2e/h$," *IEEE Trans. Instrum. Meas.*, vol. IM-25, no. 4, pp. 509-511, Dec. 1976.
- [5] T. F. Finnegan and A. Denenstein, "High accuracy potentiometers for use with 10 millivolt Josephson devices I. Double series-parallel exchange comparator," *Rev. Sci. Instrum.*, vol. 44, no. 8, pp. 944-953, Aug. 1973.

A New Switching Technique for Binary Resistive Dividers

ROBERT D. CUTKOSKY, FELLOW, IEEE

Abstract—A binary resistive divider network has been found which utilizes N cascaded DPDT reversing switches plus one SPDT switch for an N -bit divider. The network features a simple and accurate method for internal calibration. With a fixed divider input voltage the power dissipated in each resistive element is independent of switch setting.

I. INTRODUCTION

MANY OTHERWISE satisfactory resistive dividers are found in practice to be very difficult or time consuming to calibrate. This problem is most effectively handled during the design of the instrument, at which time much future frustration can often be eliminated. The resistive divider described here contains its own internal calibration circuitry, but it would probably be an impractical device if it were not coupled to a microprocessor. It is hoped that the technique contains enough advantages to make this additional complexity worthwhile.

II. BASIC CIRCUIT

The network shown in Fig. 1 is proposed for use as a binary resistive divider. It can be seen that with no output load, the resistance of the network to the right of each DPDT reversing switch is always 2 (arbitrary) units of resistance, so that with V_{in} fixed, the power in each resistance element is independent of all switch settings. It also can be seen that if all switches are on "0" (as represented in Fig. 1), $V_{out} = 0$; if S_1 is on "1" and all other switches are on "0", $V_{out} = V_{in}$. All intermediate output voltages representable by

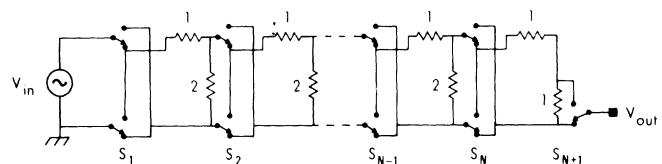


Fig. 1. An N -bit binary resistive divider. Relative resistances are indicated.

an N -bit binary code can be obtained by two different settings of the cascaded switches. This redundancy can be used to provide the divider with a self-calibration facility.

Consider the network with all switches on "0" except S_{N+1} (switch code '0—001). Then, $V_{out}/V_{in} = 1/2^N$. If the switch code is now changed to 0—011, one again has $V_{out}/V_{in} = 1/2^N$. The effect of the operating switch N is to interchange the dropping resistor and the load resistor to the right of S_N . If V_{out} is observed to change, the difference can be retained as a correction for the N th divider.

In a similar way, one can measure the change in V_{out} when the switch code changes from 0—0010—0 ($(k+1)$ th switch set) to 0—0110—0 (k th and $(k+1)$ th switch set) to obtain the correction to the k th divider. Note that $V_{out}/V_{in} = 1/2^k$ and that the load resistor for the k th divider contains all of the resistance elements to the right of stage k ; since this resistance is independent of all switch settings, however, no error will occur when the individual corrections are combined. It is therefore sufficient to make N difference measurements ($2N$ individual measurements) to completely calibrate the binary divider.

The N difference measurements required in the above scheme could be performed with ease if a fixed voltage

Manuscript received June 5, 1978; revised July 27, 1978.
The author is with the Electrical Standards Division, National Bureau of Standards, Washington, DC 20234.

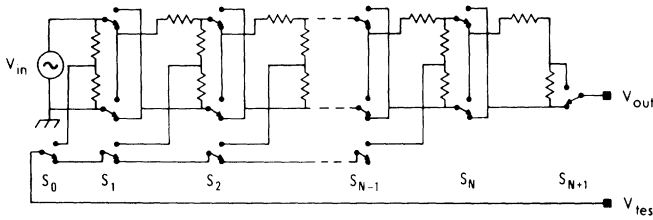


Fig. 2. An N -bit divider with enhanced self-calibration capability. All resistances are nominally equal.

source were available which provided constant output voltages programmable to approximate each of the N voltages to be compared. An ordinary N -bit uncalibrated divider could be used for this purpose provided it had the requisite stability.

Several ways can be found for generating the required reference voltages within the divider itself, one of which is shown in Fig. 2. To calibrate the k th divider, first set switches $k-1$ and $k+1$ to "1", and set all other switches to "0". Measure the ideally zero voltage, $V_{out} - V_{test}$. Second, set switch k to "1", leaving the other switches as they were. Any change in $V_{out} - V_{test}$ can be attributed to an error in the k th divider.

III. RATIO CALCULATIONS

In the following analysis, let S_k be the logical value of the k th switch; that is, $S_k = 0$ if the k th switch is "down" as shown in the figures, and $S_k = 1$ if it is reversed. Using the nomenclature of Fig. 3, neglecting switch and wiring resistances and writing $\epsilon_k = (Z_{Lk} - Z_{Dk}) / (Z_{Lk} + Z_{Dk})$, one has $V_1/V_{in} = S_1$, $V'_1/V_{in} = 1 - S_1$, and

$$V''_1/V_{in} = 1/2 + (1 - 2S_1)\epsilon_1/2.$$

More generally, V'_k is obtained by replacing S_k by $1 - S_k$ in the expression for V_k , and $V''_k = (V'_k + V_k)/2 + (V'_k - V_k)\epsilon_k/2$. The recursion formula

$$V_{k+1}/V_{in} = V_k/V_{in} + (S_{k+1}/2^k) \prod_{p=1}^k (1 - 2S_p)(1 + \epsilon_p)$$

can be readily verified, from which it follows that

$$\begin{aligned} V_{N+1}/V_{in} = & S_1 + S_2(1 - 2S_1)(1 + \epsilon_1)/2 + S_3(1 - 2S_2) \\ & \cdot (1 - 2S_1)(1 + \epsilon_1)(1 + \epsilon_2)/4 + S_4(1 - 2S_3) \\ & \cdot (1 - 2S_2)(1 - 2S_1)(1 + \epsilon_1)(1 + \epsilon_2) \\ & \cdot (1 + \epsilon_3)/8 + \dots \end{aligned}$$

For calibration of the k th ratio, measure $V_{N+1}/V_{in} = V_{out}/V_{in}$ first with $S_k = 0$, $S_{k+1} = 1$, and then

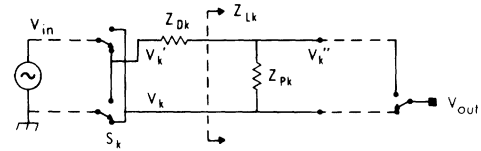


Fig. 3. The k th stage of a binary divider with voltages and impedances labeled. The load resistance Z_{Lk} is made up of all successive resistors in the chain. Z_{Dk} is the dropping resistance.

with $S_k = 1$, $S_{k+1} = 1$, in each case with all $S_p = 0$ for $p > k + 1$. The difference between these ratios is given by

$$\Delta_k = \frac{\epsilon_k}{2^{k-1}} \prod_{p=1}^{k-1} (1 + \epsilon_p) \approx \epsilon_k/2^{k-1}$$

for $2 \leq k \leq N$, and $\Delta_1 = \epsilon_1$. Note, however, that the sign to be attached to the Δ_k 's must be reversed if during calibration an odd number of the switches to the left of the k th switch are logically true.

Ignoring terms of the order ϵ^2 and higher, we have finally

$$\begin{aligned} V_{N+1}/V_{in} \approx & S_1 + S_2(1 - 2S_1)(1 + \Delta_1)/2 + S_3(1 - 2S_2) \\ & \cdot (1 - 2S_1)(1 + \Delta_1 + 2\Delta_2)/4 \\ & + S_4(1 - 2S_3)(1 - 2S_2) \\ & \cdot (1 - 2S_1)(1 + \Delta_1 + 2\Delta_2 + 4\Delta_3)/8 + \dots \end{aligned}$$

If each of the voltage measurements involved in the calibration of the divider has an uncertainty of σ_i , then each Δ_k will be uncertain by $\sigma_i\sqrt{2}$. The total uncertainty in the corrected value for V_{N+1} , σ_T , may be calculated from the preceding equation. It is found that for an N -bit divider, the maximum uncertainty in V_{N+1} , $\max(\sigma_T)$, occurs when all of the switches are up ($S_k = 1$ for all k). To a very close approximation, $\max(\sigma_T) \approx \sigma_i\sqrt{2}\sqrt{N+1}/3$. Although these assertions about $\max(\sigma_T)$ are made without proof, they may be readily verified for realistic values of N .

IV. PRACTICAL CONSIDERATIONS

Resistive dividers achieve their highest accuracy when the resistances are chosen so that the uncertainties due to switch resistance variations are about equal to those due to leakage resistance variations. If conventional switches or relays are used, 100 000- Ω resistors are about optimum and should yield divider accuracies around 1 part in 10^7 . It is expected that a commercial solid-state digital-to-analog converter would be used in the low-order end of a practical divider to reduce the number of relays to a minimum. A 17-bit DAC combined with an 8-bit binary divider is being considered for voltage measurements up to 20 V.