A New Technique for Characterization of Digital-to-Analog Converters in High-Speed Systems

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ABSTRACT
In this paper, a new technique for characterization of digital-to-analog converters (DAC) used in wideband applications is described. Unlike the standard narrowband approach, this technique employs Least Square Estimation to characterize the DAC from dc to any target frequency. Characterization is performed using a random sequence with certain temporal and probabilistic characteristics suitable for intended operating conditions. The technique provides a linear estimation of the system and decomposes nonlinearity into higher-order harmonics and deterministic periodic noise. The technique can also be used to derive the impulse response of the converter, predict its operating bandwidth, and provide far more insight into its sources of distortion.

1. INTRODUCTION
Architectures for high-speed, wideband communication systems have gradually changed to utilize advances in fabrication processes and system engineering. On the one hand, serial data systems have replaced parallel data buses in many wireline applications. On the other hand, aggressive scaling of transistors in CMOS processes has enabled implementation of complicated digital signal processing (DSP) blocks operating at high speed with moderate power consumption. As a result, many features previously implemented in analog blocks have gradually been replaced by digital solutions. Digital solutions are much more reliable and much less susceptible to process, voltage, and temperature variations.

Interfacing the digital bit streams from the DSP blocks to the communication channel requires data converters with high speed and high resolution. Shown in Fig. 1, a generic high-speed communication system consists of a transmit DSP module and a digital-to-analog converter (DAC) in the transmitter, and an analog-to-digital converter (ADC) and a receive DSP module in the receiver. This architecture has been commonly used in a variety of wireline applications such as Gigabit Ethernet, DSL, and backplane communications.

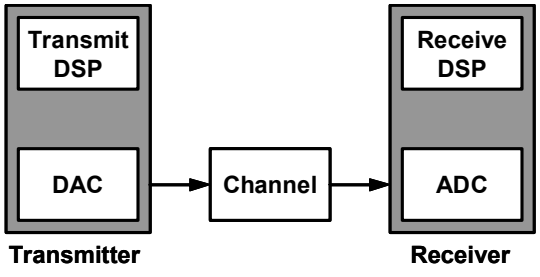

Figure 1: Generic high-speed communication system

This architecture provides flexibilities such as portability across multiple technologies and operation at different speeds that are extremely useful for implementation of mixed-mode systems. The DSP modules can easily be reconstructed in different processes, and the porting effort is reduced to the migration of the data converters. Meanwhile, the operational speed of these systems is scalable with a single clock frequency. Note that analog signal processing blocks (e.g. analog filters) require sophisticated calibration techniques in order to provide these features.

Data converters should be designed to meet requirements for speed, resolution, and linearity. For high-speed applications, the input data signal is random, and signal bandwidth stretches from zero to the Nyquist frequency. This wide-bandwidth requirement poses a new challenge in the design of the data converters and requires new methodologies to characterize their performance.

Single-tone and two-tone tests are typically used to measure the linearity of data converters [1]-[4]. If the data converter is designed to operate with narrowband signals, tone frequencies are chosen around the frequency band of signal for accuracy. As the bandwidth of the input signal increases, this characterization method provides inconsistent results dependent on the choice of the input frequency because many sources of nonlinearity are frequency dependent (e.g. voltage-dependent capacitors).

Traditional measures of maximum resolution and settling time to determine a data converter's speed and resolution also neglect the fact that data converters are parts of bigger systems. Linear distortion of a data converter, and even its nonlinear terms if correctly estimated, can be compensated for by the DSP. In addition, the metrics defined by these measures are not directly related to the ultimate performance measures of communication systems, including Signal to Noise Ratio (*SNR*) and Bit Error Rate (*BER*).

In this paper, we describe the limitation of tone tests for wideband applications and present a new technique to characterize data converters over an extended frequency range. This technique provides detailed insight into the circuit dynamics and introduces useful metrics such as impulse response and large-signal circuit bandwidth. It also provides a platform to characterize the entire communication system at the speed of a high-level simulator yet with the precision of transistor-level simulator.

In Section 2 we describe dynamic characterization techniques with emphasis on DAC design and talk about their limitations for wideband applications. Next, in Section 3 we describe a characterization technique based on Least Squares Estimation and expand on its features in Section 4. Lastly, we apply our method to an 8-bit current DAC in Section 5.

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2. DYNAMIC CHARACTERIZATION

Dynamic tests are designed to measure speed and linearity of a DAC. Speed is evaluated by measuring the settling time of the system for the maximum output swing (Figure 2(a)). Linearity is usually measured by analyzing the output spectrum and monitoring the output spur levels when a single or two tones are applied to the input (Figure 2(b)).

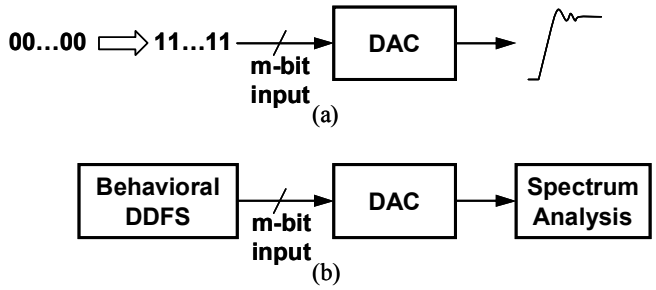

Figure 2: Dynamic characterization: (a) settling and (b) linearity tests

The input tones are produced using a behavioral Direct Digital Frequency Synthesizer (DDFS). There are infinite combinations for the input and clock frequencies in such systems. One choice is to sweep the clock frequency when the input frequency is slightly offset from 1/3 or 1/4 of the clock frequency. The small frequency offset randomizes the quantization noise and allows the distortion products to be easily observed [1].

Output spectrum analysis is in the form of either total-harmonic distortion measurement for a single tone, or inter-modulation measurement for two tones. The former is an indicator of spurious-free dynamic range (*SFDR*) and the latter is an indicator of third-order inter-modulation product (IM_3).

Several issues arise if these tests are applied to a wideband system. They include choices of tone frequency, tone offset, and applicability of such measures to a wideband system. Figure 3 shows the results of a two-tone test on a simple wideband buffer. Linearity of the circuit in this experiment was characterized by measuring IM_3 for the input frequency pairs shown on the x-axis. For most of the frequency pairs linearity improves by 2 dB for every 1 dB of drop in signal amplitude which is consistent with theory. However, measured linearity fluctuates depending on the tone frequencies. A secondary effect is that IM_3 is shaped by the bandwidth of the circuit and changing the frequency offset varies the third-order inter-modulation magnitude, thus affecting the linearity measurement.

In order to characterize a wideband system, instead of narrow-band tones, sequences should be used that represent the characteristics of the input data. For example, if the input to the DAC is random data, a random sequence is the best sequence that can be used to characterize the data converter. On the other hand, if the input to the DAC comes from a high-pass equalizer, a correlated sequence representing the spectral characteristics of the equalizer output should be used for characterization. In the following section we devise an approach to isolate the linear and nonlinear effects of the data converter by finding a linear fit to the signal and considering the residue as nonlinearity using an input sequence with desired spectral characteristics [5].

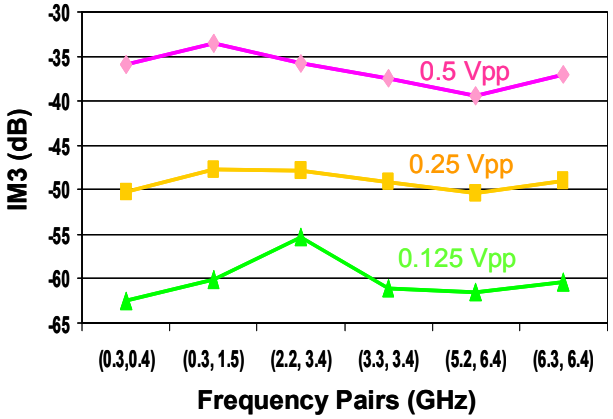

Figure 3: Two-tone characterization of a wideband buffer

3. LEAST SQUARES ESTIMATION

3.1 Linearization

This technique is based on modeling the time domain response of the DAC with a linear filter (h). Using this approach, we assume that the ideal DAC output is given by the convolution of the input and h ($y=h*x$). The best fit to h is derived by minimizing the energy of the error.

In order to characterize the DAC using this flow, we generate a piece-wise linear random sequence using Matlab and feed it to SPICE (Figure 4). Temporal and probabilistic distribution of the random sequence is set to model a typical operating condition. Over-sampling rate, r, in Fig. 4 represents the time-resolution at which estimation is performed.

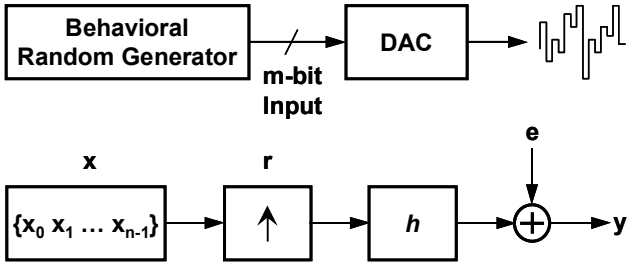

Figure 4: Wideband characterization using a random sequence

The input file produces combination of sequences that produce some worst-case effects including maximum output swing and maximum output glitch energy. The output of the DAC is stored in a text file and is fed back to Matlab.

Using the linearized model of Fig. 4, we define the system as:

$$y = Xh + e, \tag{1}$$

Where,

$$X = \begin{pmatrix} x_0 & 0 & \cdots & 0 & \cdots & x_{n-1} & 0 & \cdots & 0 \\ 0 & x_0 & \cdots & 0 & & 0 & x_{n-1} & & 0 \\ & & \ddots & & & & & \ddots & \\ 0 & 0 & \cdots & x_0 & \cdots & 0 & 0 & \cdots & x_{n-1} \end{pmatrix}^T \tag{2}$$

In this equation, X is a convolution matrix with nr rows and r columns (n is the number of input symbols and r is the up-sampling rate, their typical values are 500 and 20, respectively). The length of h (l) should be sufficiently large to model all dispersion created by the DAC.

Next we define *Error* and minimize it by letting its derivative with respect to h to go to zero.

$$Error = e^T e \tag{3}$$

This will yield to:

$$h = (X^T X)^{-1} X^T y \tag{4}$$

$$Error = y^T y - (y^T X)(X^T X)^{-1}(X^T y) \tag{5}$$

Linearity of the system is measured using its signal-to-distortion ratio (*SDR*) which can be defined as:

$$SDR = \frac{(y-e)^T (y-e)}{Error} = \frac{h^T X^T X h}{Error} \tag{6}$$

We now revisit the wideband buffer, previously characterized in Fig. 3, and apply the wideband technique to it. We note that the new results are relatively close but more pessimistic than the results derived from two-tone IM_3 tests (Fig. 5). This can be attributed to the fact that the wideband technique takes into account nonlinearities across the entire frequency range rather than a narrow slice. It should be noted that the results derived from the wideband technique tend to saturate due to the accumulation of numerical error. However, this saturation occurs at ranges beyond the required resolution of the system.

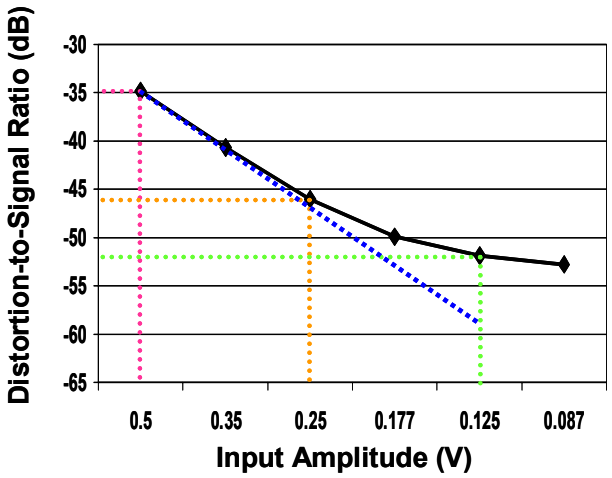

Figure 5: Wideband characterization of the circuit modeled in Fig. 3

3.2 Higher-order harmonics

The technique described in this paper, also provides the flexibility of decomposing the total error into higher-order harmonics, periodic noise sources (such as clock feedthrough and switching noise), and any other sources of error.

Using the Volterra series [6]-[7], the output can be written as (Figure 6(a)):

$$y(n) = h_0(n) + \sum_{m_1} x(n-m_1)h_1(m_1) + \sum_{m_1,m_2} x(n-m_1)x(n-m_2)h_2(m_1,m_2) + \cdots \tag{7}$$

In order to derive the energy of harmonics up to m^{th} order we describe the output of our system using a matrix form.

$$y = h_0 1 + X_1 h_1 + X_2 h_2 + \cdots + X_m h_m + e \tag{8}$$

In this equation, X_1 is the input convolution matrix, similar to the matrix described in 3.1. Other matrices (X_2 to X_m) are higher order input convolution matrices in which x_0 to x_{n-1} are replaced by x_0^i to x_{n-1}^i, where i is the index of matrix, h_0 is a scalar and represents the average output dc value caused by data-independent sources like clock or supply noise. Nonlinear cross-product terms are neglected in this formulation but can be included if expected to be large.

Again, we minimize error using Least Squares Estimation and derive h_0, h_1, h_2 … h_m. This approach will provide us with linear filters for the input signal and its higher-order harmonics.

Another observation is that many data-independent noise sources in the system are cyclo-stationary in nature. In other words, they repeat every cycle time. Therefore, instead of having their average effect represented by a single variable h_0, it is more interesting to obtain the average time domain effect over one period. This can be accomplished if we rewrite our Volterra expansion as follows:

$$y = I_0 b + X_1 h_1 + X_2 h_2 + \cdots + X_m h_m + e \tag{9}$$

Where,

$$b = [b_0 \quad b_1 \quad \ldots \quad b_r]^T, \text{ and } I_0 = [I_{r\times r} \quad I_{r\times r} \quad \cdots]^T$$

I_{rxr} is an r by r identity matrix.

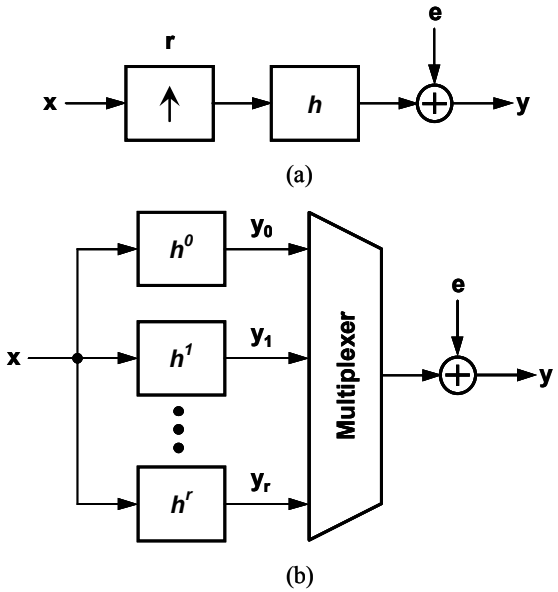

Figure 6: Harmonic calculation using (a) generic system, and (b) polyphases

In this formulation we have limited averaging only to output samples at similar positions within consecutive symbol intervals (Fig. 7).

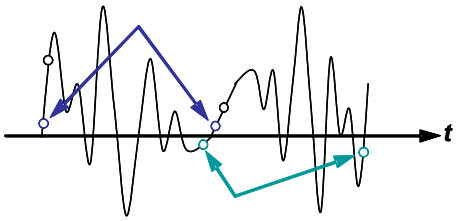

Figure 7: Samples of cyclo-stationary signal

The above equation can be written in a more compact matrix form as follows:

$$y = \begin{bmatrix} \mathrm{I}_0 & X_1 & \cdots & X_m \end{bmatrix} \begin{bmatrix} b & h_1 & \cdots & h_m \end{bmatrix}^T + e \quad (10)$$

The first term in brackets is equivalent to X in the Least Squares Solution presented in Section 3.1.

Further computational simplicity can be achieved by representing the h filters with their polyphase forms (Fig. 6(b)) and rewriting the preceding equation as a set of r independent equations, one for each polyphase. Polyphases (h^0 to h^r) are subsets of h and are generated by decimating h by the rate of r starting from the tap indicated by the polyphase index [8].

The equation for the first polyphase, for example, is written as:

$$y_0 = X_1 h_1^0 + X_2 h_2^0 + \cdots + X_m h_m^0 + b_0 + e_0 \quad (11)$$

Linear filters for the input, higher-order harmonics, and the periodic offset are derived by applying Least Squares Estimation to the above equation. This reduces the size of the matrices by a factor r (a factor of r^2 for X^TX) and significantly speeds up the matrix inversion required to obtain the solution.

3.3 Length of Simulation

Short random input sequences result in optimistic *SDR* values because such a sequence does not accurately reflect the statistical characteristics of the input data. In other words, a Least Squares Estimation solution is biased towards the finite-length input sequence used for the estimation. In order to measure this dependency we can estimate h using one random sequence, then use a new sequence and directly compute *SDR* using the previously estimated h. A discrepancy between these two *SDR* values indicates that the original input sequence is too short and estimation must be based on a longer sequence. It can be shown that the difference between these two *SDR* values linearly decreases with the observation length. In practice, the number of observation points should be increased until its dependence on the *SDR* value is no longer significant.

4. ADVANTAGES

Least Squares Estimation is a powerful technique to analyze the characteristics of a wideband system.

4.1 Impulse response and ISI

The h_1 vector calculated from Least Squares Estimation indicates the impulse response of the data converter. This response indicates the gain of the converter and describes its ISI.

Finding the linear response instead of relying on settling time measurements is advantageous for most communication systems. In such systems, even if the settling time requirements are not met, dispersion can be removed by the DSP module. Leaving ISI cancellation to the DSP module can significantly relax the specifications of the data converter.

4.2 Circuit bandwidth

The frequency response of h_1 is an indication of circuit bandwidth. For the case of the DAC, due to the zero-order hold nature of the circuit, the transfer function is shaped by a sinc function. In order to remove this effect, the 3-dB bandwidth is considered to be at the frequency where the transfer function departs from an ideal sinc function by 3-dB (Fig. 8).

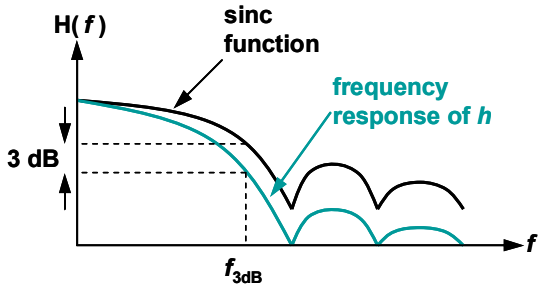

Figure 8: System bandwidth

4.3 Deterministic noise

Clock feedthrough, supply noise, and switching noise are three major sources of deterministic noise in data converters. Clock feedthrough is periodic by nature and supply noise has a strong cyclo-stationary nature at the clock period [9].

Figure 9 shows an example where switching noise from the common-source of differential pairs in a current DAC produces nonlinearity at the output. This switching directly corrupts the output and also injects data-dependent noise into the bias line of the tail current sources through parasitic gate-drain capacitances of the devices used for the current source. Switching noise is dependent on data transitions, and is not necessarily periodic. However, it has a non-zero mean which is strongest at transition points.

The magnitude of such noise sources can be calculated using the b vector derived from polyphase characterization. This number helps optimization of currents, and reduction of noise.

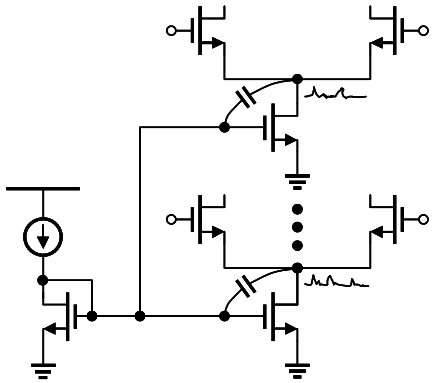

Figure 9: Deterministic switching noise in a current DAC

4.4 Decomposition of nonlinearities

Decomposition of nonlinearities into higher-order harmonics, signal independent sources, and offset identifies sources of nonlinearity and eases the optimization of the circuit. Linear vectors such as h_2 and h_3 demonstrating higher order harmonics can be correlated with measures such as IP_2, IP_3 derived from narrowband inter-modulation techniques. Such nonlinear terms can also be compensated for by the DSP.

4.5 Combination with linear filters

This technique provides a means of simulating the entire signal path of the circuit along with any other linear operation. Any linear filter can be modeled with a vector (w). The estimation can be performed using the convolution of h and w. In fact the entire communication path from transmitter input to the channel output can be characterized using this technique (Fig. 10). A precise characterization of a transistor-level data converter using the approach described here can provide all the metrics required for a detailed high-level simulation.

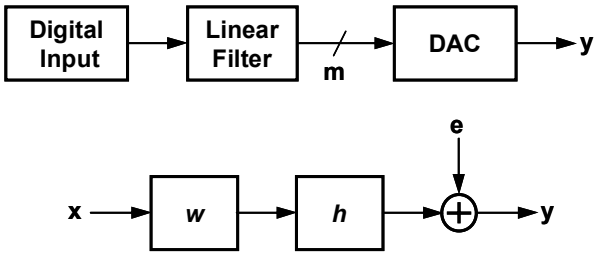

Figure 10: Combination of the DAC and a linear filter

5. SIMULATION RESULTS

The technique was applied to a binary-weighted 8-bit DAC. Shown in Fig. 11, the DAC operation is based on current summation. The circuit was designed in a 90-nm CMOS process and operates at the rate of 6 Gb/s.

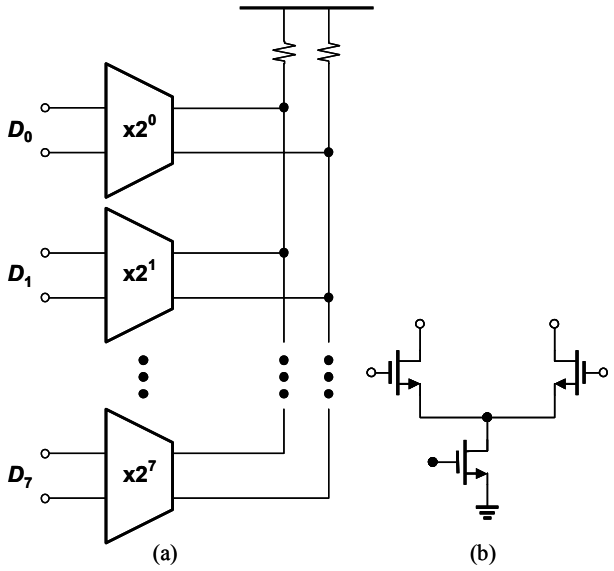

Figure 11: (a) An 8-bit, current DAC, (b) each segment

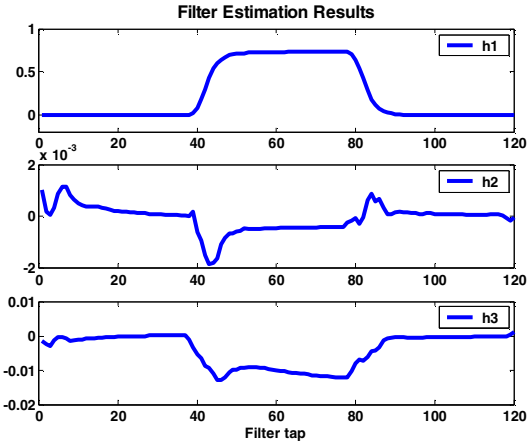

Figure 12: h_1, h_2, and h_3 vectors

The circuit achieved an overall linearity of 39 dB. Figure 12 shows h_1, h_2, and h_3. Note than h_2 is relatively small because the circuit is differential. Figure 13 depicts the periodic noise that is mostly a result of input data switching.

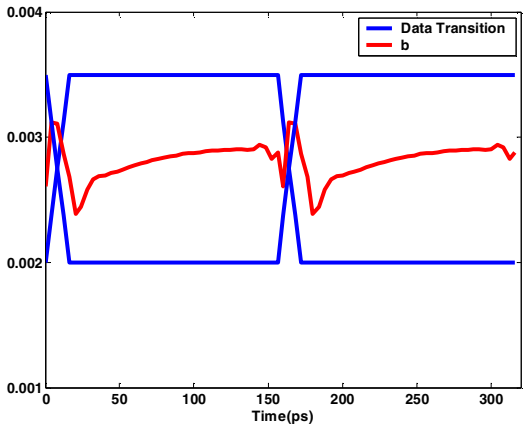

Figure 13: b vector

6. CONCLUSION

Standard characterization techniques are mostly defined for use with narrowband signals and fail to provide all the required metrics for a wideband system. In this paper a new technique based on Least Squares Estimation was proposed. This technique characterizes the system at full speed using a wideband random data. The technique proves to be powerful for analysis of higher-order harmonics, periodic disturbances, and mismatches. The approach also provides a very precise model of the circuit to be used by high-level simulators.

7. REFERENCES

[1] Walt Kester, *High-Speed Design Techniques,* Analog Devices, 1996.

[2] M. Vanden Bossche, J. Schoukens, J. Reenneboog, *Dynamic Testing and Diagnostics of A/D Converters*, IEEE Journal of Solid State Circuits, August 1996

[3] B. Razavi, *RF Microelectronics*, Prentice Hall, 1998

[4] N. Giaquinto, A. Trotta, *Fast and Accurate ADC Testing Via an Enhanced Sine Wave Fitting Algorithm*, IEEE Transactions on Instrumentation and Measurement, August 1997

[5] S. Boyd and L. Vandenberghe, *Convex Optimization*, Cambridge University Press, 2003

[6] A. Zhu, J. Dooley, and T. J. Brazil, *Simplified Volterra Series Based Behavioral Modeling of RF Power Amplifiers Using Deviation Reduction*, Digest of IEEE Microwave Symposium, June 2006

[7] S. Chan, T. Stathaki, A. Constantinides, *Adaptive Weighted Least Squares Algorithm for Volterra Signal Modeling*, IEEE Transactions on Circuits and Systems, April 2000

[8] P. P. Vaidyanathan, *Multirate systems and filter banks,* Prentice Hall, Englewood Cliffs, 1993

[9] E. Alon, V. Stojanovic, M. Horowitz, *Circuits and Techniques for High-Resolution Measurement of On-Chip Power Supply Noise*, IEEE JSSC, April 2005