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A New Technique of Interconnect Effects Equalization by using Negative Group Delay Active Circuits

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1. Introduction

During the last two decades, technological progresses in VLSI process have brought an outstanding development of information technology equipments and thus a great increase in the use of communication services all over the world. As reported by both the International Technology Roadmap for Semiconductors (ITRS) and the Overall Roadmap Technology Characteristics (ORTC), the exponential reduction of the feature size of electronic chips according to Moore's law (Moore, 1965) still occurs together with the exponential increase in time of the number of transistor per unit area. Combined to this shrinking of feature sizes, the on-chip clock frequency increases continually and should exceed 10 GHz in 2010. These ceaseless trends in VLSI circuits have led to more and more complex interconnect systems, and thus, the implementation of metal multi-layers for intra-chip interconnects has become a must. In the mid-1980's, the devices were, thus, composed of one or two layers of aluminium; in 2011, according to ITRS prediction, chips will consist of more than ten layers of copper.
Under these conditions, owing to the higher operation speeds, the interconnect propagation delay becomes more and more significant and dominates considerably the logic propagation delay (Deutsch, 1990; Rabay, 1996). Because of the sensitivities of parametric variations, clock and data flow may not be synchronized (Friedman, 1995). This explains why interconnections are so important in the determination of VLSI system performances. Besides, simplified models are worth being considered in order to reduce the complexity of any study on interconnects. Since the beginning of the 1980s the modelling of propagation delay in order to estimate the delay of an interconnect line driven by a CMOS gate has been the subject of numerous papers (Sakurai, 1983 and 1993; Deng & Shiau, 1990). The simplest and most used model of this delay was proposed by Elmore in 1948; it relies on the use of only an RC-line model. Nevertheless, due to the elevation of system data rates, this model tends to be insufficiently accurate. Therefore, more accurate models that sometimes take into account the inductive effect (Wyatt, 1987; Ismail et al., 2000) have been proposed.

To solve the problem of clock skew and propagation delays, a technique of signal integrity enhancement based on repeater insertion was proposed by different authors (Adler and Friedman, 1998; Ismail & Friedman, 2000). But, when the signals are significantly attenuated, such a solution may be unable to conserve the data duration and thus, inefficient. These considerations drove us to recently propose a new technique for interconnect-effect equalization (Ravelo, Perennec & Le Roy, 2007a, 2008a, 2009 and 2009) through use of negative group delay (NGD) active circuits. As shown in Fig. 1, it consists merely in cascading these NGD circuits at the end of the interconnect line. The possibility of signal recovery with a reduction of signal rise/fall-, settling- and propagation-delays was theoretically demonstrated and evidenced through simulations in (Ravelo et al., 2007a, 2008a) and confirmed by experiments in (Ravelo et al., 2009).

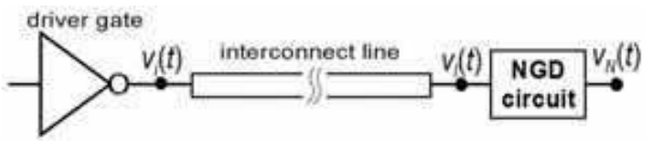


Fig. 1. Interconnect line driven by a logic gate ended by an NGD circuit.

In fact, evidences of the NGD phenomenon have been provided through theoretical demonstrations and experiments with passive-electronic devices (Lucyszyn et al., 1993; Eleftheriades et al., 2003; Siddiqui et al., 2004 and 2005) and active ones (Solli & Chiao, 2002; Kitano et al. 2003; Nakanishi et al., 2002; Munday & Henderson, 2004). As described in several physics domains (Wang et al., 2000; Dogariu et al., 2001; Solli & Chiao, 2002), in the case of a smoothed signal propagating in a device/material that generates NGD, the, the peak of the output signal and its front edge are both in time advance compared to the input ones. Then, confirmations that this counterintuitive phenomenon is not physically at odds with the causality principle have been provided (Wang et al., 2000; Nakanishi et al., 2002). A literature review shows that the first circuits that exhibited NGD at microwave wavelengths displayed also significant losses, whereas the baseband-operating ones were intrinsically limited to low frequencies. To cope with these issues, we, recently, reported on the design, test and validation through simulations and experiments of a new and totally integrable topology of NGD active circuit (Ravelo et al., 2007b, 2007c and 2008b); this topology relies on the use of a FET and showed its ability to compensate for losses at microwave frequencies over broad bandwidth. Transposition of this NGD topology to baseband frequencies allowed us to develop new structures that demonstrated their ability to simultaneously generate an NGD and gain for broad and baseband signals (Ravelo et al, 2008). Then, the idea put forward by Solly and Chiao (Solly, 2002) to compensate degradations introduced by passive systems such as interconnect lines by using NGD devices became possible.

As a continuation of these investigations, this chapter deals with further developments of this technique. Section 2 gives insight into the way this technique works, and briefly explains the role of the NGD circuit. The theory of interconnect modelling and the definition of the propagation delay are both recalled in Section 3. Analytical approach and experimental validations of RC-model equalization are presented in Section 4. The feasibility of the proposed technique, when the inductive effects are taken into account, is dealt in Section 5. In Section 6, a completely original and fully-integrable topology is proposed by

getting rid off inductance to cope with their implementation issue. Thus, the results of simulations, which provided a very good validation of the performances expected from theory, are analysed and discussed. A summary of this chapter is given in the last Section together with proposals about possible future developments.

2. The basic principle of the proposed compensation technique

Figure 2 illustrates the general case of the distortion undergone by a numerical signal degraded by the interconnect circuitry as introduced in Fig. 1. Compared to the input signal, $v_i(t)$, the degradation of the output one, $v_l(t)$, can be assessed from the signal attenuation as well as the rise-, fall- and settling-times and the 50% propagation delay. It is worth recalling that this last parameter, denoted here by $T_{p50\%}$ or merely T_p, is defined as the time needed by the output signal, v_l, to reach 50% of the unit-step input of amplitude, V_M, here. The delay required to reach 50% of the logic swing is traditionally referred as the delay time.

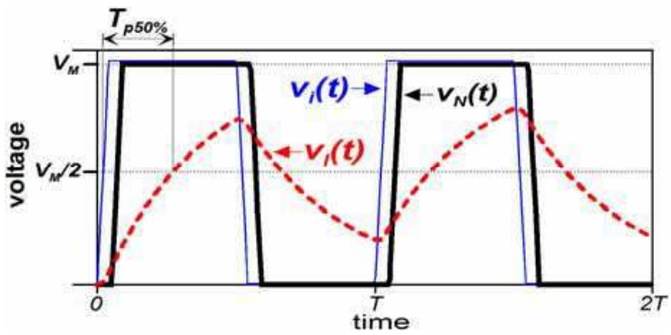


Fig. 2. Time-domain responses of the ideal system shown in Fig. 1 for a periodical input voltage, $v_i(t)$.

In frequency domain, the degradation between the input, v_i and the output, v_l corresponds to a transfer function denoted, $G_l(s)$ whose gain magnitude and group delay usually verify the following inequalities:

$$\left|G_l(j\omega)\right| < 1 \text{ and } \tau_l(\omega) = -\partial\angle G_l(j\omega)/\partial\omega > 0\,. \tag{1}$$

The output Laplace transform of this interconnect line can be written as:

$$v_l(s) = G_l(s)\,.\,v_i(s). \tag{2}$$

As shown by Figs. 1 and 2, this study was aimed at finding a relevant configuration or circuit able to provide a compensated output, v_N, (black thick curve) as close as possible to the input signal, v_i, (red dashed curve). It means that the following mathematical approximation can be made:

$$v_N(t) \approx v_i(t). \tag{3}$$

In theory, for well-matched circuits, the transfer system to be found, $G_x(s)$, must be associated to $G_l(s)$ so that equation (4) is verified:

$$v_N(s) = G_l(s).G_x(s).v_i(s) . \tag{4}$$

According to the circuit and system theory, through use of equations (3) and (4), one gets the adequate transfer function:

$$G_l(s).G_x(s).v_i(s) \approx v_i(s) \quad \Rightarrow \quad G_x(s) \approx 1/G_p(s) . \tag{5}$$

Consequently, in the frequency domain, the system gain and group delay must be such that:

$$G_x(j\omega)\big|_{dB} = -G_l(j\omega)\big|_{dB} , \tag{6}$$

$$\tau_x(\omega) = -\tau_l(\omega) . \tag{7}$$

So, on condition to take into account the condition expressed in equation (1), the gain and the group delay must be respectively such that $|G_x(j\omega)|_{dB} > 0$ and $\tau_x(\omega) < 0$. Technically, these conditions require the cascade of a system able to simultaneously exhibit Gain and an NGD in baseband. As described by the block diagram of Fig. 3, the whole cascaded system is characterized by its transfer function G(s) where G_l is the interconnect transfer function and $G_x = G_{NGD}$; τ is the whole group delay.

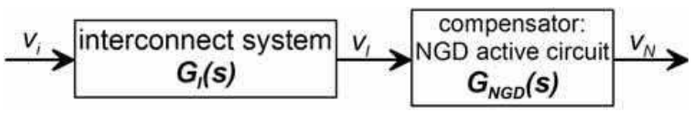


Fig. 3. Block diagram: interconnect passive system, $G_l(s)$ cascaded by the active NGD circuit, $G_{NGD}(s)$: $G(s) = G_l(s).G_{NGD}(s)$.

This process constitutes, then, a technological solution of equalization technique. In this case, the gain and group delay generated by the compensation system should be respectively the reverse and the opposite of those of the interconnect circuitry as depicted in Fig. 4. The principle of interconnect loss compensation and group delay reduction is illustrated in Fig. 4. At this stage, it is worth noting that the compensator must contain a system able to exhibit a group delay negative at base band frequencies not only with an opposite value of the interconnect one but also over the corresponding frequency band. A similar remark can be made about the gain compensation. The need for active circuits drove us to propose, here, a topology based on the use of a FET, chosen because of its biasing simplicity, the different models available (simple for analytical theory and more accurate ones for final simulations), its faculty to operate at tens of GHz as well as its easy integration.

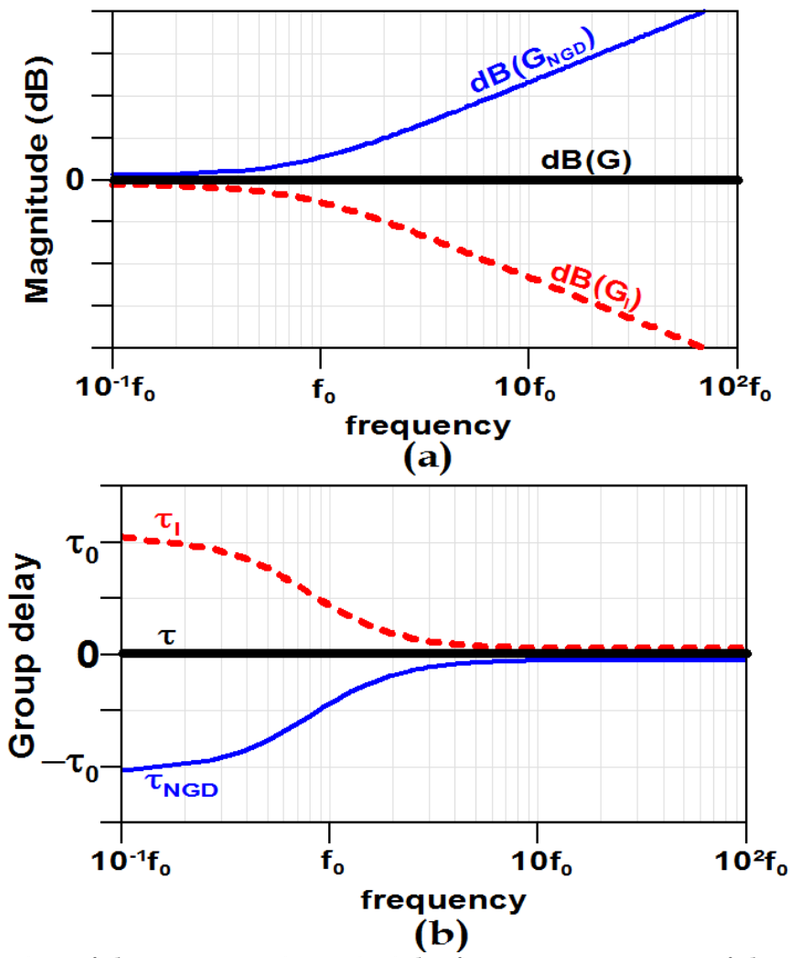


Fig. 4. Illustration of the compensation principle: frequency responses of the magnitude in dB (a) and group delay (b).

In conclusion, the NGD circuit consists in the achievement of a group delay and attenuation compensatory function. Fig. 4 depicts the compensation principle by considering the general frequency behaviour of interconnects or transmission lines. So, prior to conducting a feasibility study of this technique with concrete systems, let us briefly recall the theory on commonly used models of interconnects, i.e. RC- and RLC-circuits, and on propagation delay assessments.

3. Theory on the interconnect modelling and the propagation delay approximation

In most of microelectronic device interconnect models, the conductance effect can be neglected compared to the per-unit length resistance, R_l, the inductance, L_l, and the capacitance, C_l. Therefore, let us consider the interconnect structure presented in Fig. 5: it consists of an RLC-line model of length, d, driven by a gate with an output resistance, R_s. As previously mentioned, v_l is the circuit output voltage and v_i, the input one.

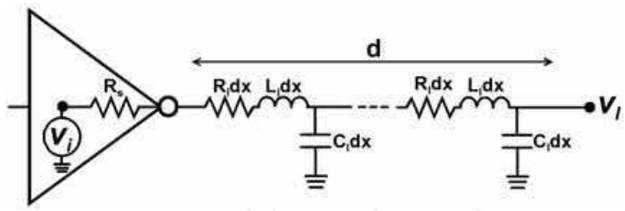


Fig. 5. A gate with output resistance, R_s, driving a RLC-model interconnect.

For the time-domain analysis of the structure under study, the input voltage, v_i, is assigned as a Heaviside unit step function, $\Gamma(t)$, of amplitude, V_M:

$$v_i(t)=V_M\Gamma(t). \tag{8}$$

As defined previously, the 50% propagation delay, T_p , is defined as the root of equation (9):

$$v_l(T_p) = V_M/2. \tag{9}$$

Before the calculation of this propagation delay, it is worth focusing on the system transfer function, which is defined as $G_l(s) = V_l(s)/V_i(s)$. It was established (Ajoy et al., 2004) that, according to the configuration of Fig. 5, this quantity is expressed as:

$$G_l(s) = \frac{1}{(1+sR_s)\cosh(\gamma d)+(R_s/Z_c)\sinh(\gamma d)}, \tag{10}$$

where

$$Z_c = \sqrt{(R_l + L_l s)/C_l s}, \tag{11}$$

and

$$\gamma = \sqrt{(R_l + L_l s)C_l s}, \tag{12}$$

are, respectively, the characteristic impedance and the propagation constant of the line. This transfer function is analysed through use of polynomial expansion as done for classical linear systems. For simplification, let us deal with the normalized transfer function, $g_l(s)$ which is determined by $G_l(s)/G_l(0)$, and that can be expressed by the m-order linear expression:

$$g_l(s) = \frac{1 + a_1 s + a_2 s^2 + ... + a_n s^n}{1 + b_1 s + b_2 s^2 + ... + b_m s^m}, \tag{13}$$

where the coefficients, a_i (i = {1,...,n}) and b_j (j = {1,...,m}) are real numbers, and m and n are integers. According to the literature (Elmore, 1948; Wyatt, 1987; Ismail et al., 2000), use of this expression allows one to estimate the 50% propagation delay expressed in equation (9). Among the existing approximation, it is worth recalling that the simplest and the most used in the industrial context is the one proposed by Elmore in 1948. It is based on the first-order consideration of equation (13). Indeed, this estimation of the propagation delay is merely defined by:

$$T_{pElmore} = b_1 - a_1. \tag{14}$$

One should note that this propagation delay is exactly equal to the group delay of the system under consideration at very low frequencies (Vlach et al. 1991). Nevertheless, this

formula has proven to become less and less accurate towards the elevation of the operating frequency. A new formula was proposed by Wyatt (Wyatt 1987): it differs from the previous approach by only the values of the coefficients, a_i and b_i, which are defined by the reciprocal of the dominant pole of the system transfer function:

$$a_1 = \sum_{i=1}^{n} z_i^{-1}, \tag{15}$$

$$b_1 = \sum_{i=1}^{m} p_i^{-1}, \tag{16}$$

where the real numbers, z_i and p_i, are, respectively, the zeros and the poles of $g_l(s)$. It is worth noting that this approach provides an exact expression of T_p in the case of the RC-model ($L_l = 0$).

3.1 Recall on RC-line model

It was established (Sakurai , 1983; Deng & Shiau, 1990) that the first-order approximation of the transfer function in equation (10) leads to the following expression:

$$G_l(s) = 1/\{1 + [(R_s + R_l d) + C_l d]s\} = G_{rc}(s). \tag{17}$$

This allows the modelling of the interconnect circuitry presented in Fig. 5 as a simple equivalent circuit (Fig. 6).

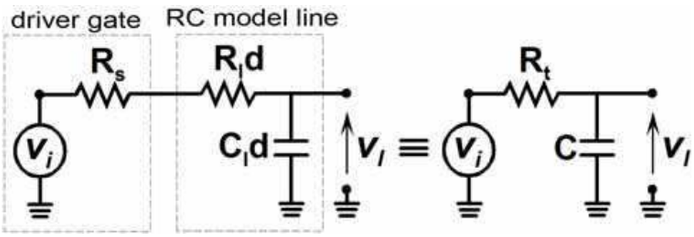


Fig. 6. Simplified representation of the structure shown in Fig. 5 by considering the first-order approximation of the transfer function.

Therefore, the driver gate loaded by the distributed transmission line can be equivalent to a lumped RC-circuit. To make easier the analytical calculation, let us consider the equivalent parameters of the system under study, $R_t = R_s + R_l d$ and $C = C_l d$. So, the Elmore propagation delay of this well-known circuit is given by:

$$T_{pRC} = R_t C. \tag{18}$$

But, it can be shown by calculation through the unit step response that the exact value of this quantity is expressed as:

$$T_{pRC} = R_t C \ln(2). \tag{19}$$

Then, the rise time, denoted t_{rRC}, which is defined as the time needed by the output signal to pass from 10% to 90% of the final output value, is written as:

$$t_{rRC} = R_t C \ln(9). \tag{20}$$

3.2 Summary on RLC-line theory

As previously mentioned, nowadays, interconnect line modelling requires, in most cases, to thoroughly consider the inductance effect. This parameter is usually taken into account through use of a second-order system, such as an RLC-network with the following canonical transfer function:

$$g_l(s) = \omega_n^2 / (s^2 + 2\zeta\omega_n s + \omega_n^2) . \quad (21)$$

where

$$\omega_n = 1/\sqrt{L_t C} , \quad (22)$$

and

$$\zeta = (R_t / 2)\sqrt{C / L_t} , \quad (23)$$

are, respectively, the undamped natural angular frequency and the damping ratio. From this second-order transfer function, an accurate propagation delay, T_{pd}, was established by Ismail & Friedman (2000):

$$T_p = (e^{-2.9\zeta^{1.35}} + 1.48\zeta) / \omega_n . \quad (24)$$

To reduce this propagation delay, and as first envisaged by Solli and Chiao (Solli et al, 2002), it could be worth cascading the interconnect line with an NGD active circuit. But a preliminary to this proposal is a detailed study of the resulting device in order to get a confirmation of the compensation principle efficacy. This will be the focus of the next Section.

4. Compensation of a first-order interconnect model (RC-circuit)

To compensate for interconnect spurious effects, especially losses and time delay, we recently developed and tested a new equalization technique based on the use of an NGD active circuit (Ravelo et al., 2007a, 2008a and 2009). In this section, we will briefly recall the theoretical fundamentals and validate the technique through experiments carried out in frequency- and time-domains in the case where a first-order circuit, i.e. an RC-circuit, is used to model the interconnect effects.

4.1 Theory

As explained above, the equalization principle consists in ending the circuit to be compensated, here an RC one, with an NGD active cell as depicted in Fig. 7. To simplify the analytical approaches, the FET is modelled by a controlled voltage current source with a transconductance, g_m, and the drain source resistance, R_{ds}.

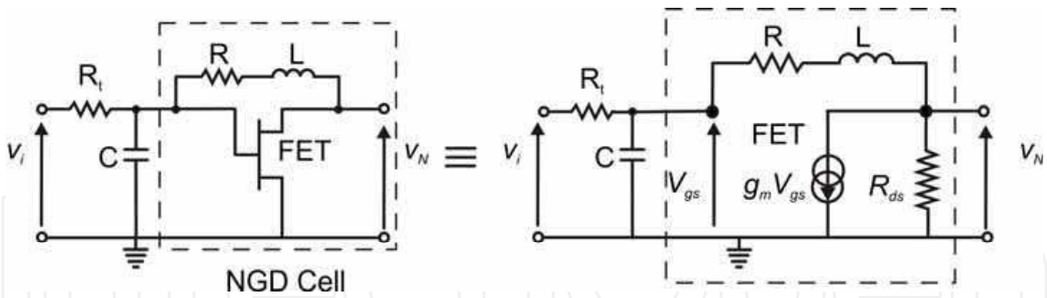


Fig. 7. RC-NGD circuit: RC-circuit cascaded with a basic cell of the NGD active circuit (FET in feedback with an RL series network) and the corresponding equivalent circuit.

In a first step, let us recall (Ravelo et al., 2007a, 2008a, 2008b, 2009) the transfer function and the group delay expressions of the NGD cell alone (in the dash box in Fig. 7) at low frequencies:

$$G_{NGD}(0) = \frac{(1 - g_m R) R_{ds}}{R + R_{ds}}, \tag{25}$$

$$\tau_{NGD}(0) = \frac{L(1 + g_m R_{ds})}{(R + R_{ds})(1 - g_m R)}. \tag{26}$$

On condition that:

$$1 - g_m R < 0, \tag{27}$$

the NGD cell exhibits a negative group delay ($\tau_{NGD}(\omega \rightarrow 0) < 0$) at very low frequencies.

Then, the transfer function and the gain at low frequencies of the whole RC-NGD circuit presented in Fig. 7 are, respectively, expressed as:

$$G(s) = \frac{R_{ds}(1 - g_m R) - g_m R_{ds} L s}{R + R_{ds} + R_t(1 + g_m R_{ds}) + \left[R_t C(R + R_{ds}) + L\right] s + R_t C L s^2}, \tag{28}$$

$$G(0) = \frac{R_{ds}(1 - g_m R)}{R + R_{ds} + R_t(1 + g_m R_{ds})}. \tag{29}$$

One should note that, because of the unmatched effect between the RC- and NGD-circuits, the transfer function, $G(s)$, is not equal to $G_{rc}(s).G_{NGD}(s)$ (Ravelo et al., 2009). The same remark applies to the group delays:

$$\left|G(j\omega)\right| \neq \left|G_{rc}(j\omega)\right|.\left|G_{NGD}(j\omega)\right|, \tag{30}$$

$$\tau(\omega) \neq \tau_{rc}(\omega) + \tau_{NGD}(\omega). \tag{31}$$

(i) Demonstration of the 50% propagation delay reduction:
From equations (18) and (28), the Elmore propagation delay (or the group delay at low frequencies) of the compensated RC-NGD circuit can be expressed as follows (Ravelo et al., 2008a):

$$T_p = \frac{[1 + g_m(R_t + R_{ds})g_m^2 R_t R_{ds}]L + T_{pRC}(R + R_{ds})(1 - g_m R)}{(R + R_t + R_{ds} + g_m R_t R_{ds})(1 - g_m R_{ds})}. \quad (32)$$

So, the delay is reduced ($T_p < T_{pRC}$,) on condition that:

$$L > (1 - g_m R)R_t^2 C / (1 + g_m R). \quad (33)$$

But this inequality is automatically verified if the condition expressed in equation (27) is true, i.e. if the active circuit generates NGD. According to this study, the optimum values of the NGD circuit can be synthesised as a function of the RC-values.

(ii) Synthesis of an NGD cell according to the RC-model values

As the aim of the equalization principle is the generation of an output signal equal or close to the input one, the transfer function magnitude and group delay should be, respectively almost equal to unity and null. For simplification purpose, let us apply these conditions at very low frequencies:

$$|G(0)| \approx 1 \text{ and } \tau(0) \approx 0. \quad (34)$$

From equations (31) and inversion of (29) and (32), one gets the synthesis relations expressed in equations (35) and (36):

$$R = [2R_{ds} + (g_m R_{ds} + 1)R_t]/(g_m R_{ds} - 1), \quad (35)$$

$$L = \frac{(g_m R - 1)(R + R_{ds})R_t C}{g_m^2 R_{ds} R_t + g_m(R_{ds} + R_t) + 1}. \quad (36)$$

These expressions are meaningful when the losses displayed by the interconnect are less than the maximal gain magnitude of an NGD cell, G_{max} :

$$G_{\max} = g_m R_{ds}. \quad (37)$$

Otherwise, several stages of NGD cells are needed to generate a whole gain of about unity; then, as reported in (Ravelo et al., 2008a), it is advised to use equation (38) for the calculation of the optimal number of cells, n:

$$n \approx 1 + \text{int}[-\ln(1 - e^{-T/(R_t C)})/\ln(G_{\max})]. \quad (38)$$

T is the time duration of the considered input square pulse. For a real x, the value of the greatest integer given by the function, $int(x)$, is equal to or lower than x. It is worth underlining that the implementation of, at least, two or an even number of transistors is preferable when the application under study requires avoiding signal inversion.

To validate these theoretical predictions, proof-of-concept (POC) circuits were designed, fabricated and measured in frequency- and time-domains as explained hereafter.

4.2 Experimental validations

The starting values of the NGD circuit come from the synthesis relations knowing the characteristics of the chosen FET and the RC-model values. Then, the most accurate available models were used to run simulations of the POC circuits on *ADS™* simulator software from *Agilent™* ; a sensitivity analysis was also performed. The different POC circuits presented in this section were implemented in hybrid planar technology (association of microstrip and surface mount chip/package components).

(i) Design Process

This demonstrator was aimed at illustrating visually the recovery of the degraded signal and the delay reduction. The circuits were designed and implemented separately; they consisted of an RC-circuit, an NGD-one and the combination of both into an RC-NGD circuit (Fig. 8(b)). To perform a broadband biasing and to avoid the eventual disruptions caused by the bias network at low frequencies, the FET was biased through an active-load technique.

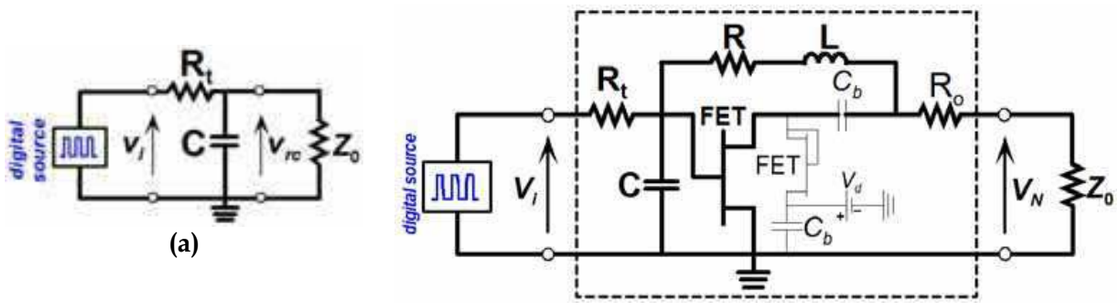


Fig. 8. Schematics of the (a) RC- and (b) RC-NGD-circuits (including the biasing network in thin lines) using a PHEMT FET (ATF-34143, V_{gs} = 0 V, V_d = 3 V, I_d = 110 mA), for R_t = 33 Ω, C = 680 pF, R = 56 Ω, R_o = 10 Ω, L = 220 nH, C_b = 100 nF and Z_0 is the output reference load.

The FET parameters required for the synthesis equations were extracted from the non-linear model and found to be g_m = 226 mS and R_{ds} = 27 Ω. For the RC circuit, the RL values of the NGD circuit were synthesised from equations (33) and (34). Then, accurate frequency responses were obtained through combination of circuit simulations (lumped components and non linear FET model) with electromagnetic co-simulations of the distributed parts by Momentum Software (from *Agilent™*). The values of the available lumped components were used in a final slight optimisation procedure. The layout of the hybrid planar circuit shown in Fig. 9 was printed on an 800-µm-thick FR4 substrate of relative permittivity, ε_r = 4.3; then the surface-mount chip passive components were set onto the substrate.

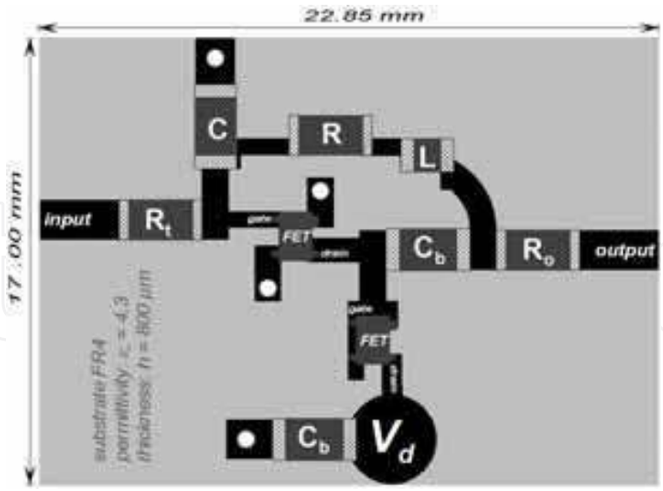
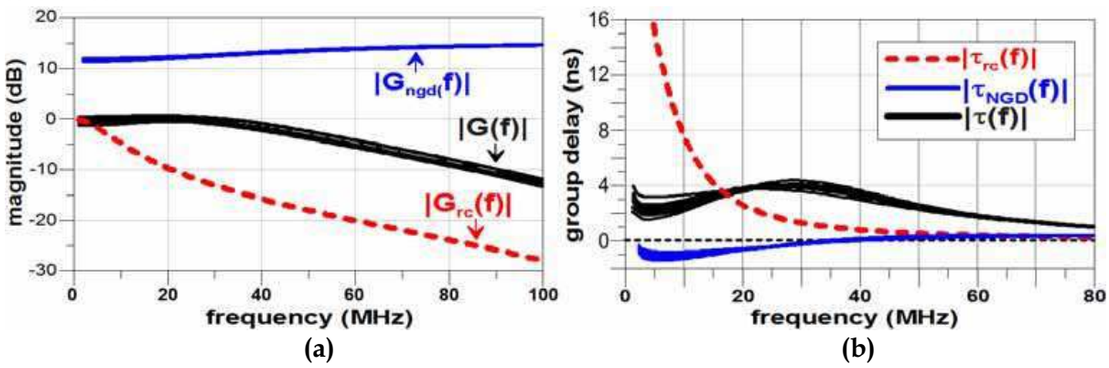


Fig. 9. Layout of the implemented RC-NGD circuit.

(ii) Simulation Results and Sensitivity Analysis

The simulations of the circuit pictured in Fig. 9 and of the RC and NGD ones were independently run in frequency- and time-domains under the specifications and conditions mentioned above. A sensitivity Monte-Carlo analysis over 10 trials was carried out on using tolerance values of ± 5% around their nominal values for the NGD elements (R = 56 Ω and L = 220 nH). All the results are presented in Figs. 10 and 11.

- Frequency-domain analysis: Fig. 10(a) shows that the magnitude $|G(f)|$ of the whole RC-NGD circuit is kept at about 0 dB up to 40 MHz, and the corresponding group delay $|\tau(f)|$ is, as expected, strongly decreased from DC to 15 MHz compared to that of the RC circuit. Moreover, the frequency responses are only slightly sensitive to lumped-component tolerance.



(a) **(b)**

Fig. 10. (a) Magnitude and (b) group delay frequency responses issued from simulations with a Monte-Carlo analysis of the NGD circuit elements R and L (± 5%).

- Time-domain analysis: It is worth underlining that, at first, the signal was measured at the output of a *Rhode & Schwarz Signal Generator SMJ 100A* at the highest available rate, i.e. 25 Msym/s, and then further used in simulations as the input signal. Then, excitation of the

simulated RC- and RC-NGD-circuits with this input square wave pulse (magnitude, V_M = 1 V) led to the time-domain simulation results presented in Fig. 11, where the dotted curve indicates the degradation induced by the RC-circuit alone; moreover, the signal recovery is evidenced by the thick black curve. It clearly appears that the compensation is significant, but incomplete. Because of the drain-source current inversion, the output signal is reversed compared to the input voltage. This is why the plot presented in Fig. 11 is that of -V_N.

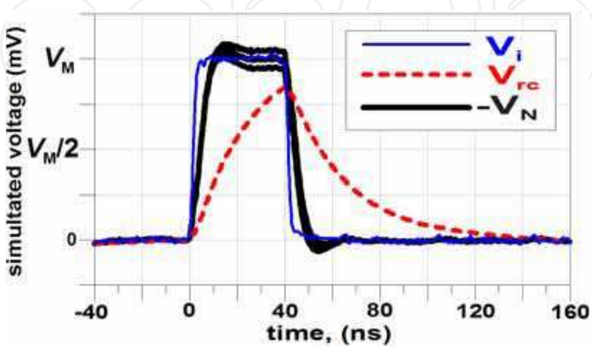


Fig. 11. Results of time-domain simulations (with a Monte Carlo analysis of the NGD circuit elements, R and L (± 5%)) for an input square wave pulse (V_M = 1 V with a 40 ns data duration).

It is worth noting that the 50% propagation delay is shortened from 16.5 ns (for the RC circuit) to about 3 ns (for the RC-NGD circuit), i.e. a relative reduction of, at least, 81%. A Monte-Carlo sensitivity analysis with a ± 5%-variation around the R and L nominal values showed nearly no change of the RC-NGD circuit output signal (including the front and leading edges), but the final value is somewhat slightly affected.

(iii) Measured results and discussions:
To check for the validity of the results of theoretical analysis and simulations, three circuits were fabricated and tested in both frequency- and time-domains.

- Frequency-domain results: These measurements were made with a vector network analyzer (*Rhode & Schwarz ZVRE 9kHz - 4GHz*), which provides the scattering matrix (S-parameters) of the devices under test. Then, the transfer function is calculated through use of the classical passage relationships in order to get the magnitude and the group delay (calculated from the transfer function phase response). The fabricated devices consisted of the single RC-circuit, the NGD one and a third one, denoted RC-NGD circuit, which combined both functions in order to avoid any connector mismatch liable to occur if the first two ones were simply cascaded. Figure 12(a) shows that the magnitude and group delay responses of the three circuits are in good agreement with the simulation results presented in Figs. 10. As expected from equations (30) and (31), the total magnitude and group delay values are different from those issued from the addition of the individual ones because of the existence of mismatch between the RC and NGD parts ($G_{RCNGD} \neq G_{RC}.G_{NGD}$). The measured magnitude, $|G(f)|_{dB}$, is close to 0 up to 40 MHz and gets down to -10 dB at 80 MHz.

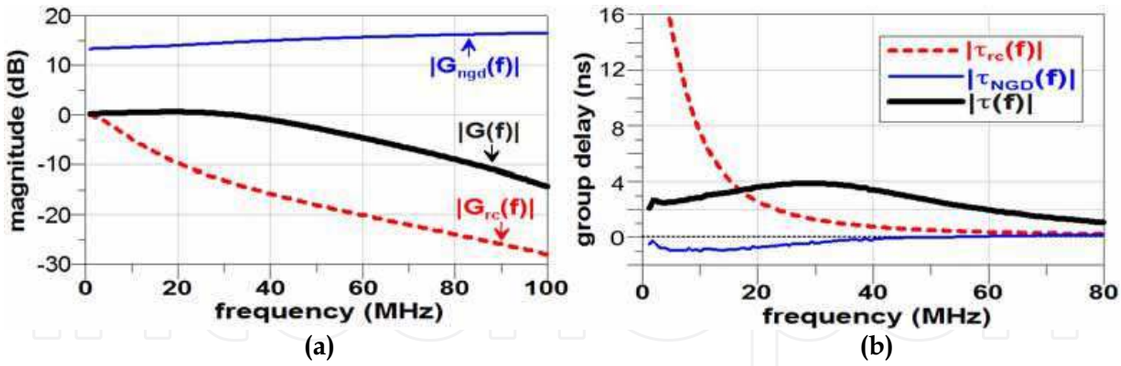


Fig. 12. Measurements of (a) magnitude and (b) group delay produced by the RC-, NGD- and RC-NGD-circuits.

One should note that, though the RC-NGD circuit group delay, $\tau(f)$, is not fully cancelled (Fig. 12(b)), it is strongly reduced below 20 MHz thanks to the NGD circuit; moreover, it is kept below 4 ns up to 80 MHz. In theory, a higher absolute value of NGD could be obtained, but a compromise between NGD value, NGD bandwidth and gain flatness has to be found to minimize the overshoot or the ripple in time-domain

- *Time-domain experimental results*: Throughout the time-domain simulations and measurements, the circuit load, Z_0, is set at a high impedance value (Z_0 = 1 MΩ).

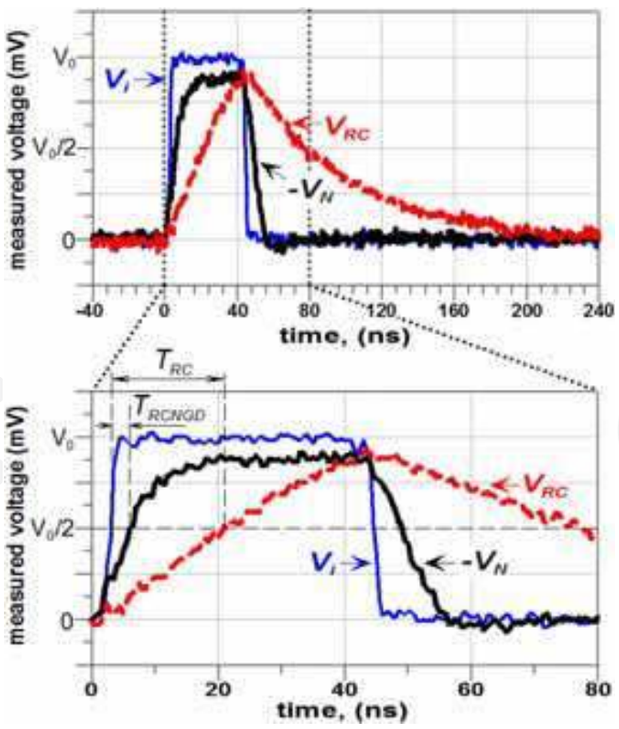


Fig. 13. Time-domain responses with an input square pulse (25-Msym/s rate, 2 ns rise- and fall-times) and zoom on twice the symbol duration.

A square wave input pulse of amplitude $V_M = 1$ V was delivered at a rate of 25-Msym/s (corresponding to a 40-ns data duration) by the baseband data output of an *R&S SMJ 100A* vector signal generator and recorded on a *2 Gs/s* LeCroy digital oscilloscope. The input pulse, V_i, was thus monitored as well as the output ones of the RC- and RC-NGD-circuits, V_{RC} and $-V_N$, prior to their resynchronization through use of the same reference signal. Figure 13 shows that the output leading edge provided by the RC-circuit is degraded and characterised by $t_{rRC} \approx 35$ ns as rise time and a 50% propagation delay of $T_{pRC} \approx 18.50$ ns. Compared to V_{RC}, the output waveform, $-V_N$, is reshaped and less distorted. Hence, the NGD circuit compensation allowed a reduction of both parameters down to $t_r \approx 10$ ns and $T_p \approx 2.50$ ns, that is relative reductions of 71.4% ($1-t_r/t_{rRC}$) and 86.5% ($1-T_p/T_{pRC}$), respectively. As shown in Fig. 13, the trailing edge is also strongly improved. This point is worth being noted in the case of an enhancement of the data rate.
The proposed interconnect equalization technique was validated through modelling of the interconnect line degradation by an RC-circuit, which is the most current model in use. However, in order to supplement this study, the inductive effects of interconnect lines will be taken into account in the next Section.

5. Equalization under conditions of interconnect line inductive effects

As underlined at the beginning of this chapter, the ceaseless increase of operating frequencies, the inductive effects can no longer be neglected in the modelling of interconnect systems. In this study, the line is modelled by the RLC network shown in Fig. 14(a) and driven by a logic gate with R_s as output resistance. In order to check whether the proposed compensation technique still works, let us consider the whole circuit presented in Fig. 14(b): it consists of the interconnect model cascaded by the compensation circuit, which is composed of a FET fedback by an RL-series network. To simplify the theoretical study, the FET is replaced by its low frequency equivalent-circuit model as introduced in Fig. 5. The terms, $R_t = R_s + R_l d$, $L_t = L_l d$ and $C = C_l d$, introduced in the previous study of the RC-network are still used.

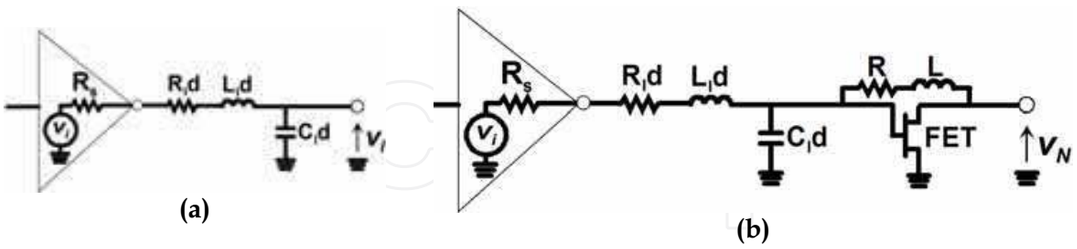


Fig. 14. (a) line model: RLC network driven by a logic gate with output resistance, R_s; (b) the whole circuit composed of the line model compensated by an NGD cell.

5.1 Theory

According to the procedure used in the previous section, the transfer function of the whole system is:

$$G(s) = R_{ds}[1 - g_m(R + Ls)]/(\alpha_0 + \alpha_1 s + \alpha_2 s^2 + \alpha_3 s^3), \quad (39)$$

where

$$\alpha_0 = R + R_t + R_{ds}(1 + g_m R_t), \quad (40)$$

$$\alpha_1 = R_t C(R + R_{ds}) + g_m R_{ds} L_t + L + L_t, \quad (41)$$

$$\alpha_2 = [LR_t + L_t(R + R_{ds})]C, \quad (42)$$

$$\alpha_3 = LL_t C. \quad (43)$$

Then, at very low frequencies ($\omega \rightarrow 0$), the corresponding gain, G(0), and the Elmore propagation delay, T_p, are respectively expressed as:

$$G(0) = [R_{ds}(1 - g_m R)]/[R + R_t + R_{ds}(1 + g_m R_t)], \quad (42)$$

$$T_p = \frac{(g_m R - 1)[R_t C(R + R_{ds}) + L_t(1 + g_m R)] - (1 + g_m R_{ds})(1 + g_m R_t)}{[R + R_t(1 + g_m R_{ds}) + R_{ds}](g_m R - 1)}. \quad (43)$$

Application of the equalization objectives expressed in (32) to equations (42) and (43) allows one to extract the following synthesis relations:

$$R = [2R_{ds} + (g_m R_{ds} + 1)R_t]/(g_m R_{ds} - 1), \quad (44)$$

$$L = (g_m R - 1)[(R + R_{ds})CR_t + (1 + g_m R_{ds})L_t]/[g_m^2 R_{ds} R_t + g_m(R_{ds} + R_t) + 1]. \quad (45)$$

To evidence the relevance of this RLC effect equalization, simulations under realistic conditions were run.

5.2 Validations by simulations

In order to solve the problem of the output voltage sign and to take into account inductive effects, a two-stage NGD circuit was simulated through use of *ADS™* for two types of interconnect lines models: i) a model with lumped RLC elements and an input signal of 1 ns in data duration, and ii) an RLC distributed line and an input signal of 5-ns data duration. Moreover, using two NGD cells allows widening the NGD frequency bandwidth (Ravelo et al, 2007c) and thus, input signals with higher data rates and smaller rise-/fall-times can be considered.

(i) Compensation of a lumped RLC-circuit for an input signal with 1 ns-data duration

Fig. 15 depicts the whole compensated RLC-NGD circuit under study. It consists in a lumped RLC-circuit ended with a two-stage NGD active circuit. The FETs used by the latter (EC-2612 with g_m = 98.14 mS and R_{ds} = 116.8 Ω) are from *Mimix Broadband™*.

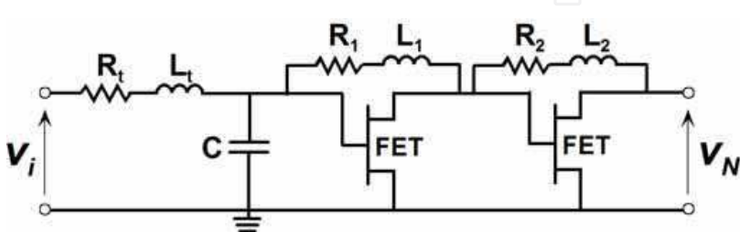
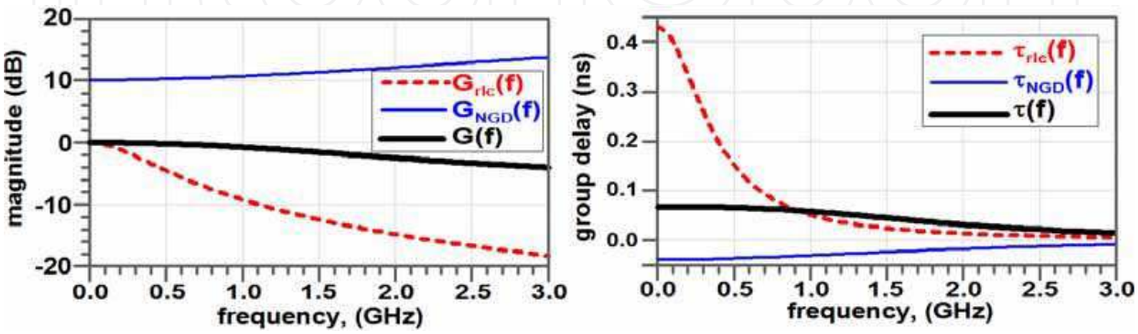


Fig. 15. Two-stage NGD active circuit compensating the RLC network (R_t = 100 Ω, L_t = 6 nH, C = 4.3 pF, R_1 = 86 Ω, R_2 = 89 Ω, L_1 = 5.2 nH, L_2 = 2.6 nH and FET/EC-2612).

One should note that the time- and frequency-domain results presented here were obtained by using the FET linear model provided by this manufacturer and recorded at the biasing point V_{ds} = 3 V and I_{ds} = 25 mA.

- Frequency-domain results: Figs. 16 (a) and (b) present the magnitudes and the group delays of the RLC- and NGD-circuits separately, and then, both cascaded (noted RLC-NGD), as depicted in Fig. 15. Fig. 16(a) shows that the transfer-function magnitude of the overall circuit (black thick curve) is kept within -4 and 0 dB up to 3 GHz.



(a) **(b)**

Fig. 16. Simulated frequency responses of the RLC, NGD and RLC-NGD circuits: (a) magnitude and (b) group delay.

Once again, one should note that the value of this whole transfer-function magnitude is different from the sum (in dB) of the individual magnitudes ($G_{RLCNGD} \neq G_{RLC}.G_{NGD}$) because of mismatch between both parts. Figure 16(b) evidences that, thanks to the NGD effect (thin blue curve), the total group delay of the whole circuit (black thick curve) is less than 68 ps. A comparison of the group delays respectively produced by the RLC and the RLC-NGD circuits shows a significant reduction up to about 0.8 GHz with the latter.

- Time-domain results: Figure 17 presents the results of transient simulations run in the case of a 2-ns periodic input signal, V_i, whose rise-/fall-times are about 92 ps (thin red curve). The response at the output of the RLC circuit alone, V_{RLC}, is depicted by the degraded dashed curve, and the corresponding 50% propagation delay, T_{pRLC}, is equal to 304 ps. Further to the insertion of the NGD circuit, the black thick curve representative of $V_{N,}$ i.e. at the output of the RLC-NGD circuit, shows improvement with a relative reduction of more than 85% of propagation delay since T_p is about 44 ps. Moreover, by comparison to $V_{i,}$ V_N presents neither attenuation, nor overshoot, and the leading and trailing edges are both improved.

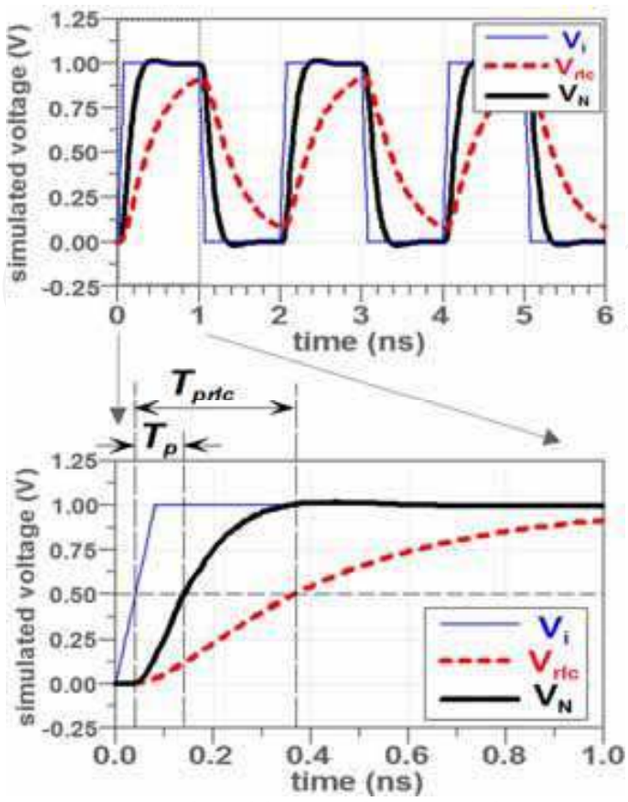


Fig. 17. Time-domain responses produced by simulations of the circuit in Fig. 15 for a 2-ns periodic trapezoidal input, rise-/fall-times, t_r = 92 ps and 50%-duty ratio with zoom on a half-period (bottom).

As the accuracy of the lumped RLC model of interconnect line used in these simulations might be insufficient for certain VLSI configurations, the simulation described in the next paragraph dealt with a distributed RLC-model (Ravelo et al, 2007a).

(ii) Compensation of a distributed RLC-line in the case of an input signal of 5-ns data-duration

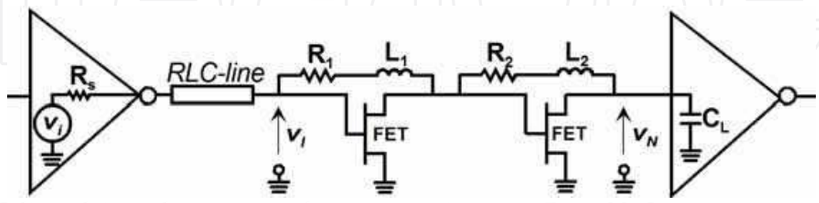
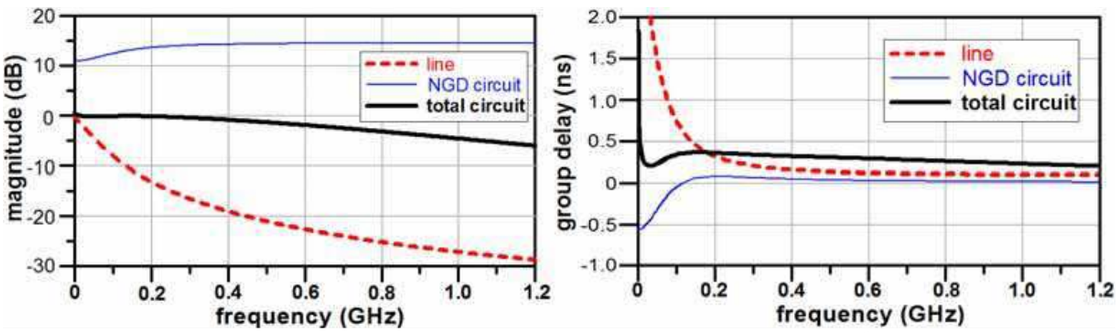


Fig. 18. RLC-line driven by a gate of output resistance, R_s = 90 Ω, compensated by a two-stage NGD circuit (FET/EC-2612, R_1 = 73 Ω, L_1 = 99 nH, R_2 = 102 Ω and L_2 = 17 nH) loaded by another gate of input capacitor C_L = 30 pF.

Fig. 18 shows the circuit under study; the interconnect line is modelled by an RLC distributed circuit. The classical RLC-line is driven by a gate of output resistance, R_s,

compensated by a two-stage NGD circuit loaded with another gate of input capacitor, C_L. The transmission line parameters were taken from ITRS roadmap so that R_l = 76 Ω/cm, L_l = 5.3 nH/cm and C_l = 2.6 pF/cm for a 0.8-cm-long line. For these values, the synthesis relations were used together with an optimization process to get an output, V_N, close to the input, V_i. Finally, the component values for the two NGD cells were: R_1 = 73 Ω, L_1 = 99 nH, R_2 = 102 Ω and L_2 = 17 nH.

- Frequency-domain results: Figs. 19(a) and (b) respectively show the transfer function magnitude and the group delays produced by simulations of the three circuits (RLC-line, NGD- and RLC-NGD-circuits). In Fig. 19(a), the important attenuation displayed by the RLC-line is compensated by the NGD cells so that the total gain is kept at about 0 dB up to about 500 MHz. With respect to the group delay produced by the RLC-line, the one by the RLC-NGD circuit (thick black curve) is strongly reduced as expected thanks to the NGD contribution (thin blue curve). Indeed, at baseband frequencies, this latter provides a minimal NGD value around -0.5 ns.



(a) **(b)**

Fig. 19. Frequency responses produced through simulations of the RLC-, NGD-, and RLC-NGD circuits shown in Fig. 18: magnitude (a) and group delay (b).

- Time-domain results: Time-domain simulations were run on using at the input a 10-ns-period signal with 0.60 ns as rise-/fall-times.

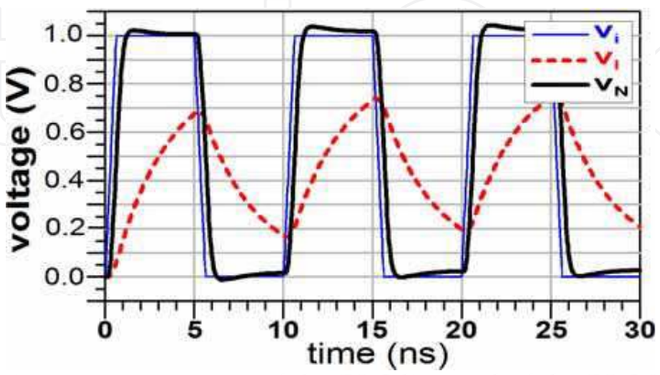


Fig. 20. Time domain output responses of the RLC-line and of the RLC-NGD compensated structure for a trapezoidal input voltage at a 200 Mbit/s rate.

Fig. 20 evidences a marked degradation of the output waveform, V_l, of the RLC-line compared to the input waveform. Once again, the insertion of the NGD active circuit allows great enhancement illustrated by a notable signal regeneration, a reduction of the propagation delay of about 1.60 ns (from 1.86 ns to 0.26 ns) accompanied with an enhancement of the signal leading- and trailing-edges. These results confirm the efficacy and the reliability of this technique to equalize the degradation induced either by lumped or distributed RLC-model of interconnect lines.

6. Improvement of the NGD topology toward an integration process

Application of these innovative cells to the compensation of VLSI interconnect-induced degradation requires compatibility with VLSI integration process. So, here, the main issue is the integration and manufacturing of inductive elements such as the inductance of the FET feedback and the biasing Inductance (choke self with a high value). The latter can be replaced with, for example, an active bias which, moreover, provides a possibility of operating bandwidth enhancement. To get rid of the feedback inductance, let us consider a new topology of NGD active circuit with no inductance. It simply consists of a FET cascaded with a shunt RC-network. To match the cell output to the following stage input, an R_2 resistor is connected in shunt at its end. As described in Fig. 21, this new topology is cascaded at the end of an RC circuit, which models the interconnect line to be compensated.

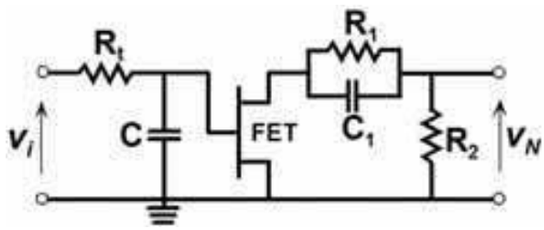


Fig. 21. RC-circuit compensated by a NGD cell without inductance.

Let us focus, at first, on the analytical study of the proposed cell according to the RC circuit values prior providing evidence, through simulations, of the compensation of the RC effects, i.e. signal recovery and delay reduction, by using the proposed NGD topology

6.1 Theory

According to (Ravelo et al, 2008), the transfer function of the RC-NGD device described in Fig. 21 is:

$$G(s) = \frac{-G_{max} R_2 (1 + R_1 C_1 s)}{(1 + R_t C s)[R_1 + R_2 + R_{ds} + R_1 C_1 s (R_2 + R_{ds})]}, \tag{48}$$

where G_{max} is the maximal gain value expressed in equation (37). The minus sign is explained by the intrinsic FET model, which entails naturally the inversion of the output voltage direction compared to the input one. Otherwise, with the same approach as in Section 4.1, from this transfer function it can be established that the gain at very low frequencies and the Elmore propagation delay are given by:

$$G(0) = \frac{-G_{max}R_2}{(R_1 + R_2 + R_{ds})}, \tag{49}$$

$$T_p = \frac{[(R_2 + R_{ds})T_{pRC} - R_1C_1(R_t + R_1)]}{(R_1 + R_2 + R_{ds})}. \tag{50}$$

From expression (49), loss compensation ($|G(0)| > 1$) is effective on condition that the following condition between G_{max} and the resistance values be met:

$$G_{max} > 1 + \frac{R_1 + R_{ds}}{R_2}. \tag{51}$$

In addition, from expression (50), it can be found that, whatever the values of the RC- and the NGD-circuit parameters, T_P is always lower than T_{pRC}. In other words, the RC-propagation delay is always reduced in the configuration of Fig. 21. At this stage, it is worth pointing out that equation (50), despite its usefulness, is an approximation of the 50% propagation delay as proposed by Elmore. Indeed, according to Ismail and Friedman, a relative inaccuracy of about 30% is possible. Another limitation appears when the following condition is satisfied:

$$R_tC < \frac{R_1C_1(R_t + R_1)}{R_2 + R_{ds}}. \tag{52}$$

In this case, expression (50) provides a negative value for T_p, which leads to an unrealistic behaviour that would contradict the causality principle. Indeed, calculation of the exact expression for T_p from the root of the equation, $v_N(T_p) = V_M/2$, gives always a positive value for the total propagation delay.
Despite these restrictions, equations (49) and (50) are particularly useful for a first analytical approximation and permit the extraction of the synthesis relations needed to determine the values of the NGD cell components:

$$R_1 = R_2(G_{\max} - 1) - R_{ds}, \tag{53}$$

$$R_2 = (R_1 + R_{ds})/(G_{\max} - 1), \tag{54}$$

and by using the equation, $\tau(0) \approx 0$:

$$C_1 = CR(R_1 + R_2 + R_{ds})/R_1^2. \tag{55}$$

The synthesis relations (53) and (54) are physically realistic under the following conditions:

$$G_{\max} > 1, \tag{56}$$

$$R_2 > R_{ds}/(G_{\max} - 1). \tag{57}$$

6.2 Discussion on the simulation results

The previous synthesis relations were used to design and simulate, with *ADS* software, the circuit presented in Fig. 22(a). The thin lines indicate the DC bias network. The RC-circuit is compensated by a two-stage NGD circuit, and the whole circuit is excited at the rate of 1 Gbit/s by an input signal, V_i, with rise and fall times of about 0.2 ns.

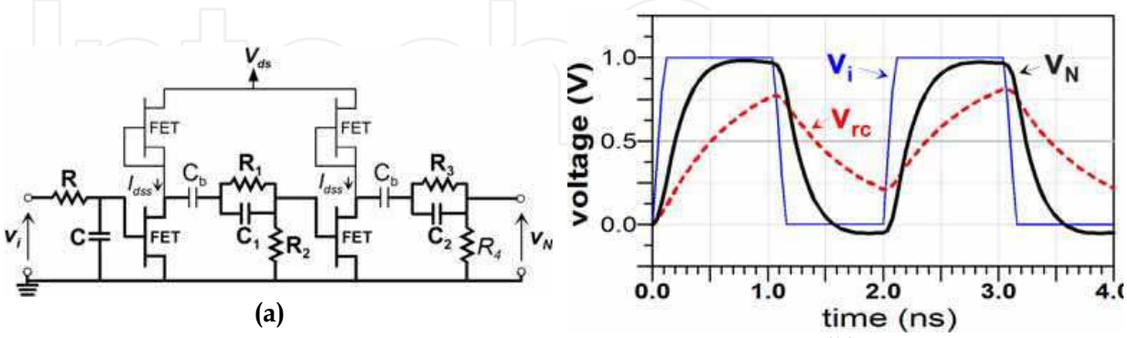


Fig. 22. (a): The whole circuit composed of an RC-model compensated by a two-stage NGD circuit in active biasing; FET (EC-2612, V_d = 3 V, I_{ds} = 30 mA), R = 68 Ω, C = 10 pF, R_1 = 142 Ω, R_2 = 32 Ω, C_1 = C_2 = 10 pF, R_3 = 100 Ω, R_4 = 51 Ω and (b) the corresponding simulation results.

An active load bias with the same FETs (EC-2612) was applied to the circuit. No inductance element is needed in this circuit. Transient simulations run with ideal components gave the results displayed on Fig. 22(b). Once again, the comparison of the RC- and RC-NGD-outputs highlights a signal recovery, characterised by a gain of about 1.85 dB at $t = T/2$ and a reduction of propagation from $T_{pRC} \approx 47$ ps to $T_p \approx 12$ ps or $\Delta T/T_{pRC} \approx 74.4\%$ in relative value. Time-domain measurements are scheduled and will indicate if further improvements are required prior to the integration in a final VLSI device.

7. Conclusion and future works

A novel and innovative technique of interconnect effect equalization in electronic systems was developed through theoretical studies and experimentally validated. It relies on the use of active circuits able to simultaneously generate gain and negative group delay in baseband over broad bandwidth.

The properties of these circuits were used to propose a new compensation approach consisting in an equalization of both the positive group delay and attenuation induced by interconnects by an equivalent negative group delay and gain.

The theory on commonly used circuits to model interconnect effects were briefly recalled. Then, a circuit composed of a first-order interconnect model (i.e. an RC-circuit) cascaded with an NGD cell was theoretically studied in order to determine the conditions required to compensate for both the degraded propagation delay and the attenuation and to express the synthesis relations to be used in the determination of the values of the NGD cell components. This NGD cell simply consists in a FET fedback by an RL series network. Then, for this first modelling of interconnect line, a proof-of-concept circuit implemented in hybrid planar technology was fabricated to demonstrate the efficiency of this technique. The

experimental results in frequency- and time-domains were in very good agreement with simulations and validated the compensation technique in the case of an input signal with a 25 Mbit/s data rate. Indeed, the reductions of the rise time and the 50% propagation delay were 71 and 86%, respectively.
In many VLSI systems and particularly in long wires and/or for high data rates or clocks, the inductive spurious effects can no longer be neglected. So, a more elaborated system composed of an RLC interconnect model compensated with NGD cells was also studied analytically in order to check for the validity and efficacy of the equalization technique and to determine the synthesis relations to be used in further applications. To validate the approach, a first series of simulations was run with an RLC lumped model for an input signal at 1 Gbits/s-rate; then , the model used in the second set of simulations was an RLC distributed line for an input signal at a rate of 200 Mbit/s. These simulations under realistic conditions confirmed the compensation approach with reduction of the propagation delay of the same order as previously. Moreover, as observed with the RC-model, the front and trailing edges both showed great enhancements indicative of a good recovery of the signal integrity.
Finally, to be able to compensate for interconnect effects in VLSI systems, the proposed circuits must be compatible with a VLSI integration process. This requirement drove us to propose improvements of the proposed topology in order to cope with inductance integration and manufacturing prerequisites. So, a topology with no inductance, but with the same behaviour and performances as previously was proposed. A theoretical study provided evidence of its ability to exhibit a negative group delay in baseband together with gain. Then, time-domain simulations of a two-stage NGD device excited by a 1 Gbits/s-rate input signal were run to validate the expected compensation approach and check for the signal recovery.

The implementation of this equalization technique in the case of a VLSI integration process is expected to allow compensation for spurious effects such as delay and attenuation introduced by long inter-chip interconnects in SiP and SoC equipments or by long wires and buses. A preliminary step would be the design and implementation of such a circuit in MMIC technology and especially by using distributed elements. At this stage, even if experimentally the NGD cells were not particularly sensitive to noise contribution, it would be worth comparing this approach and repeater insertion under rough conditions, i.e. long wires with a significant attenuation, in order to gain key information on their respective behaviour under conditions of significant noise. As identified in ITRS roadmap, the power consumption is now one of the major constraints in chip design and has been identified as one of the top three overall challenges over the last 5 years. Faced to these constraints, further investigations are needed to accurately evaluate the consumption of the presented NGD active circuits.

8. References

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VLSI

Edited by Zhongfeng Wang

ISBN 978-953-307-049-0

Hard cover, 456 pages

Publisher InTech

Published online 01, February, 2010

Published in print edition February, 2010

The process of Integrated Circuits (IC) started its era of VLSI (Very Large Scale Integration) in 1970's when thousands of transistors were integrated into one single chip. Nowadays we are able to integrate more than a billion transistors on a single chip. However, the term "VLSI" is still being used, though there was some effort to coin a new term ULSI (Ultra-Large Scale Integration) for fine distinctions many years ago. VLSI technology has brought tremendous benefits to our everyday life since its occurrence. VLSI circuits are used everywhere, real applications include microprocessors in a personal computer or workstation, chips in a graphic card, digital camera or camcorder, chips in a cell phone or a portable computing device, and embedded processors in an automobile, et al. VLSI covers many phases of design and fabrication of integrated circuits. For a commercial chip design, it involves system definition, VLSI architecture design and optimization, RTL (register transfer language) coding, (pre- and post-synthesis) simulation and verification, synthesis, place and route, timing analyses and timing closure, and multi-step semiconductor device fabrication including wafer processing, die preparation, IC packaging and testing, et al. As the process technology scales down, hundreds or even thousands of millions of transistors are integrated into one single chip. Hence, more and more complicated systems can be integrated into a single chip, the so-called System-on-chip (SoC), which brings to VLSI engineers ever increasingly challenges to master techniques in various phases of VLSI design. For modern SoC design, practical applications are usually speed hungry. For instance, Ethernet standard has evolved from 10Mbps to 10Gbps. Now the specification for 100Mbps Ethernet is on the way. On the other hand, with the popularity of wireless and portable computing devices, low power consumption has become extremely critical. To meet these contradicting requirements, VLSI designers have to perform optimizations at all levels of design. This book is intended to cover a wide range of VLSI design topics. The book can be roughly partitioned into four parts. Part I is mainly focused on algorithmic level and architectural level VLSI design and optimization for image and video signal processing systems. Part II addresses VLSI design optimizations for cryptography and error correction coding. Part III discusses general SoC design techniques as well as other application-specific VLSI design optimizations. The last part will cover generic nano-scale circuit-level design techniques.

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