A New Type of STATCOM Based on Cascading Voltage-Source Inverters with Phase-Shifted Unipolar SPWM

Yiqiao Liang, *Member, IEEE*, and C. O. Nwankpa, *Member, IEEE*

***Abstract*— In this paper, a new type of static compensator (STATCOM) is proposed. This new STATCOM is constructed by cascading several identical full-bridge (H bridge) voltage-source inverters (VSI's). A so-called phase-shifted sinusoidal pulsewidth modulation (SPWM) unipolar voltage switching scheme is applied to control the switching devices of each VSI. The harmonics in STATCOM current caused by the dc voltage ripple is rejected by a new method developed in this paper. As a result, the size of inductor and dc capacitors can be further reduced. A very effective startup procedure is proposed to start up the STATCOM. The proposed STATCOM has the advantage of a fewer number of VSI's, the VSI's being identical and extremely fast in response to reactive power change.**

***Index Terms*—Phase-shifted sinusoidal pulsewidth modulation, static compensator, voltage-source inverter.**

I. INTRODUCTION

SEVERAL static compensators (STATCOM's) based on gate turn-off thyristors (GTO's) and a special zigzag transformer have been developed and put into operation in recent years [1], [2]. It has been recognized that these STATCOM's have advantages over conventional static var compensator's (SVC's) of generating no harmonic or less harmonic current to the system and requiring a much smaller reactor. However, zigzag transformers used in these STATCOM's are bulky, expensive, and unreliable [6].

STATCOM's based on multilevel voltage source inverters (VSI's) have been widely studied due to their capability of eliminating the zigzag transformer. In this multilevel VSI-based STATCOM category, there are mainly three different system configurations: 1) diode-clamped converter configuration [3], [4]; 2) flying-capacitor converter configuration [5]; and 3) cascading converter configuration [6]. A seven-level single phase STATCOM based on the third configuration is illustrated in Fig. 1. It is constructed by cascading several (three, in this case) voltage-source H-bridge inverters. It is shown in [6] that the third configuration has the advantages over the first and second configurations of not requiring a very large number of clamping diodes or flying capacitors.

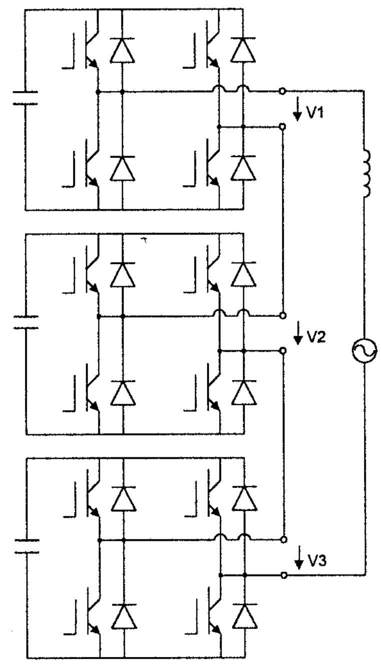

Fig. 1. Single-phase cascading VSI STATCOM.

Moreover, packaging and physical layout is very easy due to its modular structure. However, it suffers from the following disadvantages.

1) It requires a fairly large number of inverters to reduce the harmonics, even in distribution-level or industrial applications where system voltage usually ranges from 4.16 to 13.8 kV.
2) To maintain the harmonic contents within a specified range and achieve fast system response, a complicated dc voltage regulation method has to be applied to control the STATCOM output voltage [13].

In addition, none of these proposed STATCOM's based on multilevel VSI's addressed the startup procedures or the problem of output current harmonics caused by the dc ripple voltage [9].

A new type of STATCOM is proposed in this paper to solve the problems stated above and to address the startup procedures and the problem of output current harmonics

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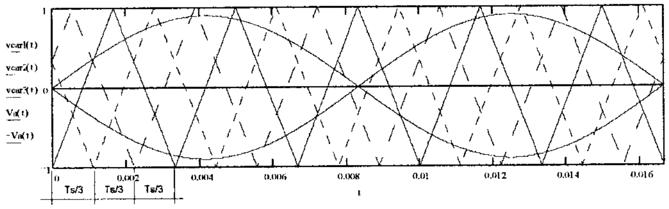

Fig. 2. Unipolar SPWM switching scheme.

caused by the dc ripple voltage. The operation principle of this proposed STATCOM will be discussed in Section II. Section III establishes the dc capacitor ripple voltage equations and the criterion for sizing the dc capacitors. A method to reject the STATCOM current harmonics caused by dc capacitor ripple voltage is developed in Section IV. A simple, yet very effective startup procedure is proposed in Section V to start up the STATCOM. Section VI gives some simulation results, and Section VII concludes the paper.

II. Proposed STATCOM and Its Operation Principle

The circuit configuration, switching scheme, control of reactive power, and dc voltage regulation are addressed in this section.

A. Main Circuit Configuration

The single-phase main circuit configuration is shown in Fig. 1, which is the same as that in [6] except for the following.

- All the H-bridge inverters including the dc capacitors are identical.
- All the switches and diodes in the main circuit have the same ratings.
- The system can have a fewer number of H-bridge inverters due to the superiority of the proposed switching scheme.

The inductor between the system and three cascading inverters serves as a current harmonic attenuator to attenuate the high-frequency current harmonics that the STATCOM generates. A three-phase STATCOM is composed of three single-phase ones with "Y" or "Δ" connection.

B. Switching Scheme

A so-called phase-shifted unipolar sinusoidal pulsewidth modulation (SPWM) switching scheme is proposed to operate the switches in the system. The scheme, which is a slightly modified version of phase-shifted SPWM [7], [10], is briefly explained with the aid of Fig. 2. Three triangle carrier signals ($\mathrm{car1}(t)$, $\mathrm{car2}(t)$, and $\mathrm{car3}(t)$) are for three H-bridge inverters, respectively. They are time shifted by $T_s/3$, where T_s is the period of these carrier signals. Three H-bridge inverters share the same modulating sinusoidal signals $V_a(t)$ and $-V_a(t)$. It is obvious that the switching scheme of each H-bridge inverter is SPWM unipolar voltage switching [8]. The output voltage of the single-phase STATCOM shown in Fig. 1 is the summation of these three H-bridge inverter output voltages. One of the main advantages of this switching scheme is that the harmonics of the resultant STATCOM output voltage only appear as

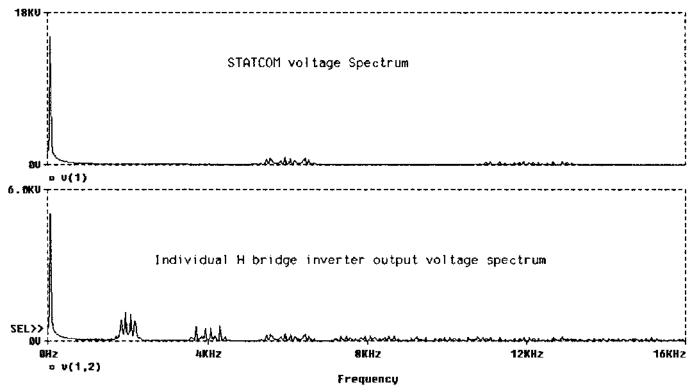

Fig. 3. Spectrums of the STATCOM voltage and individual inverter voltage.

sidebands centered around the frequency of $2Nf_s$ and its multiples, provided that the voltage across the dc capacitor of each inverter is the same. Here, N is the number of H-bridge inverters, and f_s is the frequency of triangle carrier signals. Therefore, the resultant STATCOM output voltage has very high equivalent switching frequency, even if the switching frequency of the individual switches is not so high.

The theoretical proof of this conclusion can be obtained by following the similar procedure presented in [7], where the Double Fourier Analysis method is applied. To demonstrate this conclusion, the output voltage spectrums of an individual H-bridge inverter and the STATCOM composed of three cascading H-bridge inverters are shown in Fig. 3. The switching frequency of the individual switch is 1 kHz. As we can see from this figure, the harmonics of the STATCOM output voltage only appear around 6 kHz, 12 kHz, and so on. Another observation from this figure is that the fundamental component of the STATCOM output voltage is three times that of the individual H-bridge output voltage.

C. Control of Reactive Power

It is well known that the amount and type (capacitive or inductive) of reactive power exchange between the STATCOM and the system can be adjusted by controlling the magnitude of STATCOM output voltage with respect to that of system voltage. The reactive power supplied by the STATCOM is given by

$$Q = \frac{V_{\mathrm{STATCOM}} - V_s}{X} V_s \tag{1}$$

where V_{STATCOM} and V_s are the magnitudes of STATCOM output voltage and system voltage, respectively, and X is the equivalent impedance between STATCOM and the system. When Q is positive, the STATCOM supplies reactive power to the system. Otherwise, the STATCOM absorbs reactive power from the system. Since the modulating signals are the same for the H-bridge inverters in the system, the fundamental component of the STATCOM output voltage is N times that of each H-bridge inverter, provided that the voltage across the dc capacitor of each inverter is the same. As a result, the STATCOM output voltage can be controlled by the modulating index (MI) (m_a). V_{STATCOM} is proportional to m_a, as long

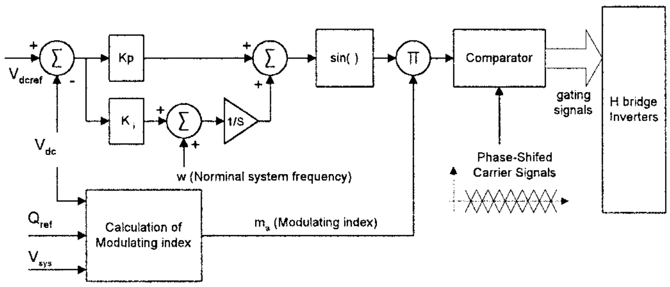

Fig. 4. STATCOM control system block diagram.

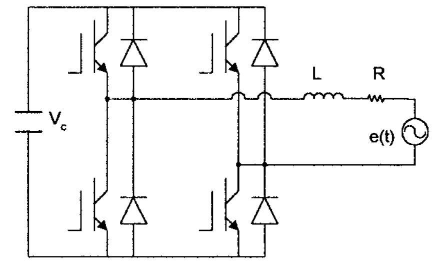

Fig. 5. One-inverter STATCOM.

as the individual H-bridge inverter is in the linear modulating region. Due to its ability to control the output voltage by the MI, the proposed STATCOM has extremely fast dynamic response to system reactive power demand.

D. Control of DC Capacitor Voltages

If all the components in Fig. 1 were ideal and the STATCOM output voltage were exactly in phase with the system voltage, there would have been no real power exchange between the STATCOM the and system, therefore, the voltages across the dc capacitors would have been able to sustain. However, a slight phase difference between the system voltage and the STATCOM output voltage is always needed to supply a small amount of real power to the STATCOM to compensate the component loss, so that the dc capacitor voltages can be maintained. This slight phase difference is achieved by adjusting the phase angle of the sinusoidal modulating signal. If the real power delivered to the STATCOM is more than its total component loss, the dc capacitor voltage will rise, and vice versa. The real power exchange between the STATCOM and the system is described by

$$P = \frac{V_s V_{\rm STATCOM}}{X}\sin(\delta) \tag{2}$$

where δ is the phase angle difference between STATCOM voltage and the system voltage. The proportional plus integral (PI) controller presented in [12] is adopted to regulate and equalize the dc capacitor voltage. The basic idea of this controller is to use the error between the reference and the actual dc voltage as feedback signal. This signal is then fed to a PI regulator to produce the phase angle δ to control the real power exchange between the STATCOM and the system and, thus, regulate the dc capacitor voltage. Interested readers are referred to [12] for a detailed description of this PI regulator. A simplified control block diagram is illustrated in Fig. 4. In this block diagram, the calculation of the MI is based on (1) and the linear modulating principle, i.e., $V_{\rm STATCOM} = m_a V_{\rm dc}$. A systematic method to design the gains of the controller is out of the scope of this paper and will be studied in the future.

III. Ripple of DC Capacitor Voltages and Sizing of the DC Capacitors

DC capacitors not only play an important role in STATCOM system performance, but comprise a large part of the total system cost, as well. Hence, proper sizing of the dc capacitors is essential to low system cost and high performance of the proposed STATCOM. Since the inverters in the STATCOM are identical, the equations are based on a one-inverter system, as shown in Fig. 5.

A. System Differential Equations

Equations (3) and (4) describe the system behavior of the one-inverter system shown in Fig. 5

$$C\frac{dv_c}{dt} = {\rm sw}\cdot i_L \tag{3}$$

$$L\frac{di_L}{dt} + Ri_L = e(t) - {\rm sw}\cdot v_c. \tag{4}$$

In (3) and (4), $e(t)$ is the system voltage, v_c is the capacitor voltage, and sw is the switching function.

B. DC Capacitor Voltage

Under the assumptions that: 1) the harmonic components centered around the switching frequency and its multiples are negligible; 2) the dc capacitor voltage ripple is small; and 3) system voltage $e(t)$ is sinusoidal, we have, in steady state, the following:

$${\rm sw}(t) = m_a \sin\omega t \tag{5}$$

$$i_L(t) = I\sin(\omega t + \varphi_i). \tag{6}$$

In (5) and (6), I is the inductor peak current, m_a is the MI, and $\varphi_i = \pm 90^\circ$ when the resistor R approaches zero. Equations (3), (5), and (6) result in

$$C\frac{dv_c}{dt} = m_a\sin\omega t\cdot I\sin(\omega t+\varphi_i) = \pm\frac{1}{2}m_a I\sin 2\omega t \tag{7}$$

$$v_c(t) = V_{\rm DC} + \frac{1}{4\omega C}m_a I\cos 2\omega t. \tag{8}$$

C. Sizing of the DC Capacitors

From (8), we know that the DC capacitor peak–peak voltage ripple is $\Delta V_c = (2m_aI)/(4\omega C)$. Once this ripple value is specified, the size of the dc capacitor can be calculated by

$$C = \frac{m_a I}{2\omega\Delta V_c}. \tag{9}$$

To keep the ripple voltage within the specified value in the full range of reactive power of the STATCOM, m_a in (9) should be set to one. Compared with [6, eqs. 8, 9], the total required capacitance of the proposed STATCOM in this paper is less than that of the STATCOM proposed in [6].

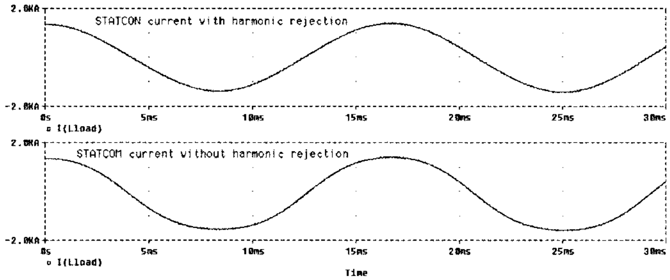

Fig. 6. STATCOM currents with and without harmonic rejection.

IV. Rejection of Current Harmonics Caused by DC Capacitor Voltage Ripple

From (4), (5), and (8), we know that the dc capacitor voltage ripple will cause inductor current i_L to have third-order harmonic component. If this harmonic component can be rejected, the size of the inductor L and dc capacitors can be further reduced. A technique to reject harmonic caused by dc voltage ripple was proposed in [9], where the dc voltage ripple is independent of the inverter current. Unfortunately, the dc voltage ripple is proportional to the inverter current in the proposed STATCOM. Nevertheless, the basic idea in [9] enlightened the authors to develop a new method to tackle the problem.

In (4), if the switching function can be expressed

$$\mathrm{sw}(t) = \frac{V_{\mathrm{STATCOM}} \sin \omega t}{v_c(t)} \tag{10}$$

the inductor current will be purely sinusoidal. Equations (3), (6), and (10) will result in

$$\frac{d(v_c^2)}{d(2\omega t)} = \pm \frac{1}{2\omega C} V_{\mathrm{STATCOM}} I \cos 2\omega t \tag{11}$$

$$v_c(t) = V_{\mathrm{DC}}(1 \pm k \cos 2\omega t)^{\frac{1}{2}} \tag{12}$$

where

$$k = \frac{m_a I}{2\omega C V_{\mathrm{DC}}} \tag{13}$$

$$m_a = V_{\mathrm{STATCOM}} / V_{\mathrm{DC}}. \tag{14}$$

As we can see, (8) is the first-order approximation of (12). From (10), (12), and (14), we have

$$\mathrm{sw}(t) = m_a \sin \omega t \cdot (1 \pm k \cos 2\omega t)^{-\frac{1}{2}}. \tag{15}$$

Instead of $m_a \sin \omega t$, a slightly modified version, i.e., (15), is chosen as the modulating signal. In this case, the inductor current will have no low-order harmonic components.

Another option to reject the harmonic component is to use (10) directly as the modulating signal. Since the dc voltage ripple frequency is much lower compared to the resultant STATCOM switching frequency $(2Nf_s)$, the switching function will approach (10), if (10) is used as the modulating signal.

Depending on system implementation, either one of the above proposed methods can be used. The result is the same. The PSPICE simulation result shown in Fig. 6 illustrates the effectiveness of the proposed harmonic rejection method.

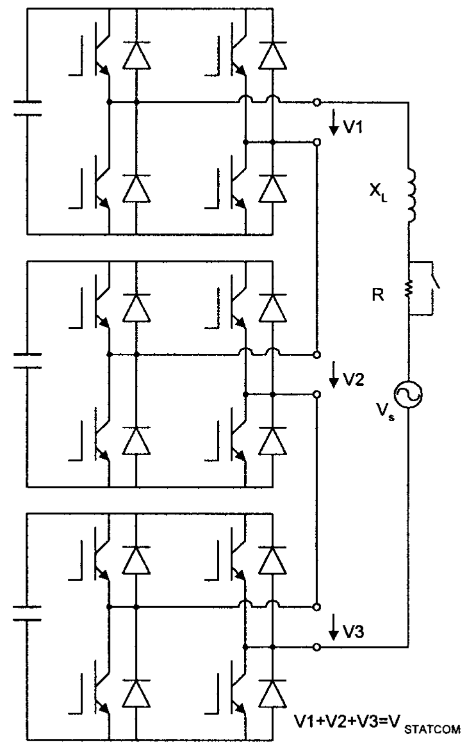

Fig. 7. STATCOM with startup insertion resistor.

V. Startup Procedure

The task of starting up the STATCOM is to bring the reactive power output to a certain level in a very short time, while maintaining all the switching devices within their ratings. The challenge of starting up the STATCOM lies in the fact that, before startup, the dc capacitor voltages are zero. It is observed, however, that when all the active switches are suppressed (no gating signals are supplied to these switches), the STATCOM system is actually composed of several cascading full-bridge rectifiers with no dc-side load except the dc capacitors (Fig. 7). Based on this observation, a startup procedure is proposed. The steps of this procedure are explained with the aid of Fig. 7.

Step 1: Insert a resistor (R) in the ac side of the STATCOM (Fig. 7) and suppress all the gating signals to the active switches, so that the dc capacitors are charged through their corresponding rectifiers. The purpose of inserting the resistor is to limit the initial charging current and, thus, limit the current through the diodes. The dc capacitor voltages of all three units will be equally charged due to the fact that the dc capacitances of all three cascading units are equal.

Step 2: When the dc voltage reaches a certain level, the resistor is bypassed and the gating of the active switches are enabled. A certain phase-angle difference between the STATCOM output voltage and the system voltage is maintained, such that the STATCOM is absorbing more real power from the system than its total component loss. Therefore,

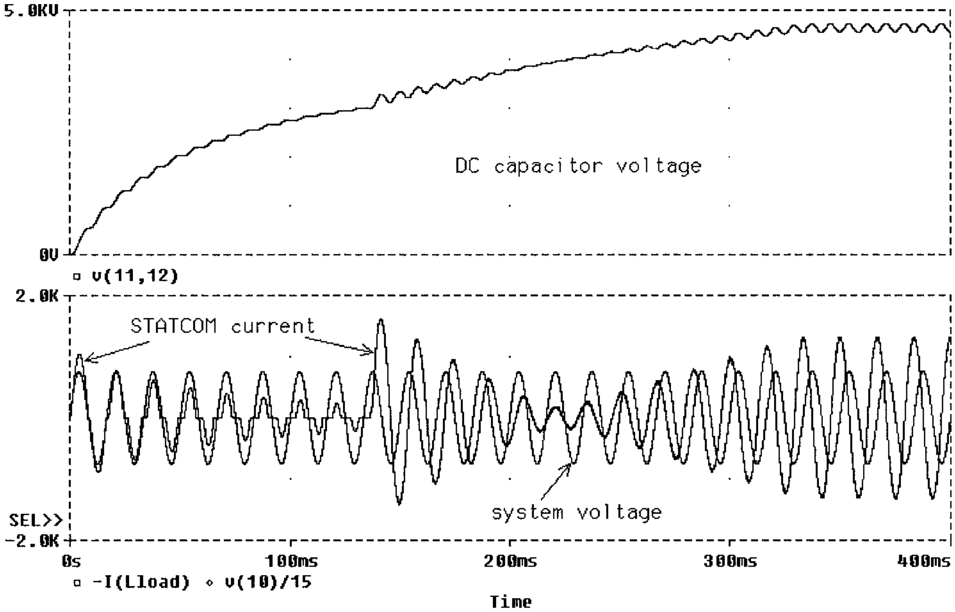

Fig. 8. Startup of the STATCOM.

the dc voltages are further raised to their normal operating level.

Step 3: Once the dc voltages reach their normal operating levels, the STATCOM is put into regulation mode.

Simulation is carried out based on the above three steps. The result is shown in Fig. 8. The system is in rectifying mode from 0 to about 140 ms. At about 140 ms, the resistor is bypassed and the gating signals of the STATCOM active switches are enabled. The STATCOM absorbs reactive power until about 230 ms, because during the interval from 140 to 230 ms V_{STATCOM} is lower than V_s. After 230 ms, the dc capacitor voltage reaches a level, such that V_{STATCOM} is greater than V_s and, therefore, the STATCOM supplies reactive power to the system. At about 330 ms, the dc capacitor voltage reaches the required level and the STATCOM is put into regulation mode. From 0 to 330 ms, the STATCOM is absorbing more real power than its total component loss. As a result, the capacitor voltage keeps increasing. During the interval from 330 to 400 ms, the real power absorbed by the STATCOM equals its total component loss. Hence, the dc capacitor voltage maintains the same level.

VI. System Simulation Results

Simulation of a ±50-Mvar STATCOM connected to the 13.8-kV system is carried out. The STATCOM is of "Y" connection with three H-bridge inverters per phase. The main parameters are as follows:

- $V_s = 13.8$ kV;
- $Q_{\mathrm{VAR}} = \pm 50$ Mvar;
- $L = 4$ mH;
- $V_{\mathrm{DC}} = 5.5$ kV;
- $\Delta V_c = 7\% V_{\mathrm{DC}} \approx 370$ V;
- $C = 10$ mF;
- $f_s = 600$ Hz.

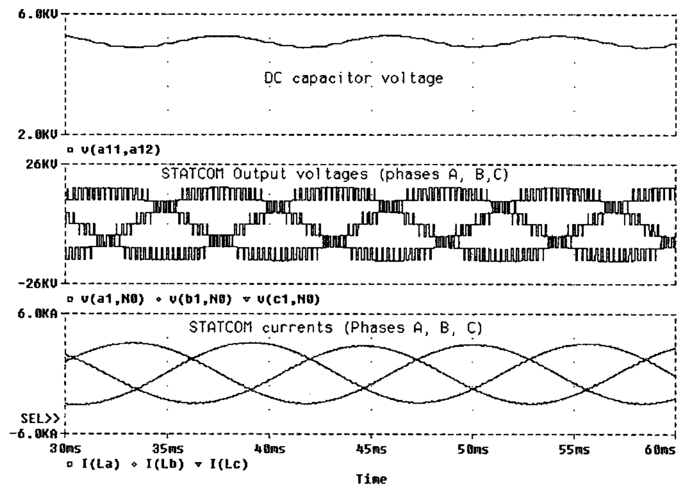

Fig. 9. STATCOM in steady state.

A. Steady State

System operation in the steady state is simulated, and some of the results are shown in Fig. 9. In the steady state, the STATCOM supplies 50 Mvar of reactive power to the system. As we can see from this figure, there is a second-order harmonic component superimposed on the dc capacitor voltage, as described by (8). However, no low-order harmonic component is observed in the STATCOM current due to the effectiveness of the proposed harmonic rejection method.

B. Dynamic Response to Reactive Power Demand

Fig. 10 illustrates some of the simulation results, when the reactive power demand is changed from +50 Mvar to −50 Mvar. It is observed from this figure that the STATCOM takes almost no time to achieve the changeover. This simulation result further demonstrates the extremely fast dynamic

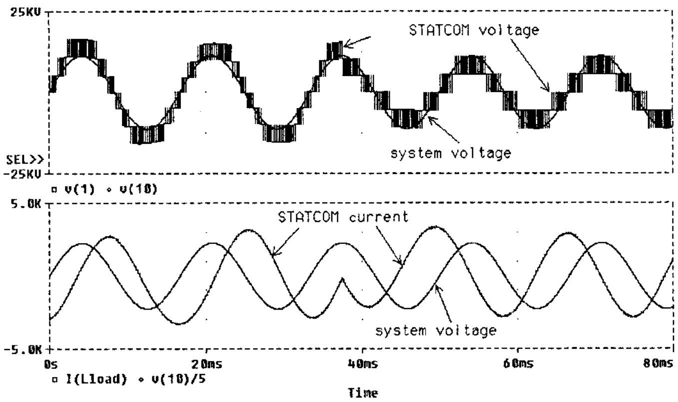

Fig. 10. Dynamic response to reactive power demand change.

response of the proposed STATCOM because of the MI control method. Another interesting observation from this figure is that STATCOM output voltage dropped one step of the staircase-like waveform to achieve lower fundamental component value.

VII. Conclusion

A new type of STATCOM based on cascading VSI's with phase-shifted unipolar SPWM switching scheme has been proposed in this paper. The main circuit of this STATCOM is composed of several identical voltage-source H-bridge inverters. Compared with the other types of multilevel VSI-based STATCOM's, it has the following advantages.

- All H-bridge inverters including storage capacitors are identical. The main switches and diodes have the same ratings. As a result, system design, maintenance, and stocking of spare parts are made easy.
- Total system cost is reduced due to a fewer number of inverters required in system application.
- System response is faster due to the MI regulation method.
- Redundancy is easily achieved by cascading one more identical H-bridge inverter to the system.

The dc capacitor voltage ripple was theoretically analyzed and the criterion for sizing the dc capacitor was established. A novel method was proposed to reject the STATCOM current harmonic component caused by the dc capacitor voltage ripple. A simple, yet very effective startup procedure was developed to start up the STATCOM. Higher device switching loss is a disadvantage of the proposed STATCOM compared with the one proposed in [6]. However, this disadvantage will diminish when low-loss and high-power switching devices [11] are developed and used in the H-bridge inverters.

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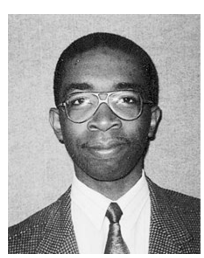

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