A new, universal Series Hybrid Cascaded H-Bridge Converter for Power-Hardware in the Loop Emulation

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«Hardware», «Multilevel converters», «Resonant converter», «Amplifiers», «Converter circuit»

Abstract

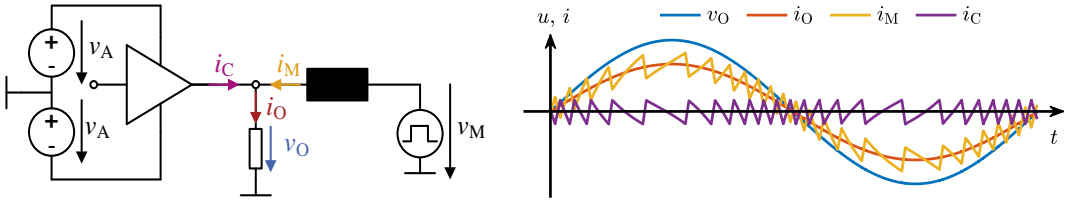
This paper presents a new Series-Hybrid Cascaded H-Bridge (SH-CHB) Converter for Power-Hardware in the Loop (PHIL) systems. The converter combines the benefits of CHB-Cells, high power density and high system efficiency, with the advantages of Linear Power Amplifiers (LPA), high bandwidth and high fidelity. The introduced system is used to emulate different AC-grids as well as DC-grids with simultaneous supply of sinusoidal test signals for impedance spectroscopy of converters. The system provides sinusoidal test signals up to 105 kHz with a three-phase output AC voltage of 400 V or a DC voltage of 1000 V. The maximum output power of the system is 60 kVA.

Introduction

In converter-fed grids, the converters connected to the point of common coupling (PCC) define the behavior of the PCC. Consequently, the simplified consideration of a grid behavior by means of passive grid impedances is obsolete. Additionally, the installed power transformed by converters in the European electrical grid is increasing, whereby the converters define more and more the PCC behavior. Hence, the behavior of the PCC depends among others on characteristics of those converters, such as the control parameters, the phase lock loop (PLL) design and the filter components. Due to the impact of the converter characteristics on the PCC behavior, parallel connected converters can influence each other. This could lead to unstable operating points of the grid. To predict the behavior of converters in converter-fed grids, models of the converters and the grid must be developed and parameterized. Hence, a Power-Hardware in the Loop (PHIL)-system is needed, which could determine the parameters of the grid and the converters. Therefore, the designed PHIL-system should be able to emulate different grid situations, so that the converter can be investigated under the same operating conditions under which it will be used later. Simultaneously, the PHIL-system must generate test signals to measure the behavior of the converter. One possible method to analyze the stability of a converter is the Nyquist stability criterion [1]. For the Nyquist stability criterion a small signal model or a harmonic impedance model of the analyzed converters and the grid are needed [1, 2]. These can be obtained by an impedance spectroscopy. To parameterize the models, sinusoidal test signals with frequencies up to the switching frequency of the analyzed converter must be added to the output voltage of the PHIL-system. For accurate measurements a high power, high fidelity and high dynamic AC-voltage source is necessary. Therefore, a new Series-Hybrid CHB (SH-CHB) concept was developed. The presented SH-CHB converter can provide a 400 V three-phase AC-Grid or 1000 V DC-Grid. The maximum output power of the system is 60 kVA with a maximum large signal bandwidth of 105 kHz.

Hybrid Converter Concepts

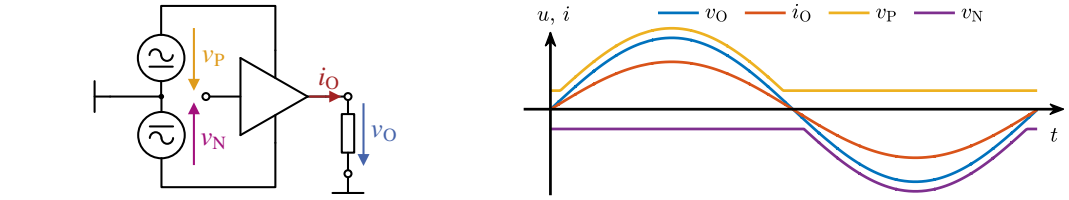
Hybrid Converter Concepts can be distinguished between three main concepts: Envelope Hybrid Converter (EHC), Series Hybrid Converter (SHC) and Parallel Hybrid Converter (PHC) [3]. In this consideration, the Hybrid converter consists of a main converter, which is a switched-mode power supply (SMPS) and a correction amplifier, which is a Linear Power Amplifier (LPA). In PHCs, the main converter provides the main part of the output current i_M. The correction amplifier has only to provide a fraction of the output current i_C and hence it can be designed for a small current. In Figure 1b the idealized current and voltage waveforms are illustrated. According to Figure 1a, the correction amplifier is directly connected to the output, hence the correction amplifier must be designed for the whole output voltage v_O. Thus, the PHC is only reasonable for low output voltages [3]. Also the LPA must be designed in a way that it can provide the total output current i_O in transients because the current slope of the main converter is limited [4].



a) Amplifier schematic b) Idealized waveforms

Figure 1: Amplifier schematics and idealized waveforms of a Parallel Hybrid Converter (PHC)

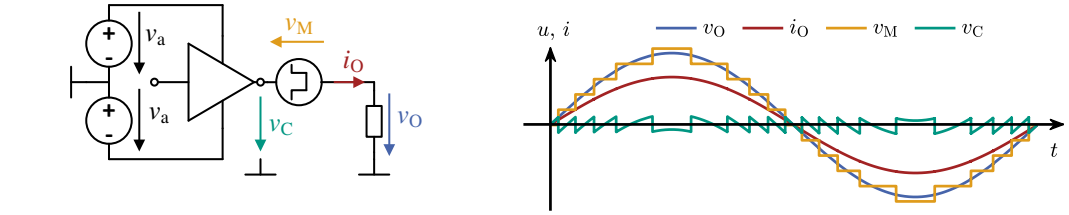
In EHCs, the SMPS drives a variable DC-bus system, which supplies the LPA, shown in Figure 2a. The positive and negative DC voltage v_P and v_N are controlled in such a way that the voltage drop over the LPA is as small as possible, which is illustrated in Figure 2b. The LPA has to provide the whole output current. One drawback of this concept is that for high frequency output signals the DC voltages v_P and v_N must also be changed at a high frequency. This leads to a switching frequency of the SMPS in the megahertz range [5] and hence this concept is only reasonable for low output power systems [3].



a) Amplifier schematic b) Idealized waveforms

Figure 2: Amplifier schematics and idealized waveforms of an Envelope Hybrid Converter (EHC)

The typical concept of SHC is shown in Figure 3a. The correction amplifier is in series with the main converter. Both must provide the complete output current i_O. As can be seen in Figure 3b, the output voltage v_O is the sum of the main converter voltage v_M und the correction amplifier voltage v_C. To reduce the difference between the output voltage v_O and the main converter voltage v_M, the main converter should be a multi-level-converter. Through this, the correction amplifier has only to provide the remaining, small difference, shown in Figure 3b.



a) Amplifier schematic b) Idealized waveforms

Figure 3: Amplifier schematics and idealized waveforms of a Series Hybrid Converter (SHC)

The usage of a multi-level-converter allows to increase the output voltage v_O at will by increasing the number of multilevel converter cells. Independently, the correction amplifier needs to deliver only a

fraction of the output voltage v_O, which is an advantage compared to the PHC and EHC. The bandwidth of the system is defined by the LPA, thus a high frequency LPA is needed. One drawback of this concept is that for a high quality output voltage the LPA must be able to compensate the step voltage of the main converter. Hence, a LPA with a very high slew rate is necessary and additionally a small dv/dt-filter parallel to the main converter is needed.

In summary, the SHC is considered as the best topology to be used in the application as a PHIL emulator, because this topology allows high output voltages in combination with high bandwidth and high power. Another important fact is the guarantee of a safe operation mode in transients of the LPA compared to the PHC.

Series Hybrid Cascaded H-Bridge Converter

There are different implementations of SHCs. Here, the SHC is implemented as a Series Hybrid Cascaded H-Bridge (SH-CHB) Converter, shown in Figure 4. The converter consists of 12 CHB-Cells with a secondary DC-Link voltage of 30 V. The LPA is in series with the CHB-Cells towards the output of the PHIL-system. Between the CHB-Cells and the LPA an optional dv/dt-filter is implemented to reduce the voltage slope which must be compensated by the LPA.

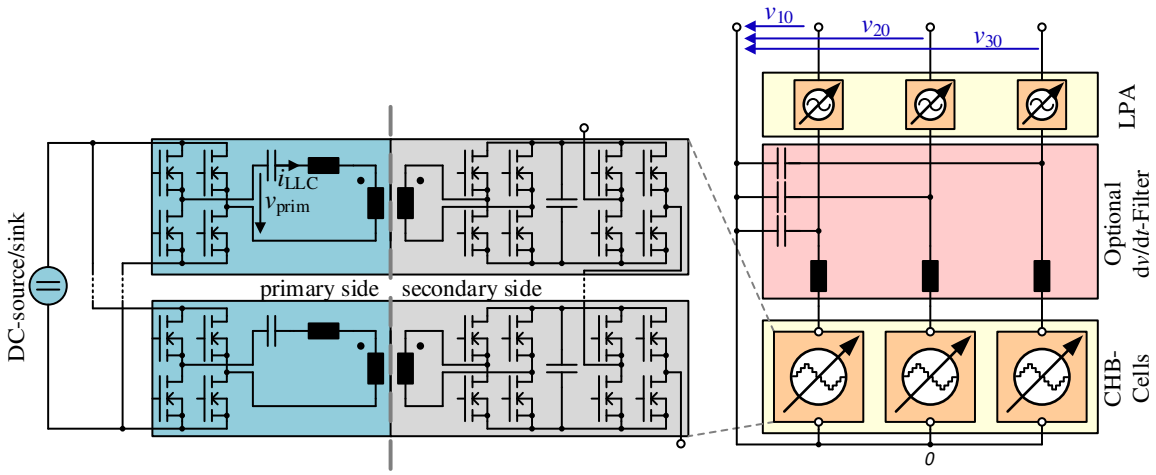


Figure 4: Series Hybrid Cascaded H-Bridge Converter Concept

The introduced SH-CHB converter is able to provide a three-phase AC output voltage up to 400 V or DC voltage up to 1000 V. The nominal output power is 60 kVA. In Figure 5 the interconnection of one phase between CHB converter and the LPA of previous described systems [6–8] and of the new presented system is depicted.

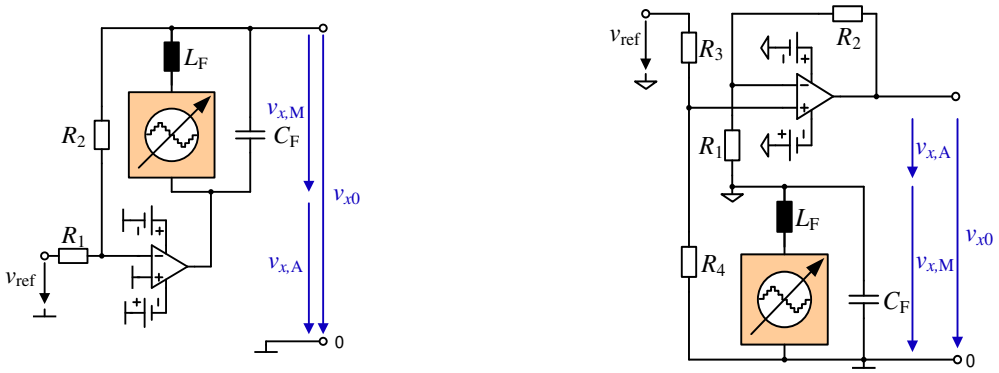
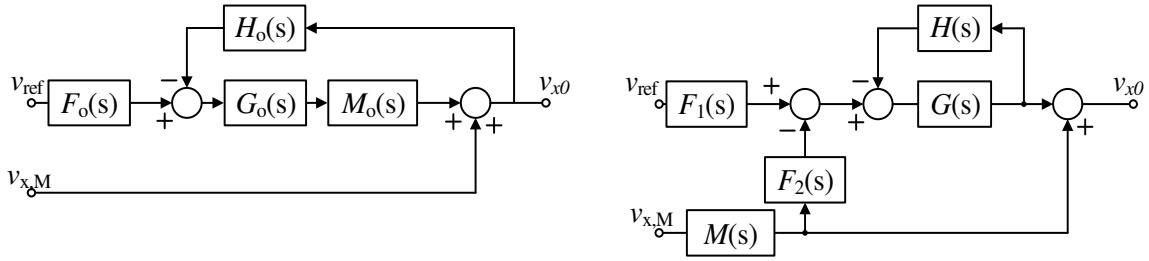


Figure 5: Left: Concept of previous described SHCs, right: New Concept of the SH-CHB Converter

In Figure 6a the corresponding control block scheme of previous described systems according to [6, 7, 9] and in Figure 6b of the new system are illustrated, respectively. G(s) is the open-loop transfer function of the LPA, M(s) is the transfer function of the multilevel converter including the dv/dt filter, F(s) and H(s) are the transfer functions of the resistor circuits. As can be seen in Figure 5 and Figure 6, the closed

loop of the previous systems contain the multilevel converter. In the new presented system, the multilevel converter is not a part of the closed loop of the LPA.



a) Previous published systems b) New presented system

Figure 6: Control block scheme of SH-CHB converter: a) previous published system [6, 7, 9]; b) new presented system

Based on Figure 6, the closed loop transfer function of the LPA for the previous system $G_{c,o}(s)$ and the presented system $G_c(s)$ can be derived. The transfer functions $G(s)$ and $G_o(s)$ are the same, depending on the used LPA. Subsequently, the damping resistor for the dv/dt filter is neglected. According to [9], the transfer function $F_o(s)$, $H_o(s)$ and $M_o(s)$, that are shown in Figure 6a, are defined as follows:

$$F_o(s) = \frac{R_2}{R_2+R_1} \quad (1)$$

$$H_o(s) = \frac{R_1}{R_2+R_1} \quad (2)$$

$$M_o(s) = \frac{R_1+R_2}{R_2+R_1+Z_{\mathrm{MLC}}(s)} \quad (3)$$

$$Z_{\mathrm{MLC}}(s) = \frac{R_{\mathrm{MLC}}+sL_{\mathrm{F}}}{1+sR_{\mathrm{MLC}}C_{\mathrm{F}}+s^2L_{\mathrm{F}}C_{\mathrm{F}}}, \quad (4)$$

For the new presented system, the transfer function $F_1(s)$, $F_2(s)$, $H(s)$ and $M(s)$, compared to Figure 6b, are given by:

$$F_1(s) = \frac{R_4}{R_3+R_4} \quad (5)$$

$$F_2(s) = \frac{R_3}{R_3+R_4} \quad (6)$$

$$H(s) = \frac{R_1}{R_2+R_1} \quad (7)$$

$$M(s) = \frac{1}{1+sR_{\mathrm{MLC}}C_{\mathrm{F}}+s^2L_{\mathrm{F}}C_{\mathrm{F}}} \quad (8)$$

Thus, the closed loop transfer function of the LPA for the previous system $G_{c,o}(s)$ and the new system $G_c(s)$ are defined by:

$$G_{c,o}(s) = \frac{G_o(s)\cdot M_o(s)}{1+G_o(s)\cdot M_o(s)\cdot H_o(s)} = \frac{G_o(s)\cdot(R_1+R_2)}{R_1+R_2+Z_{MLC}(s)+R_1\cdot G(s)} \quad (9)$$

$$G_c(s) = \frac{G(s)}{1+G(s)\cdot H(s)} = \frac{G(s)\cdot(R_1+R_2)}{R_1+R_2+R_1\cdot G(s)} \quad (10)$$

As can be seen in Equation (9), the multilevel converter is part of the closed loop of the LPA in the previous system. This results in higher latency and attenuation over the feedback path and in an additional pole. Thus, the closed loop of the previous system is less stable than of the new system and so the bandwidth of the LPA system is limited. In addition, the multilevel voltage is a distortion value within the closed loop of the LPA, which can induce oscillations. The benefit of the new presented system is that the feedback path of the LPA is closed within the LPA system. Hence, the feedback path is short so that a higher bandwidth can be reached. To guarantee, that the LPA can compensate the voltage steps of the multilevel converter the transfer function $F_2(s)$ must have a high bandwidth and a low latency. Due to the high input resistance of the non-inverting input of the LPA, a simple resistor circuit with high bandwidth and low latency can be applied to form the difference between the reference voltage v_{ref} and the CHB-voltage $v_{\mathrm{x,M}}$.

To control the output voltage of the multilevel converter, the number of activated CHB-Cells n_{CHB} is calculated by comparing the cell voltage with the necessary reference. The difference between the CHB-voltage $v_{x,\mathrm{M}}$ and the reference voltage v_{ref} is allocated by the LPA. Hence, no switching of the CHB-Cells is necessary which increases the efficiency of the CHB-Cells. To reduce the voltage of the LPA, the voltage drop over the CHB-Cells and cables are considered. Therefore, an iterative loop is necessary to calculate the number of activated CHB-Cells n_{CHB}. In Figure 7 the calculation loop is illustrated.

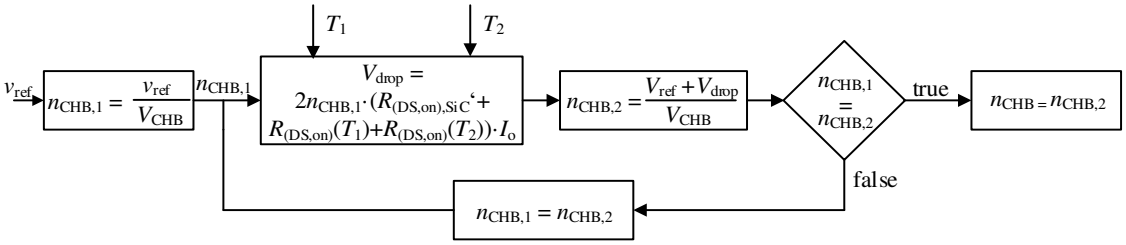


Figure 7: Algorithm to determine the number of activated cells

In addition, a sorting algorithm is developed that ensures a symmetric stress of the CHB-Cells. In contrast to the Modular Multilevel Converter (MMC), no balancing of the cell voltages is necessary due to the power supply of each cell [10]. Hence, the sorting algorithm is used to balance the stress of the single cells. Therefore, the parts with the highest losses within one cell are considered. The highest losses occur in the output H-Bridge and the secondary H-Bridge of the LLC. The highest temperature of these two parts is considered as an input parameter for the sorting algorithm. In Figure 8 the principle of the sorting algorithm is depicted.

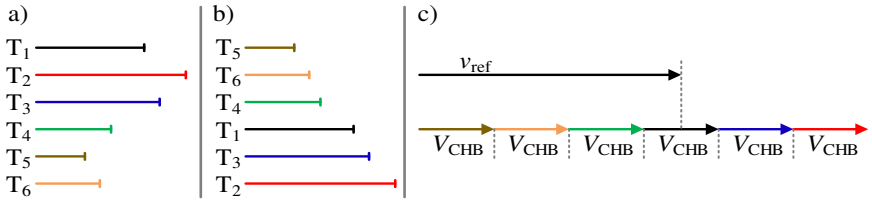


Figure 8: Sorting algorithm to balance the cell stress

The reference voltage v_{ref} is generated by using the cells with the lowest temperature. In contrast to an MMC, the last cell is the LPA and thus no PWM is necessary.

Implementation and experimental results

In the following, the hardware implementation of the system is described. The system consists of 36 CHB-Cells and three LPAs. Additionally, a high-performant control structure is implemented consisting of a self-developed System-on-Chip (SoC)-System to control the system and a Local Control Unit (LCU) on each CHB-Cell.

H-Bridge Cell with resonant DC-DC Converter

The structure of the CHB-Cells is illustrated in Figure 4. An Active Front End with 660 V on the primary side supplies the CHB-Cells. Thus, on the primary side the 900 V SiC-MOSFETs *C3M0280090D* from *Wolfspeed* are used. The galvanic isolation is implemented by a transformer with a ratio of 22:1, seen in Figure 9.

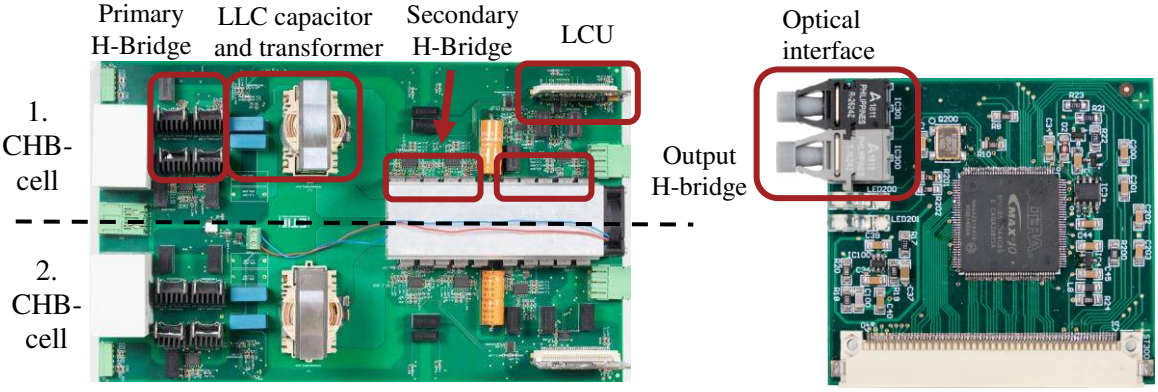


Figure 9: CHB-Cell (left) and Local Control Unit (LCU) (right)

The capacitance of the LLC-circuit is calculated so that the resonance frequency is about 60 kHz. On the secondary side, the DC-link voltage is 30 V and the output current of the CHB-Cells is 80 A. Hence, the 60 V Si-MOSFETs *CSD18536KCS* from *Infineon* with a rated current I_D of 200 A are used. In Figure 9 the developed board is illustrated. The 660 V input is on the left side and the 30 V output is on the

right side. On each board, two CHB-Cells are implemented. The CHB-Cells share one heatsink for the secondary-side Si-MOSFETs. In addition, the LCU is shown on the right side. The LCU controls one CHB-Cell on the PCB. The LCU contains a *MAX10* FPGA from *Altera* with 8000 logic cells. For the communication with the central SoC-System fiber optical cables are used with a bandwidth of 50 MBaud/s, shown in Figure 9.

In Figure 10 the measured LLC-current i_{LLC} and output voltage of the primary H-bridge v_{prim} is depicted. The LLC resonant circuit shows inductive behavior. Hence, zero voltage switching at turn-on is reached. The turn-on switching event is shown on the right side in Figure 10. The MOSFET is turned on while the drain-source-voltage $v_{DS,\,SiC}$ is already zero. Thus, no turn-on losses occur.

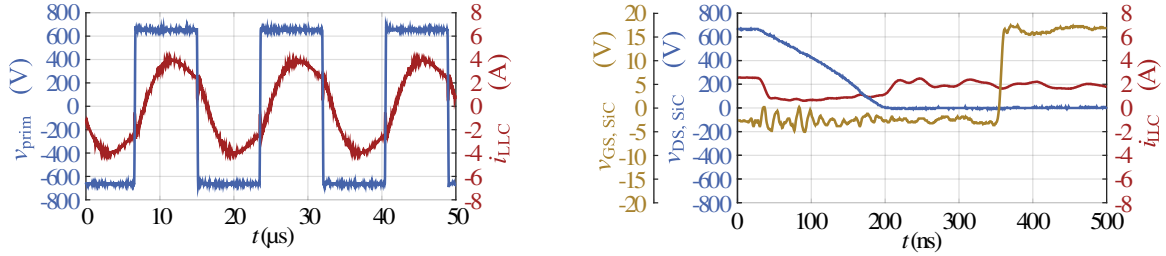


Figure 10: left: resonant LLC current i_{LLC} and input voltage of the LLC v_{prim}, right: turn-on event of the primary SiC-MOSFET; blue: Drain-Source voltage v_{DS}, brown: Gate-Source voltage v_{GS}, red: LLC current i_{LLC}

To adjust 36 LLC resonant circuits with 36 different resonance frequencies, an algorithm is developed that automatically determines the correct switching frequency f_{sw}. The algorithm is implemented in the LCU and is depicted in Figure 11 (right).

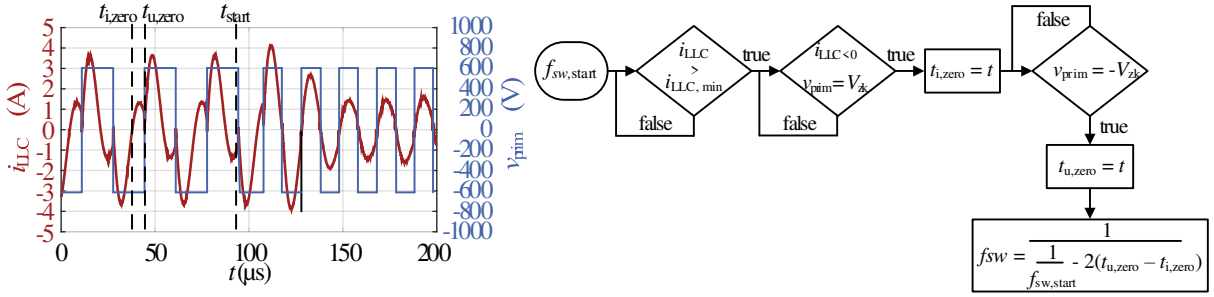


Figure 11: left: resonant LLC current i_{LLC}, right: algorithm for automatic switching frequency adaptation

At the beginning of the algorithm, every CHB-Cell starts with the same switching frequency $f_{sw,\,start}$, which is lower than the resonance frequency of the LLC circuit. Then the algorithm measures the time between the polarity change of the LLC current i_{LLC} and the polarity change of the output voltage of the primary H-bridge v_{prim}. The output voltage of the primary H-bridge is calculated based on the signals within the FPGA and the measured latency of the board. Subsequently, the correct switching frequency f_{sw} can be calculated by equation (11).

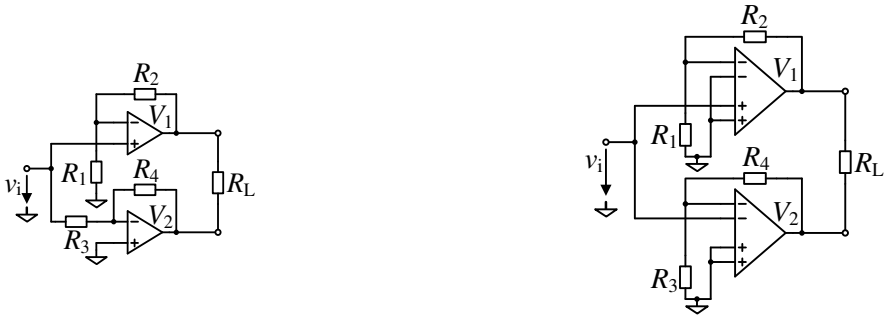
$$f_{sw} = \frac{1}{\frac{1}{f_{sw,start}} - 2(t_{u,zero} - t_{i,zero})} \tag{11}$$

Where $t_{i,zero}$ and $t_{u,zero}$ are the points in time of the polarity change of the LLC current i_{LLC} and of the output voltage of the primary H-bridge v_{prim}, respectively. In Figure 11 (left) the measured LLC current i_{LLC} is depicted. At the instant t_{start} the algorithm calculates the correct switching frequency f_{sw}. By means of the algorithm each cell runs in the optimal operating point. Through this, a cell efficiency of 98 % is reached.

High dynamic Linear Power Amplifier

The LPA is a very important part of the whole system since it defines the dynamics and the fidelity of the output voltage. The most important parameters of the LPA are the slew rate, the latency, the bandwidth and the maximum output current. To compensate the step voltage of the CHB-Cells the slew rate must be very high and the latency must be low. Since an LPA cannot reach the slew rate of a switched converter, an additional dv/dt-filter is necessary. Typical existing LPA slew rates and latencies are 10 - 30 V/µs and 1 µs, respectively [11]. With these parameters, a compensation of the step voltage is only possible for low dynamics of the output voltage. Hence, a new LPA concept was developed. To reach a

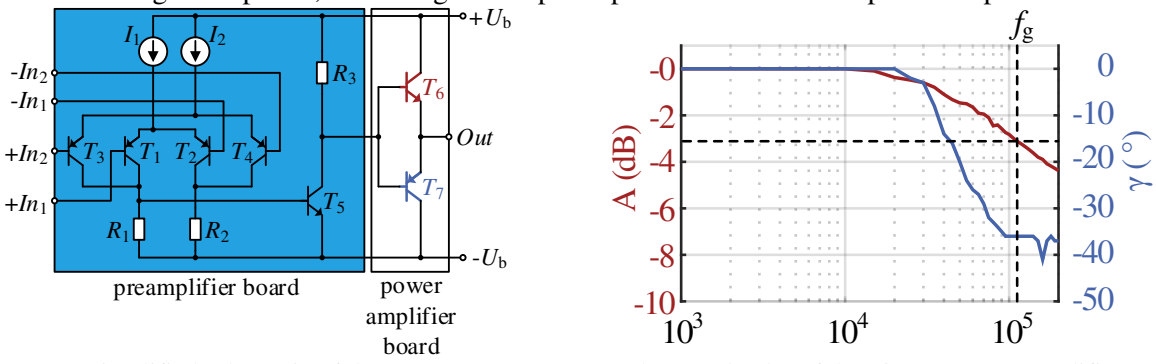
higher maximum slew rate two LPAs are interconnected in H-bridge, shown in Figure 12. Figure 12a shows the interconnection of two standard amplifiers. The drawback of this system is that the resistor R_3 defines the input impedance, which is relatively small compared to the input resistor of the amplifier. Since the signal source of the LPA is a passive resistor circuit, shown in Figure 5, a low input impedance would lead to distortion. Thus, an H-bridge interconnection of two standard amplifiers cannot be used. Therefore, a new amplifier was developed, which has four independent inputs. The H-Bridge with the new developed amplifiers is shown in Figure 12b. Through this new interconnection, the amplifier impedance defines the input impedance of the H-bridge, which is about 1000 times higher than R_3.



a) Conventional amplifier H-bridge b) New developed amplifier H-Bridge

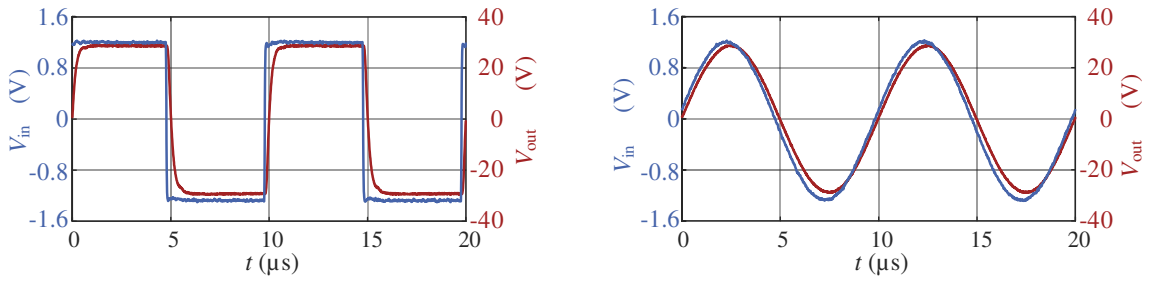
Figure 12: Amplifier H-bridge with a) conventional amplifiers and b) new developed amplifiers with four independent inputs

In Figure 13a, the significantly simplified schematic of one LPA is shown. The particularity of this LPA is the new, differential input stage. By means of their high gain, the input transistors decouple the four inputs, so the four input signals do not influence each other. In Figure 15 (left) the realization of the LPA as H-Bridge is depicted, consisting of two preamplifier boards and six power amplifier boards.



a) Simplified schematic of the LPA b) Bode plot of the Linear Power Amplifier

Figure 13: a) simplified schematic of the LPA, b) Bode plot of the Linear Power Amplifier



a) Square wave output voltage b) Sinusoidal output voltage

Figure 14: Output voltage of the LPA, a) square wave output voltage with frequency of 100 kHz, b) Sinusoidal output voltage with a frequency of 100 kHz

In Figure 14, the square wave output voltage of the LPA (left) and sinusoidal output voltage (right) are illustrated. As can be seen in Figure 14a, a maximum slew rate of 500 V/µs and a latency of only 200 ns are achieved with the H-bridge interconnection of two LPAs. Besides the slew rate, the bandwidth is also important to facilitate sinusoidal test signals with a high frequency. To analyze converters with

switching frequencies up to 60 kHz, it is necessary to generate sinusoidal test signals up to this frequency. In Figure 14b the sinusoidal output voltage of the LPA is shown with an output frequency of 100 kHz. The measured bode plot of the LPA is depicted in Figure 13b. The represented LPA has a -3dB bandwidth up to 105 kHz and thus it easily can generate test signals up to 60 kHz.

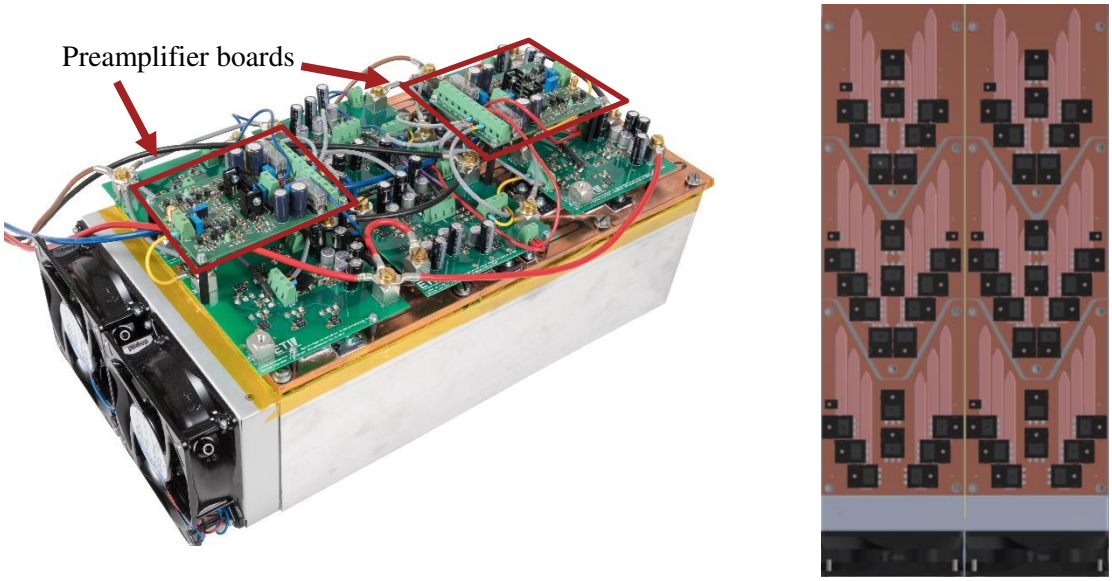


Figure 15: Left: Linear Power Amplifier, right: output transistors and cooling concept of the LPA

In addition, the maximum output current of the LPA is crucial, because it is in series with the CHB-Cells and thus defines the maximum output current. In Figure 15 (right), the realization of the output transistors T_6 and T_7 of the LPA is depicted. The transistor T_6 consists of 10 NPN-transistors *MJL4281* and the transistor T_7 consists of 10 PNP-transistors *MJL4302*, respectively. To increase the maximum output current, a cooling concept with heatpipes for spreading the heat was developed. The particularity of this cooling concept is that the isolation is implemented between the six copper plates and the heatsink and not between the transistors and the copper plates. Thus, the heat is first spread by the heatpipes, which increases the effective surface, before passing through the thermal foil below the copper plates. Through this, the maximum heat dissipation of one transistor can be increased from 65W to 133 W. With this cooling concept, the possible heat dissipation of one LPA is 5 kW and thus an output current of 100 A is possible.

Converter concept

Besides the power electronic units, CHB-Cells and LPA, the control structure is also crucial for the performance of the PHIL-system. In Figure 16, the control structure of the system is depicted.

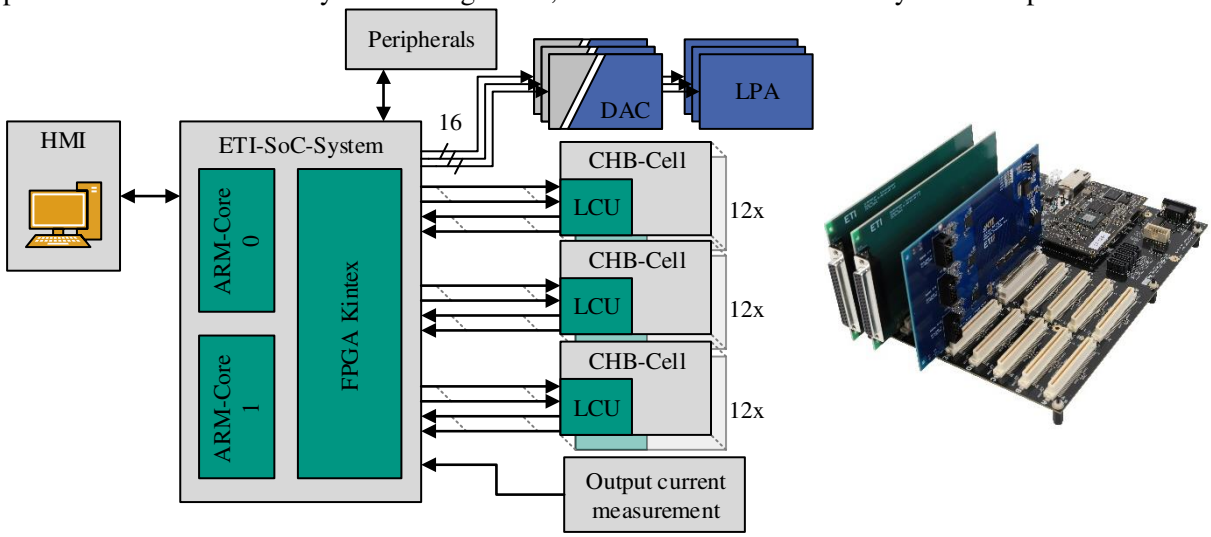


Figure 16: Control structure of the PHIL-system (left); implemented *ETI-SoC-System* (right)

The HMI is written in *LabView* and allows a simple communication with the *ETI-SoC-System* [12]. The *ETI-SoC-System* is the central control unit, shown in Figure 16 (right). It is based on a mainboard with eight expansion boards. The computing unit is the System-On-Module (SOM) *PicoZed 7030* from *AVNET* with the System-on-Chip *Zynq7000* from *Xilinx*. The developed software structure of the ETI-SoC-System is described in [13]. The ETI-SoC-System communicates over fiber optical cables with the CHB-Cells. A self-developed serial protocol with two different data channels, a slow and a high-speed channel, is implemented. The slow channel is used to transmit general information with a maximum of 16 integer variables in both directions and has a cycle period of 16 µs. The high-speed channel is used to transmit switching states to each CHB-Cell. The maximum delay of this channel is 200 ns. Thus, only a low dead time occurs for the communication within the closed loop of the PHIL system. The set point for the LPA is generated with the digital-analog converter *LTC1667* from *Analog Devices* with a sampling rate of 50 MS per second and settling time of only 20 ns. A digital isolator IC ensures the galvanic isolation, with a propagation delay of only 11 ns.
Under consideration of the bandwidth of the single power electronic units and the dead time of all system parts, a simulation model was developed to proof the practicability of the system. In Figure 17 the simulated three-phase output voltage v_{x0} of the system, the voltage of the CHB-cells $v_{chb,x0}$ and the LPA voltage $v_{LINAMPx}$ are depicted. As can be seen, the LPA is able to compensate the square wave output voltage of the CHB-cells and thus a smooth output voltage can be generated.

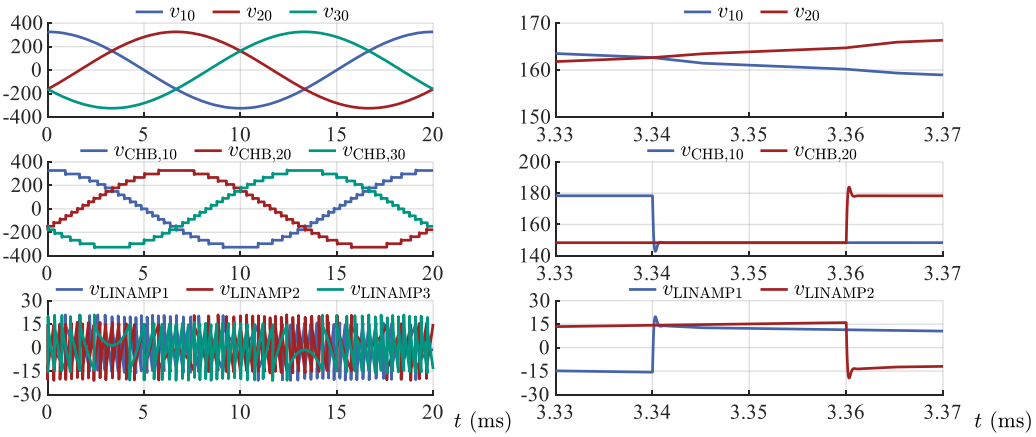


Figure 17: Simulation results of the three-phase output voltage v_{x0} of the system, the voltage of the CHB-cells $v_{chb,x0}$ and the LPA voltage $v_{LINAMPx}$, left: observation period 20ms; right: observation period 40 µs

In Figure 18 the implemented system is depicted. In the front, the ETI-SoC-System as well as 18 CHB-Cell boards are located. In the back three LPAs, the Active-Front-End, for the supply of the system, and the terminals are placed.

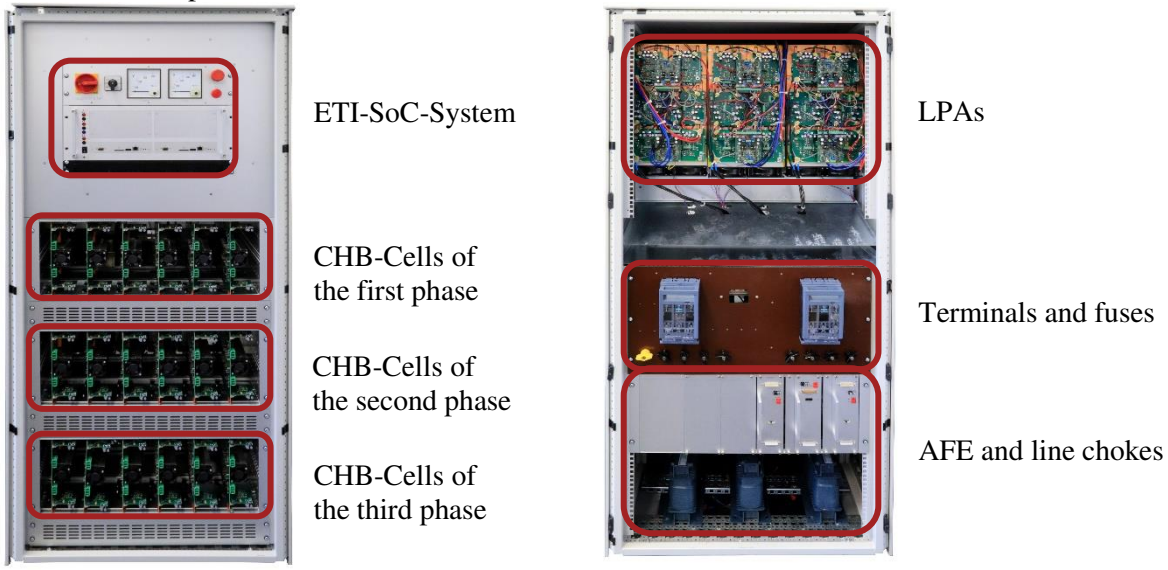


Figure 18: Implemented SH-CHB converter; front view (left) and back view (right)

Conclusion

This paper presents a new Series Hybrid Cascaded H-Bridge converter for PHIL-systems. First, a short outline of the different hybrid converter concepts is given. Subsequently, the new SH-CHB is introduced. The SH-CHB converter is the first three-phase SHC with a high output power of 60 kVA, an output voltage of 400 VAC or 1000 VDC and an output frequency of 60 kHz. It is used to emulate different grid situations. In addition, the PHIL-system is able to do an impedance spectroscopy of converters with sinusoidal test signals up to 60 kHz. This is possible due to a new interconnection concept of the LPA and the CHB-Cells, which allows a short feedback path of the LPA. Through this, the developed converter can provide higher output frequencies compared to converters based on previous concepts [6–8]. Furthermore, all important parts of the PHIL-systems are described, consisting of the CHB-Cell, the LPA and the control structure. The CHB-Cell is built up with a 60 kHz LLC-converter, an output MOSFET H-Bridge and a LCU. On the LCU a new algorithm is implemented, which facilitates an automatic switching frequency adaptation for the LLC resonant part of the CHB-Cell. Besides that, a new Linear Power Amplifier (LPA) concept is presented. With this new concept, a LPA was realized with a maximum slew rate of 500 V/µs, a large signal -3 dB bandwidth of 105 kHz and a maximum dead time of only 200 ns. Experimental results of the LPA and the CHB-Cell are illustrated, which proof the functionality of the single system parts.
Summing up, the presented CH-CHB converter can be used for a wide field of applications like emulation of grids, long cables, etc. as well as for impedance spectroscopy of converters to analyze the behavior of the converters in different grid situations.

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