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ones by checking the magnitude of the equalizer parameter vector. These results have been developed with the intention of aiding further research into developing initialization tactics and parameter constraints designed to guarantee the desirable global convergence of blind equalization algorithms.

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# A New Variable Fractional Sample Delay Filter with Nonlinear Interpolation

Ging-Shing Liu and Che-Ho Wei

*Abstract*—**This paper presents a finite impulse response (FIR) filter that can synthesize any fractional sample delay by nonlinear interpolation technique. Analytically closed-form solutions for the tap weights of such an FIR filter and their frequency responses are presented.**

## I. Introduction

In signal processing applications, linear phase shifter or constant delay of a signal waveform is often desired. Delaying a signal by integer multiples of the sampling period can be easily realized by cascading unit-delay elements. However, for some applications, it may be desirable to delay a signal by a fractional multiples of the sampling period. In this case, the signal must be interpolated to obtain new samples of the waveform at noninteger sampling instants. The process is considerably more difficult [1], [2].

Application in which such noninteger delays in the signal waveform are required often occurs when some digital system must interface with other digital systems that are not clocked synchronously. In general, to transfer digital samples from one system to another system with the same clock rate but separate clocks would require an interpolator or a first in–first out buffer to compensate for the delay time between these clocks. For nonsynchronous clocks of nearly the same frequency, the length of the required buffer is determined by the maximum difference in clock frequencies. Several digital signal processing techniques, such as the multirate signal processing method [3] and the minimum mean-square error method [1], have been adopted to solve this problem.

Given an equally spaced data sequence of finite length, there are many interpolation techniques capable of estimating the sample value between the available discrete samples. Interpolation near the center of a set of evenly spaced samples is best accomplished by using central differences. There are many interpolation formulas using central differences. Stirling's formula is one of the most commonly used methods [4]. For real-time transmitted data sequences, which may be of infinite length, the concept of Stirling's formula for central difference interpolation can be generalized.

In this paper, by using this interpolation concept, a new fractional sample delay filter is proposed. It can buffer and delay a real-time transmitted data sequence by a fractional sample period. It can be implemented by a single-rate FIR filter whose coefficients are explicit functions of the delay time. This filter can be used as a digital interpolator capable of compensating for the delay time between the echo canceller output and the receiver input for the V.32 full-duplex modem or the U-transceiver in digital subscriber loops (DSL). Analytically closed-form solutions for the filter coefficients are derived. Frequency responses of the delay filter are then computed and compared versus the design parameters.

## II. Design Method

Consider a polynomial $x(t)$ of degree $N$ given by

$$x(t) = a_0 + a_1 t + a_2 t^2 + a_3 t^3 + \cdots + a_N t^N = \sum_{k=0}^{N} a_k t^k \quad (1)$$

passing through $(N+1)$ different points $(t_n, x_n)$, where $n = 0, 1, 2, \cdots, N$. It is well known that coefficients $\{a_k\}$ can be solved by Cramer's rule as $a_k = \Delta_k / \Delta$ $(k = 0, 1, 2, \cdots, N)$, where $\Delta$ is the Vandermonde determinant given by

$$\Delta = \det \begin{vmatrix} 1 & t_0 & t_0^2 & \cdots & t_0^k & \cdots & t_0^N \\ 1 & t_1 & t_1^2 & \cdots & t_1^k & \cdots & t_1^N \\ & & \cdots & & & & \\ 1 & t_N & t_N^2 & \cdots & t_N^k & \cdots & t_N^N \end{vmatrix} = \prod_{0 \le i < j \le N} (t_j - t_i) \quad (2)$$

and $\Delta_k$ is the determinant of a new matrix obtained by replacing the $k$th column in (2) by the column vector $(x_0, x_1, \cdots, x_N)^T$. The samples at noninteger sampling instants are directly interpolated by such a polynomial. It is worth noting that these $(N+1)$ successive samples may be a fragment of a real-time transmitted sequence.

In the following, based on the simple idea, the derivation for the filter coefficients of the nonlinear interpolator with $N = 2$ and $N = 4$ will be presented.

### A. Second-Order Polynomial Interpolation ($N = 2$)

Fig. 1(a) demonstrates the function of a second-order polynomial interpolator. It is assumed that the polynomial $x(t) = a_2 t^2 + a_1 t + a_0$ passes through three equally spaced points $((n-1)T, x(n-1))$, $(nT, x(n))$ and $((n+1)T, x(n+1))$. Thus the polynomial must satisfy the following linear equation:

$$TA = X \quad (3)$$

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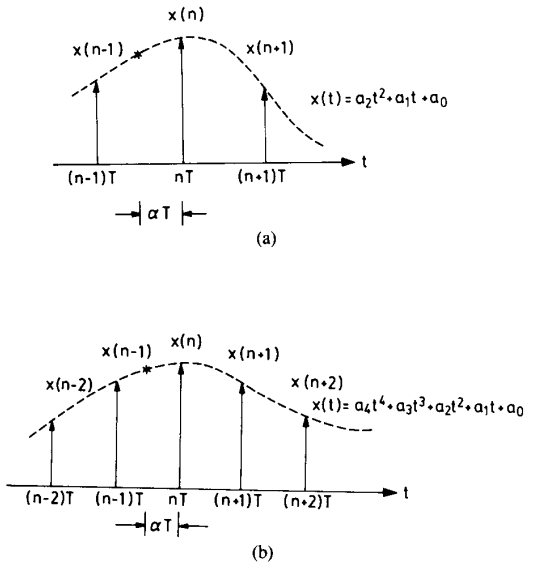


Fig. 1. Nonlinear interpolations. (a) $N = 2$. (b) $N = 4$.

where

$$\boldsymbol{T} = \begin{bmatrix} (n+1)^2T^2 & (n+1)T & 1 \\ n^2T^2 & nT & 1 \\ (n-1)^2T^2 & (n-1)T & 1 \end{bmatrix}$$

$$\boldsymbol{A} = \begin{bmatrix} a_2 \\ a_1 \\ a_0 \end{bmatrix}$$

$$\boldsymbol{X} = \begin{bmatrix} x(n+1) \\ x(n) \\ x(n-1) \end{bmatrix}. \tag{4}$$

By using Cramer's rule, vector $\boldsymbol{A}$ can be solved and rearranged with $\boldsymbol{X}$ as

$$\boldsymbol{A} = \begin{bmatrix} \frac{1}{2T^2} & -\frac{1}{T^2} & \frac{1}{2T^2} \\ \frac{(2n-1)}{2T} & \frac{4n}{2T} & -\frac{(2n+1)}{2T} \\ \frac{n(n+1)}{2} & -(n+1)(n-1) & \frac{n(n-1)}{2} \end{bmatrix} \cdot \begin{bmatrix} x(n+1) \\ x(n) \\ x(n-1) \end{bmatrix}. \tag{5}$$

The interpolated sample at time $t = (n - \alpha)T$ can be written as

$$\hat{x}(n-\alpha) = a_2t^2 + a_1t + a_0 \big|_{t=(n-\alpha)T} \tag{6}$$

where $\alpha$ denotes the fractional sample delay and $\hat{x}(n - \alpha)$ represents the estimate of the delayed replica of $x(n)$ with delay time $\alpha T$. Combining (5) and (6), the estimate $\hat{x}(n - \alpha)$ can be simplified and expressed with $\boldsymbol{X}$ as

$$\hat{x}(n-\alpha) = C_1x(n-1) + C_0x(n) + C_{-1}x(n+1)$$

where

$$C_1 = 1/2\alpha(\alpha+1)$$
$$C_0 = -(\alpha-1)(\alpha+1)$$
$$C_{-1} = 1/2\alpha(\alpha-1). \tag{7}$$

It is noted that $C_1$, $C_0$, and $C_{-1}$ are time-invariant and depend only on the delay parameter $\alpha$. Therefore, the interpolator can be implemented as a linear time-invariant FIR filter to synthesize the fractional sample delay $\alpha T$. The delay filter output, i.e., the interpolated sample at noninteger multiples of sampling period, can be expressed explicitly as a linear combination of those at integer multiples of sampling period. Fig. 2 shows the waveforms at the output of such an FIR filter with various delays ranging from 0 to $T$, where a sine wave is used as the input signal.

### *B. Fourth-Order Polynomial Interpolation ($N = 4$)*

The function of a fourth-order polynomial interpolation is illustrated in Fig. 1(b). Let the polynomial pass through five equally spaced samples. After some tedious but straightforward manipulations, a time-varying coefficient vector $\boldsymbol{A}$ is obtained. Similar to (6) and (7), the interpolated sample at $t = (n - \alpha)T$ can be determined and expressed with $\boldsymbol{X}$ as

$$\hat{x}(n-\alpha) = C_2x(n-2) + C_1x(n-1) + C_0x(n) + C_{-1}x(n+1) + C_{-2}x(n+2)$$

where

$$C_{-2} = \frac{1}{24}(\alpha+1)\alpha(\alpha-1)(\alpha-2)$$
$$C_{-1} = -\frac{1}{6}(\alpha+2)\alpha(\alpha-1)(\alpha-2)$$
$$C_0 = \frac{1}{4}(\alpha+2)(\alpha+1)(\alpha-1)(\alpha-2)$$
$$C_1 = -\frac{1}{6}(\alpha+2)(\alpha+1)\alpha(\alpha-2)$$
$$C_2 = \frac{1}{24}(\alpha+2)(\alpha+1)\alpha(\alpha-1). \tag{8}$$

The frequency response for such an FIR filter can be written as

$$\hat{H}(e^{j\omega}) = \left[\frac{1}{12}\alpha^2(\alpha^2-1)\cos(2\omega) - \frac{1}{3}\alpha^2(\alpha^2-4)\cdot\cos(\omega) + \frac{1}{4}(\alpha^2-4)(\alpha^2-1)\right] + j\left[-\frac{1}{6}\alpha(\alpha^2-1)\sin(2\omega) + \frac{1}{3}\alpha(\alpha^2-4)\sin(\omega)\right]. \tag{9}$$

For ideal fractional sample delay filter, its frequency response is $H(e^{j\omega}) = e^{-j\omega\alpha}$. The squared approximation error between $H(e^{j\omega})$ and $\hat{H}(e^{j\omega})$ can be defined as

$$\xi = |H(e^{j\omega}) - \hat{H}(e^{j\omega})|^2. \tag{10}$$

Fig. 3 plots the squared approximation error $\xi$ versus $\alpha$ and $\omega$ ($N = 4$).

### *C. Nth-Order Polynomial Interpolation ($N = 2M$)*

There are several very interesting regularities in the coefficients given in (7) and (8) for the second- and fourth-order delay filters.

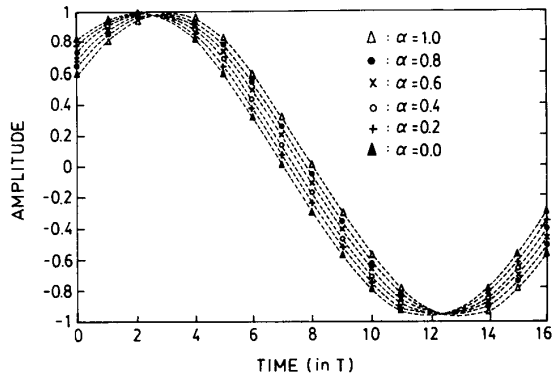


Fig. 2. Output waveforms with various delays ($N = 2$).

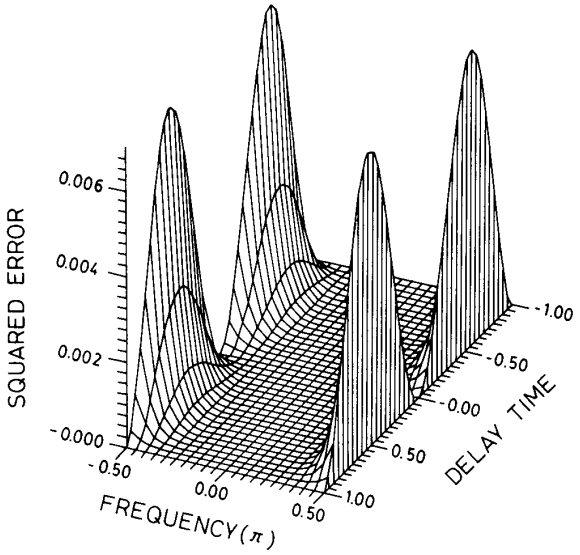


Fig. 3. Squared approximation error $\xi$ versus $\alpha$ and $\omega$ ($N = 4$).

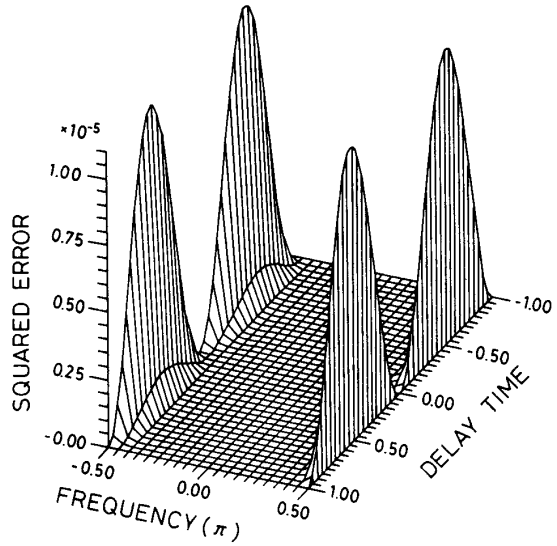


Fig. 4. Squared approximation error $\xi$ versus $\alpha$ and $\omega$ ($N = 12$).

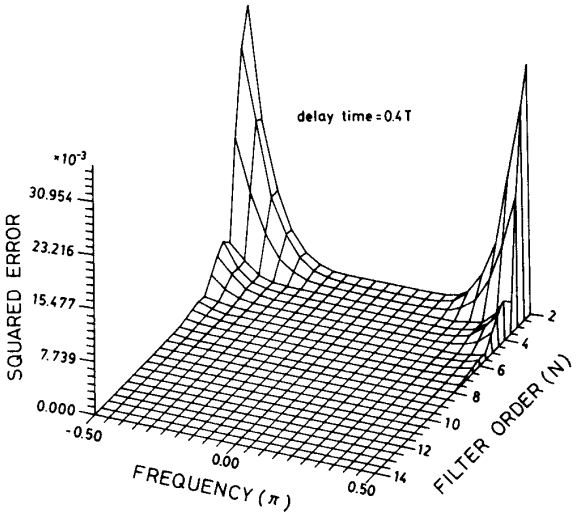


Fig. 5. Squared approximation error $\xi$ versus $N$ and $\omega$.

First, for some coefficient $C_j$, all the factors in the form of $(\alpha - i)$, except $(\alpha - j)$, will appear at the right-hand side of the equations, where index $i$ ranges from $-M$ to $M$. Second, $C_j$ equals unity when $j$ is substituted for $\alpha$ in (7) and (8). Furthermore, $C_j$ equals zero when any integer $m$ not equal to $j$ is substituted for $\alpha$, where $-M \le m \le M$. For example, letting $\alpha = 1$ in (8), we obtain

$$C_2 = 0,\ C_1 = 1,\ C_0 = 0,\ C_{-1} = 0,\ C_{-2} = 0. \qquad (11)$$

In this case, $y(n) \equiv \hat{x}(n - \alpha) = x(n - 1)$, i.e., the filter synthesizes an integer delay.

Based on these regularities, for an $N$th-order (with $N = 2M$) delay filter, a generalized closed-form solution for the filter coefficients can be derived and appears as

$$C_j = \frac{1}{(-1)^{M-j}(M + j)!(M - j)!} \prod_{\substack{i=-M \\ i \neq j}}^{M} (\alpha - i)$$

$$j = -M, -M + 1, \cdots, M - 1, M. \qquad (12)$$

Note that (7) and (8) are special cases of (12) with $M = 1 (N = 2)$ and $M = 2 (N = 4)$, respectively. Fig. 4 demonstrates the squared approximation error $\xi$ versus the delay ($\alpha$) and the frequency ($\omega$) for a higher order filter ($N = 12$). Given the same delay time $\alpha T$, Fig. 5 compares the squared approximation error versus the filter order $N$ in frequency domain.

From the numerical results shown in Figs. 3 and 4, it is found that the filter always provides nearly flat delay and magnitude responses over the band of $[-0.5\pi, +0.5\pi]$ (or $[-1/4T, +1/4T]$), where $T$ is the sampling period. For practical applications, the designer can only choose a suitable value $N$. As a rule of thumb, if the designer wants to design a programmable delay filter, which is capable of delaying a discrete sequence by fractional delay between $-MT$ and $MT$, the suitable choice of the filter order $N$ is $2M$ or more. To any specific order $N$, the higher the sampling rate, the better the linearity of the delay filter. As a compromise between

complexity and approximation error, the fourth-order ($N = 4$) delay filter is a desirable candidate for many applications.

## III. Conclusions

A new technique is presented for designing and implementing a programmable digital delay element capable of synthesizing any fractional sample delay-time $\alpha T$. This method is based on the concept of nonlinear polynomial interpolation. Derivation of the analytically closed-form solutions for the filter coefficients has been described. The resulting digital FIR filter can be implemented directly in real-time structure. The flatness of the delay response can be improved by using higher order delay filters. To any specific order $N$, the higher the sampling rate, the better the linearity of the delay filter.

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# A Theoretical Approach to the Design of A/D Converter by Means of Schmitt Triggers

G. Di Cataldo and G. Palumbo

*Abstract*—**In this paper a neural A/D converter that avoids the incorrect conversion of the Hopfield A/D is proposed. The converter proposed is noteworthy for its conversion speed as it relates to its size. The conversion procedure is based on a theorem, included in this paper, which starts from the Smith and Portmann suggestion relative to the study of the Hopfield neural network by means of Schmitt triggers.**

## I. Introduction

Neural networks, based on a massive parallelism of simple processors (artificial neurons) [1], are well established; however, studies in this area have been revitalized due to advances in VLSI technologies [2]-[6]. In particular the Hopfield neural network, composed of one-layer neurons fully connected by feedback resistors, is widely applicable in electronic computing. Because of the simplicity of the network structure and the convergence in the time-domain behavior [7], [8], it can powerfully perform associative memory, patter classification, and optimization [9].

The realization of an A/D converter is a specific problem of optimization for which a Hopfield neural network can be built (Fig. 1). An example of a four-bit A/D converter is reported in [10]. The actual transfer characteristic of an A/D converter, based on a Hopfield neural network, shows strong nonlinearity due to amplifier mismatches and to the initial state of the network. In particular, in a neural A/D converter, the problem deriving from the initial state of the network can simply be eliminated by resetting the network for each sample date. However, this solution is not sufficient to avoid hysteresis and incorrect encoding of the Hopfield A/D converter [11]-[14].

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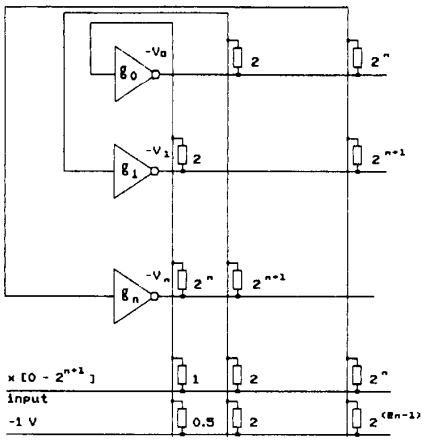


Fig. 1. Hopfield A/D converter.

Smith and Portmann, referring to the previous work of Cattermole [11], have proposed the realization of converters that are modified with respect to the original Hopfield neural network, in order to avoid the above-mentioned problems. In particular they point out that by redesigning a Hopfield A/D converter as a Type I serial encoder, we can assure stability and correct encoding. This solution leads to an A/D converter that takes a time $n \cdot \tau$ (where $\tau$ is the settling time for each neuron) [13].

In this paper we present a Type I serial encoder in which the speed operation is increased and takes a time of $2(\tau + \Delta T)$ with $\Delta T \ll \tau$, instead of $n \cdot \tau$. In our analysis we will make use, as suggested in [13], of an equivalent network made of Schmitt triggers designed so as to have different settling times.

## II. The Proposed A/D Converter

To better understand the hysteresis and incorrect encoding of Hopfield neural networks, transformation into an equivalence feedback electric circuit realized by means of Schmitt triggers has been proposed [13] (Fig. 2). We started from this suggestion to develop our circuit. Our converter, reported in Fig. 3, is derived from the circuit of Fig. 1 operating a right shift for each trigger characteristic equal to $2^{i-1}$. Moreover, we have assumed that for trigger settling times $\tau_{i+1} < \tau_1$ holds [15], i.e., the triggers respond with a decreasing speed to the decrease in the bit weight that each represents. We point out that the resulting network has an ideal sum node (i.e., a sum node with zero response time).

The solution here discussed is based on a theorem that assures the correct theoretical conversion of circuit. The proof is reported in the Appendix.

*Theorem:*

*Hp:* 1) The circuit in Fig. 3(a) has $n$ Schmitt triggers that have settling times of $\tau_{i+1} < \tau_1$;
2) the Schmitt trigger characteristic is shown in Fig. 3(b);
3) the network has a zero initial state: $V_{n-1}(0) = \cdots = V_0(0) = 0$;
4) $V_{\text{in}}$ is constant for $0 \le t \le \tau_0$.