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A new ZVT-ZCT-PWM DC-DC converter — Source link

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A New ZVT–ZCT–PWM DC–DC Converter

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***Abstract*—In this paper, a new active snubber cell is proposed to contrive a new family of pulse width modulated (PWM) converters. This snubber cell provides zero voltage transition (ZVT) turn on and zero current transition (ZCT) turn off together for the main switch of a converter. Also, the snubber cell is implemented by using only one quasi resonant circuit without an important increase in the cost and complexity of the converter. New ZVT–ZCT–PWM converter equipped with the proposed snubber cell provides most the desirable features of both ZVT and ZCT converters presented previously, and overcomes most the drawbacks of these converters. Subsequently, the new converter can operate with soft switching successfully at very wide line and load ranges and at considerably high frequencies. Moreover, all semiconductor devices operate under soft switching, the main devices do not have any additional voltage and current stresses, and the stresses on the auxiliary devices are at low levels. Also, the new converter has a simple structure, low cost and ease of control. In this study, a detailed steady state analysis of the new converter is presented, and this theoretical analysis is verified exactly by a prototype of a 1-kW and 100-kHz boost converter.**

***Index Terms*—Active snubber cells, soft switching, zero current transition, zero voltage transition.**

I. Introduction

SWITCHING frequency should be increased by decreasing switching losses to achieve higher power density and faster transient response in well known pulse width modulated (PWM) dc–dc converters. This aim can be realized by using soft switching (SS) techniques instead of hard switching (HS) techniques. SS techniques are implemented by snubber cells, and basically provide zero voltage switching (ZVS) or zero current switching (ZCS) for semiconductor devices in these converters [1]–[14].

The normal zero voltage transition (ZVT) PWM converter [1] had been presented to implement the ZVS turn on process of the main switch during a very short ZVT time provided with a resonance. In this converter, the main switch and the main diode operate under SS conditions, and the auxiliary switch is turned on with ZCS. However, the auxiliary switch is turned off under HS, and the operation of the circuit is strongly dependent on line and load conditions due to the turn off snubber capacitor. A number of papers concerning ZVT had been proposed to solve the problems of the normal ZVT converter in recent years [4]–[7], and [9]–[13].

The conventional zero current transition (ZCT) PWM converter [2] had been presented to realize the ZCS turn off process of the main switch through a resonance. Basically, the main switch is turned off and the main diode is turned on under SS, and the auxiliary switch is turned on with ZCS in this converter. But, the main switch is turned on and the main diode is turned off under HS simultaneously, and a short circuit through these devices occurs at the same time. Also, the auxiliary switch is turned off under HS. To overcome the drawbacks of the normal ZCT converter, a lot of papers had been proposed [3], and [9].

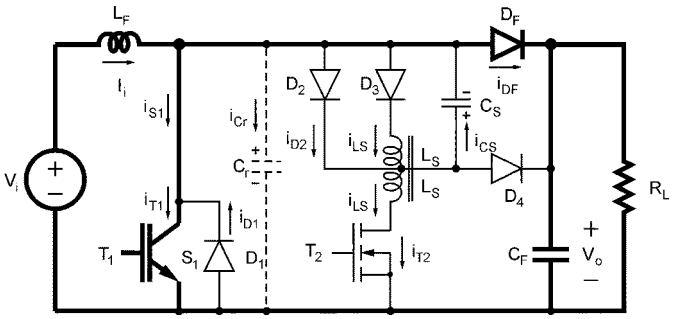

Fig. 1. New ZVT–ZCT–PWM boost converter.

Subsequently, the ZVT technique provides basically a perfect turn on process for the main switch of a converter by using a quasi resonant circuit. Also, the ZCT technique provides a perfect turn off process in a similar manner. In both processes, no overlap between the voltage and the current of the main switch and so no switching losses take place. Unfortunately, the turn off process of a ZVT converter and the turn on process of a ZCT converter are not perfect, and they have many problems mentioned above. The improved or new ZVT and ZCT converters had tried to solve these problems in different manners. But, these processes have still some drawbacks and some switching losses generally. Consequently, to use the ZVT and ZCT techniques together in one converter seems the best solution for the whole of these problems without a significant increase in the cost and the complexity of the converter.

Recently, a zero current and zero voltage transition (ZCZVT) commutation cell was presented in [9] to provide ZVT turn on and ZCT turn off together for the main switch. It has a lot of good features, but has some drawbacks at the same time, such as, the input voltage smaller than half the output voltage for its operation, an additional current stress on the main switch, and the existence of four half resonant periods taking long time and causing high losses over one switching cycle.

In this study, a new active snubber cell is proposed to contrive a new family of PWM converters. This snubber cell provides perfectly ZVT turn on and ZCT turn off together for the main switch of a converter by using only one quasi resonant circuit without an important increase in the cost and complexity of the converter. New ZVT–ZCT–PWM converter equipped with the proposed snubber cell implements most the desirable features of both the ZVT and ZCT converters presented previously, and

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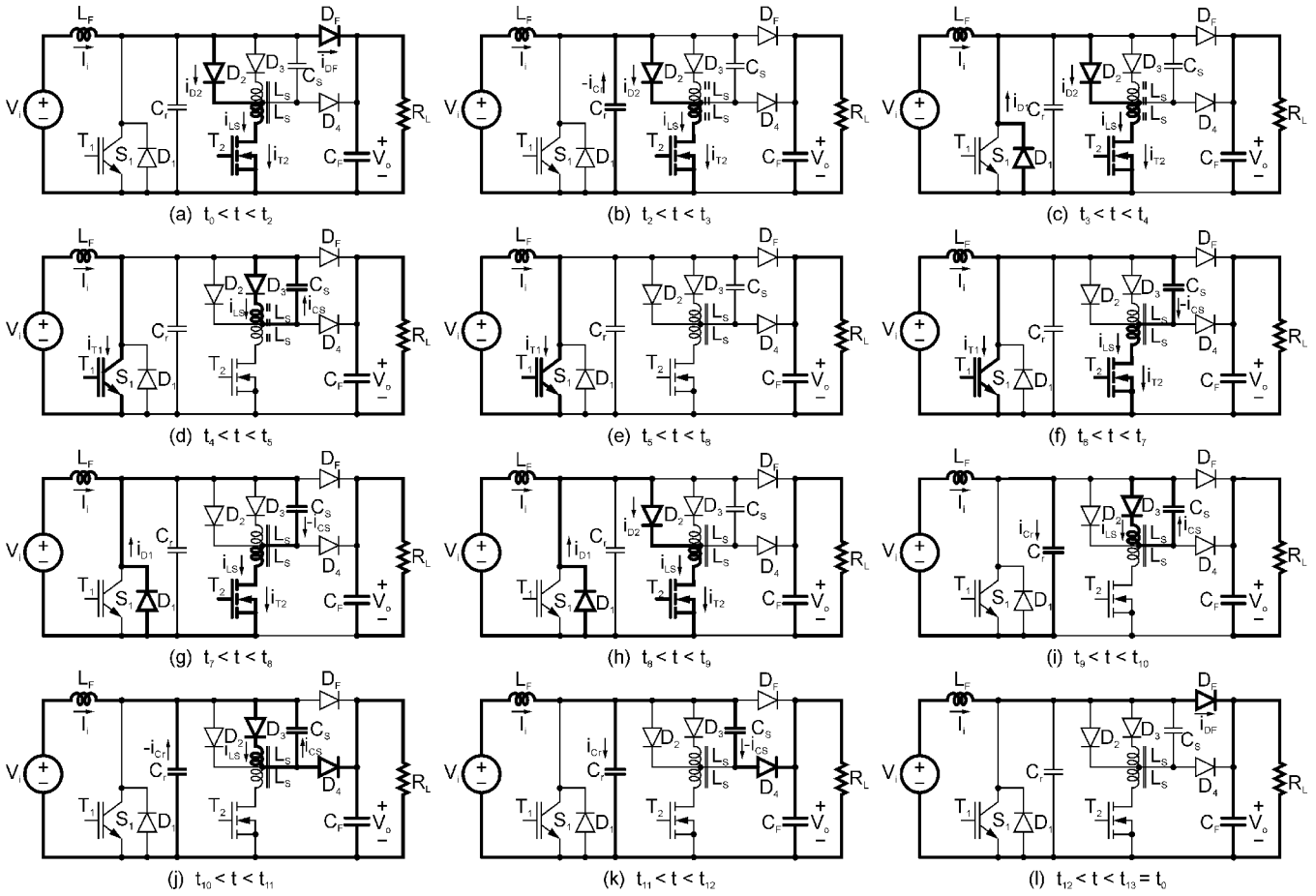

Fig. 2. Equivalent circuits of the operation stages in the proposed converter.

overcomes most the drawbacks of these converters. The steady state operation of the new converter is analyzed in detail, and this theoretical analysis is verified exactly by a prototype of a 1-kW and 100-kHz boost converter.

II. Operation Principles and Analysis

A. Definitions and Assumptions

The circuit scheme of new ZVT–ZCT–PWM boost converter is given in Fig. 1. The proposed snubber cell consists of a center tapped and magnetic coupled snubber inductor $(2L_s)$, a snubber capacitor (C_s), a resonant capacitor (C_r), an auxiliary transistor (T_2), and four auxiliary diodes (D_1, D_2, D_3 and D_4). The diode D_1 can be considered the body diode of the main transistor T_1. The parasitic capacitors of the semiconductor devices T_1, D_F, D_1 and D_4 are incorporated the capacitor C_r, and are sufficient generally for the operation of the converter. Thus, C_r can be assumed the sum of these parasitic capacitors.

To simplify the steady state analysis of the circuit shown in Fig. 1 during one switching cycle, it is assumed that input and output voltages and input current are constant, and semiconductor devices and resonant circuits are ideal. But, the reverse recovery time of the main diode is taken into account.

B. Operation Stages

Twelve stages occur over one switching cycle in the steady state operation of the proposed converter. The equivalent circuit schemes of the operation stages are given in Fig. 2(a)–(l) respectively, and key waveforms concerning these stages are shown in Fig. 3. The detailed analysis of this converter is presented as follows.

1) Stage 1 [$t_0 < t < t_2$: Fig. 2(a)]: At $t = t_0$, $i_{T1} = 0$, $i_{T2} = 0$, $i_{DF} = I_i$, $i_{Ls} = 0$, $v_{Cr} = V_o$ and $v_{Cs} = 0$ are valid. The main transistor T_1 and the auxiliary transistor T_2 are in the off state, and the main diode D_F is in the on state and conducts the input current I_i. At the moment a turn on signal is applied to the gate of T_2, this stage begins. T_2 current rises and D_F current falls simultaneously and linearly during this stage. T_2 current flows through the diode D_2 and the lower half of the snubber inductor at the same time. For this stage, the equations

$$i_{Ls} = i_{D2} = i_{T2} = \frac{V_o}{L_s}(t - t_0) \tag{1}$$

$$i_{DF} = I_i - i_{Ls} = -\frac{V_o}{L_s}(t - t_0) + I_i \tag{2}$$

are derived. At first, i_{T2} reaches I_i and i_{DF} falls to 0 at t_1. Later i_{DF} reaches $-I_{rr}$ at t_2 thus D_F is turned off and this stage stops. Thus

$$t_{01} = \frac{L_s}{V_o} I_i \tag{3}$$

$$t_{12} = t_{rr} = \frac{L_s}{V_o} I_{rr} \tag{4}$$

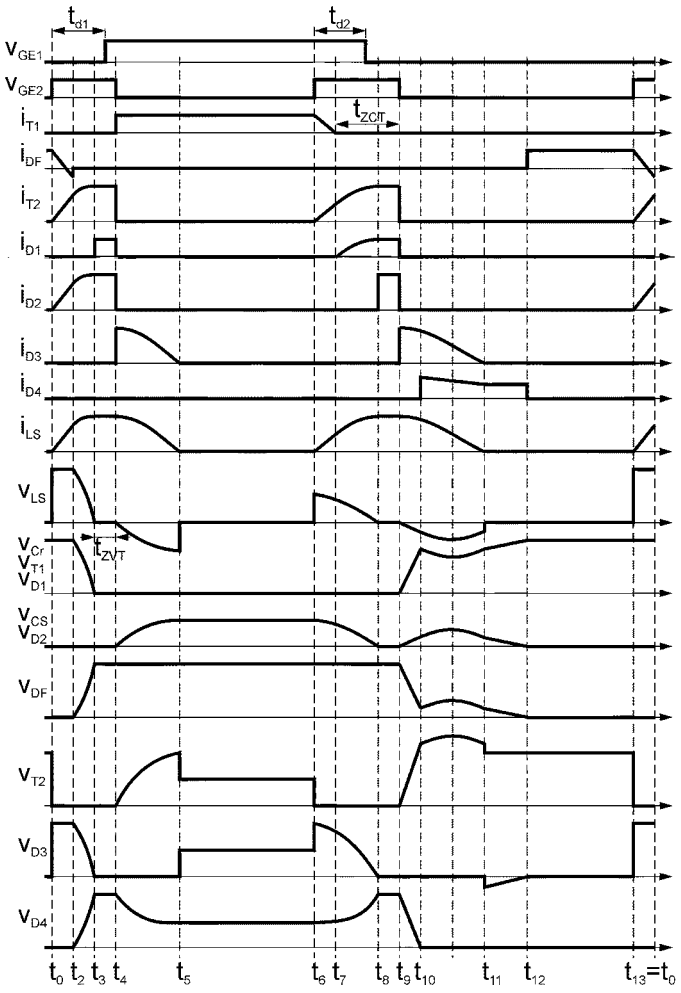

Fig. 3. Key waveforms concerning the operation stages in the proposed converter.

can be written. Here I_{rr} and t_{rr} are the reverse recovery current and the reverse recovery time of D_F respectively, for the values of $I_F = I_i$ and $-di/dt = -V_o/L_s$.

Therefore, T_2 is turned on with ZCS due to the lower L_s, and D_F is turned off with nearly ZCS and ZVS through the lower L_s and C_r in this stage. The currents I_i and I_{rr} are commutated to T_2 and the lower L_s during this stage.

2) Stage 2 [$t_2 < t < t_3$: Fig. 2(b)]: When $i_{T1} = 0$, $i_{T2} = I_i + I_{rr}$, $i_{DF} = 0$, $i_{Ls} = I_i + I_{rr}$, $v_{Cr} = V_o$ and $v_{Cs} = 0$ are existent at $t = t_2$ a resonance between C_r and the lower L_s starts via the path $C_r - D_2 - L_s - T_2$ under the input current I_i. The initial current of the lower L_s is $I_i + I_{rr}$. For this resonance

$$\begin{aligned} i_{Ls} &= i_{D2} \\ &= i_{T2} \\ &= I_{rr}\cos(\omega_1(t-t_2)) + \frac{V_o}{Z_1}\sin(\omega_1(t-t_2)) + I_i \end{aligned} \quad (5)$$

$$\begin{aligned} v_{Cr} &= v_{T1} \\ &= v_{D1} \\ &= V_o\cos(\omega_1(t-t_2)) - Z_1 I_{rr}\sin(\omega_1(t-t_2)) \end{aligned} \quad (6)$$

are achieved. At $t = t_3$, v_{Cr} becomes 0 and this stage is finished. Thus, the transfer of the energy stored in C_r to the inductor is completed. The current and energy values of the lower L_s reach their maximum levels at the same time. From (5) and (6)

$$t_{23} = \frac{1}{\omega_1}\mathrm{arctg}\frac{V_o}{Z_1 I_{rr}} \quad (7)$$

$$\begin{aligned} i_{Ls}(t_3) &= I_{Ls3} \\ &= I_{Ls\max} \\ &= I_i + \sqrt{I_{rr}^2 + \left(\frac{V_o}{Z_1}\right)^2} \end{aligned} \quad (8)$$

$$\begin{aligned} W_{Ls}(t_3) &= W_{Ls3} \\ &= W_{Ls\max} \\ &= \frac{1}{2}L_s I_{Ls\max}^2 \end{aligned} \quad (9)$$

are derived. In these equations

$$\omega_1 = \frac{1}{\sqrt{L_s C_r}} \quad (10)$$

$$Z_1 = \sqrt{\frac{L_s}{C_r}} \quad (11)$$

are valid.

3) Stage 3 [$t_3 < t < t_4$: Fig. 2(c)]: At the beginning of this stage, $i_{T1} = 0$, $i_{T2} = I_{Ls\max}$, $i_{DF} = 0$, $i_{Ls} = I_{Ls\max}$, $v_{Cr} = 0$ and $v_{Cs} = 0$ are valid. Just after v_{Cr} becomes 0 at t_3, the diode D_1 is turned on and this stage begins. D_1 conducts the excess of $I_{Ls\max}$ from I_i during this stage. The time period of this stage is the zero voltage transition (ZVT) time of the main transistor T_1. For this state

$$i_{Ls} = i_{D2} = i_{T2} = I_{Ls\max} \quad (12)$$

$$i_{D1} = I_{Ls\max} - I_i \quad (13)$$

$$t_{34} = t_{ZVT} \quad (14)$$

can be written. At the instant the gate signal of T_2 is removed at $t = t_4$ this stage finishes. The turn on signal of T_1 should be applied to its gate during ZVT.

4) Stage 4 [$t_4 < t < t_5$: Fig. 2(d)]: Before $t = t_4$, $i_{T1} = 0$, $i_{T2} = I_{Ls\max}$, $i_{DF} = 0$, $i_{Ls} = I_{Ls\max}$, $v_{Cr} = 0$ and $v_{Cs} = 0$ are valid. As the gate signal of T_2 is removed at t_4, T_2 is turned off, T_1 is turned on and begins to conduct I_i, and a resonance between the upper L_s and C_s starts by the way of $D_3 - L_s - C_s$. For this resonance

$$i_{Ls} = i_{D3} = I_{Ls\max}\cos(\omega_2(t-t_4)) \quad (15)$$

$$v_{Cs} = v_{D2} = \frac{v_{T2}}{2} = Z_2 I_{Ls\max}\sin(\omega(t-t_4)) \quad (16)$$

are derived. At $t = t_5$, i_{Ls} becomes 0, and thus this resonance and this stage are finished. Therefore, the energy stored in the snubber inductor is transferred to the snubber capacitor completely. The voltage and energy values of C_s reach their maximum levels at the same time. In this state, the equations

$$t_{45} = \frac{1}{\omega_2}\frac{\pi}{2} \quad (17)$$

$$v_{Cs}(t_5) = V_{Cs5} = V_{Cs\max} = Z_2 I_{Ls\max} \quad (18)$$

$$\begin{aligned} W_{Cs}(t_5) &= W_{Cs5} = W_{Cs\max} = W_{Ls\max} \\ &= \frac{1}{2}C_s V_{Cs\max}^2 = \frac{1}{2}L_s I_{Ls\max}^2 \end{aligned} \quad (19)$$

are obtained. In these equations

$$\omega_2 = \frac{1}{\sqrt{L_s C_s}} \quad (20)$$

$$Z_2 = \sqrt{\frac{L_s}{C_s}} \tag{21}$$

are existent. Therefore, the main transistor T_1 is perfectly turned on under ZVS provided by ZVT, and the auxiliary transistor T_2 is turned off under ZVS through the snubber capacitor C_s in this stage.

5) Stage 5 [$t_5 < t < t_6$: Fig. 2(e)]: This stage is the on state of the normal PWM converter. For this stage

$$i_{T1} = I_i \tag{22}$$

can be written.

6) Stage 6 [$t_6 < t < t_7$: Fig. 2(f)]: Before this stage, $i_{T1} = I_i$, $i_{T2} = 0$, $i_{DF} = 0$, $i_{Ls} = 0$, $v_{Cr} = 0$ and $v_{Cs} = V_{Cs\max}$ are existent. At $t = t_6$ as a turn on signal is applied to the gate of T_2,. a resonance between C_s and the lower L_s starts via the path $C_s - L_s - T_2 - T_1$. During this stage, T_2 current rises and T_1 current falls simultaneously. At $t = t_7$, T_2 current reaches I_i and T_1 current drops to zero, and this stage finishes. The equations

$$\begin{aligned} i_{Ls} &= i_{T2} \\ &= \frac{V_{Cs\max}}{Z_2}\sin(\omega_2(t - t_6)) \end{aligned} \tag{23}$$

$$\begin{aligned} v_{Cs} &= v_{D2} \\ &= V_{Cs\max}\cos(\omega_2(t - t_6)) \end{aligned} \tag{24}$$

$$\begin{aligned} t_{67} &= \frac{1}{\omega_2}\arcsin\frac{Z_2 I_i}{V_{Cs\max}} \\ &= \frac{1}{\omega_2}\arcsin\frac{I_i}{I_{Ls\max}} \end{aligned} \tag{25}$$

are formed for this stage. Here T_2 is turned on with ZCS through L_s.

7) Stage 7 [$t_7 < t < t_8$: Fig. 2(g)]: At $t = t_7$, $i_{T1} = 0$, $i_{T2} = I_i$, $i_{DF} = 0$, $i_{Ls} = I_i$, $v_{Cr} = 0$ and $v_{Cs} = V_{Cs7}$ are valid. Just after T_1 current drops to zero at t_7, D_1 is turned on and this stage begins. During this stage, the resonance started before continues by the way of $C_s - L_s - T_2 - D_1$. At $t = t_8$ as v_{Cs} falls to zero, the current and energy values of the lower L_s reach their maximum levels, and this stage finishes. For this stage

$$\begin{aligned} i_{Ls} &= i_{T2} \\ &= \frac{V_{Cs\max}}{Z_2}\sin(\omega_2(t + t_{67} - t_7)) \end{aligned} \tag{26}$$

$$\begin{aligned} v_{Cs} &= v_{D2} \\ &= V_{Cs\max}\cos(\omega_2(t + t_{67} - t_7)) \end{aligned} \tag{27}$$

$$t_{78} = \frac{1}{\omega_2}\left(\frac{\pi}{2} - \arcsin\frac{I_i}{I_{Ls\max}}\right) \tag{28}$$

$$\begin{aligned} i_{Ls}(t_8) &= I_{Ls8} \\ &= I_{Ls\max} \\ &= \frac{V_{Cs\max}}{Z_2} \end{aligned} \tag{29}$$

are obtained. D_1 conducts the excess of i_{Ls} from I_i during this stage. Also, the sum of the time periods t_{67} and t_{78} is equal to $(\pi/2)/\omega_2$.

8) Stage 8 [$t_8 < t < t_9$: Fig. 2(h)]: At $t = t_8$, $i_{T1} = 0$, $i_{T2} = I_{Ls\max}$, $i_{DF} = 0$, $i_{Ls} = I_{Ls\max}$, $v_{Cr} = 0$ and $v_{Cs} = 0$ are existent. Just after v_{Cs} becomes 0 at t_8 the diode D_2 is turned on and this stage begins. During this stage, D_1 conducts the excess of $I_{Ls\max}$ from I_i. The sum of the time periods of Stages 7 and 8, in which D_1 is in the on state, is the zero current transition (ZCT) time of T_1. For this state

$$i_{Ls} = i_{D2} = i_{T2} = I_{Ls\max} \tag{30}$$

$$i_{D1} = I_{Ls\max} - I_i \tag{31}$$

$$t_{78} + t_{89} = t_{ZCT} \tag{32}$$

can be written. This stage finishes at the moment the gate signal of T_2 is removed at t_9. The turn on signal of T_1 should be removed from its gate during ZCT.

9) Stage 9 [$t_9 < t < t_{10}$: Fig. 2(i)]: Before $t = t_9$, $i_{T1} = 0$, $i_{T2} = I_{Ls\max}$, $i_{DF} = 0$, $i_{Ls} = I_{Ls\max}$, $v_{Cr} = 0$ and $v_{Cs} = 0$ are existent. When the turn on signal of T_2 is removed from its gate at t_9, T_2 is turned off and this stage starts. Two different closed circuits take place during this stage. C_r is charged by I_i linearly in the one circuit. A resonance between the upper L_s and C_s begins via the path $D_3 - L_s - C_s$ with the initial current $I_{Ls\max}$ of L_s in the other circuit. When the sum of the voltages of v_{Cr} and v_{Cs} reaches the output voltage V_o this stage is finished. The equations

$$v_{Cr} = \frac{I_i}{C_r}(t - t_9) \tag{33}$$

$$i_{Ls} = i_{D3} = I_{Ls\max}\cos(\omega_2(t - t_9)) \tag{34}$$

$$v_{Cs} = v_{D2} = Z_2 I_{Ls\max}\sin(\omega_2(t - t_9)) \tag{35}$$

are formed for this stage. If it is assumed that C_s is very larger than C_r and thus C_s is charged by $I_{Ls\max}$ linearly, the time period of this stage is derived as

$$t_{910} \cong \frac{C_s C_r}{C_s I_i + C_r I_{Ls\max}} V_o. \tag{36}$$

Therefore, the main transistor T_1 is perfectly turned off under ZCS provided by ZCT, and the auxiliary transistor T_2 is turned off under ZVS through the capacitors C_s and C_r in this stage.

10) Stage 10 [$t_{10} < t < t_{11}$: Fig. 2(j)]: At the beginning of this stage, $i_{T1} = 0$, $i_{T2} = 0$, $i_{DF} = 0$, $i_{Ls} = I_{Ls10}$, $v_{Cr} = V_o - V_{Cs10}$ and $v_{Cs} = V_{Cs10}$ are valid. As the sum of v_{Cr} and v_{Cs} reaches V_o at t_{10} the diode D_4 is turned on and this stage begins. In this stage, a resonance between the upper L_s and C_r and C_s takes place under the input current I_i. At the instant i_{Ls} becomes 0 at t_{11} this resonance and this stage are finished. Thus, the energy stored in the inductor is transferred to the capacitors and the load completely in this stage. For this stage

$$\begin{aligned} i_{Ls} &= (I_{Ls10} - I_i)\cos(\omega_3(t - t_{10})) \\ &\quad - \frac{V_{Cs10}}{Z_3}\sin(\omega_3(t - t_{10})) + I_i \end{aligned} \tag{37}$$

$$\begin{aligned} v_{Cs} &= V_o - v_{Cr} \\ &= V_{Cs10}\cos(\omega_3(t - t_{10})) \\ &\quad + Z_3(I_{Ls10} - I_i)\sin(\omega_3(t - t_{10})) \end{aligned} \tag{38}$$

$$\begin{aligned} t_{1011} = \frac{1}{\omega_3}\Bigg(&\arcsin\frac{Z_3 I_i}{\sqrt{Z_3^2(I_{Ls10} - I_i)^2 + V_{Cs10}^2}} \\ &+ \operatorname{arctg}\frac{Z_3(I_{Ls10} - I_i)}{V_{Cs10}}\Bigg) \end{aligned} \tag{39}$$

are derived. In these equations

$$C_3 = C_r + C_s \tag{40}$$

$$\omega_3 = \frac{1}{\sqrt{L_s C_3}} \tag{41}$$

$$Z_3 = \sqrt{\frac{L_s}{C_3}} \tag{42}$$

are valid.

11) Stage 11 [$t_{11} < t < t_{12}$: Fig. 2(k)]: At $t = t_{11}$, $i_{T1} = 0$, $i_{T2} = 0$, $i_{DF} = 0$, $i_{Ls} = 0$, $v_{Cr} = V_o - V_{Cs11}$ and $v_{Cs} = V_{Cs11}$ are existent. During this stage, C_r is charged and C_s is decharged as parallel with C_r, under the constant input current I_i. When C_r voltage reaches V_o and C_s voltage falls to zero simultaneously at t_{12}, D_F is turned on and this stage finishes. The equations

$$v_{Cs} = V_{Cs11} - \frac{I_i}{C_3}(t - t_{11}) \tag{43}$$

$$t_{1112} = \frac{C_3}{I_i} V_{Cs11} \tag{44}$$

can be written for this stage. The main diode is turned on under ZVS through C_s and C_r at the end of this stage.

12) Stage 12 [$t_{12} < t < t_{13}$: Fig. 2(l)]: This stage is the off state of the normal PWM converter. For this stage

$$i_{DF} = I_i \tag{45}$$

can be written. Consequently, at the moment the turn on signal of T_2 is applied again to its gate at $t = t_{13} = t_0$ this switching cycle is completed and another cycle begins.

III. Design Procedure

The detailed design procedure of the proposed new snubber cell is mainly based on the ZVT turn on and ZCT turn off processes of the main transistor. The new snubber cell also provides soft switching for the other semiconductor devices in the converter. But, a detailed analysis is not done for the minimization of the additional losses.

1) The following general comments about the operation of the new converter can be required to understand the design procedure and the features of the converter. It is known that firstly a snubber cell is designed for the lowest input voltage and the highest load current in a converter. Also, the input current I_i decreases when both the input voltage V_i rises and the load current I_o falls. If C_r is ignored, Stages 2 and 9 do not occur, and so t_{23} and t_{910} become zero. In addition to the ignored C_r, if $I_{Ls\,max} = 2I_i$, also Stage 11 does not take place, and so t_{1112} becomes zero and t_{1011} is equal to π/ω_2 The intervals t_{01} and t_{12} are relatively small, and become smaller when I_i falls because they are dependent on I_i. Both t_{34} and t_{89} are selected freely, and so they can be assumed zero. The durations t_{45}, t_{67}, t_{78} and t_{1011} are resonant intervals, and so they are not dependent on I_i or I_o and are always constant. Moreover, $t_{45} = (\pi/2)/\omega_2$, $t_{67} + t_{78} = (\pi/2)/\omega_2$ and $t_{1011} + t_{1112} \cong \pi/\omega_2$ can be written generally. If the durations t_{01} and t_{12} are ignored, the sum of the transient intervals is equal to only one resonant period in the new converter.

2) Snubber inductor L_s can be selected to provide the following conditions with reference to [5], [12] and [14]

$$\frac{V_o}{L_s} t_{r2} \le I_i \quad \text{and} \quad \frac{V_o}{L_s} 3t_{rr} \le I_i. \tag{46}$$

In fact, L_s should be selected as large as possible to decrease both the turn on loss of the auxiliary switch and the reverse recovery loss of the main diode. But, a larger L_s selected results in longer transient intervals and so more limitations in duty cycle. Here, t_{r2} is the rise time of the auxiliary switch, and t_{rr} is the reverse recovery time of the main diode for the values $I_F = I_i$ and $-di_F/dt = -V_o/L_s$.

3) Resonant capacitor C_r is not a turn off snubber capacitor of the main switch, and is not needed in addition to the parasitic capacitors for the operation of the new converter generally. If it is ignored, Stage 9 does not occur, and in Stage 10 the equation (37) is converted to

$$i_{Ls} = (I_{Ls\,max} - I_i)\cos(\omega_2(t - t_9)) + I_i. \tag{47}$$

According to this equation, $I_{Ls\,max}$ must be minimally twice I_i for the reset of the inductor energy in Stage 10. This state can be defined as

$$I_{Ls\,max} \ge 2I_i. \tag{48}$$

For C_r needed for providing this condition, by using (8) and (11)

$$C_r \ge \frac{I_i^2 - I_{rr}^2}{V_o^2} L_s \tag{49}$$

is derived. It is known that I_{rr} is proportional to nearly $\sqrt{I_F(di_F/dt)}$ or $\sqrt{I_i/L_s}$ here. Also, it is about I_i for the values $I_F = I_i$ and $-di_F/dt = -100\ A/\mu s$ in some fast diodes. The parasitic capacitors together with I_{rr} are sufficient to provide the condition (48) generally in practice. In this state, C_r can be considered the sum of the parasitic capacitors.

4) A decrease in the value of the snubber capacitor C_s results in shorter transient intervals, but higher voltages which the auxiliary transistor T_2 is subjected to at the same time. T_2 is subjected to a voltage by $2V_{Cs}$ in Stage 4. For the maximum value of this voltage by using (18), (21), and (48)

$$V_{T2\,max\,4} = 2V_{Cs\,max\,4} = 2I_{Ls\,max}\sqrt{\frac{L_s}{C_s}} = 4I_i\sqrt{\frac{L_s}{C_s}} \tag{50}$$

is derived. Also, T_2 is subjected to a voltage by $V_o + v_{Cs}$ in Stage 10. For the maximum value of this voltage by using (38), (42), and (48) with ignored C_r

$$\begin{aligned} V_{T2\,max\,10} &= V_o + V_{Cs\,max\,10} \\ &= V_o + (I_{Ls\,max} - I_i)\sqrt{\frac{L_s}{C_s}} \\ &= V_o + I_i\sqrt{\frac{L_s}{C_s}} \end{aligned} \tag{51}$$

is achieved. If C_s is selected to be charged to maximally $V_o/2$ in Stage 4, for its value from (50)

$$C_s \ge 16\frac{I_i^2}{V_o^2} L_s \tag{52}$$

is found. In this state, T_2 is subjected to V_o in Stage 4 and $1,25V_o$ in Stage 10.

5) By considering Fig. 3 and the comments given above, the sum of the transient intervals, and the minimum and maximum durations of the turn on signal of the main switch can be respectively defined as

$$T_{TRsum} \cong 2\pi\sqrt{L_s C_s} = t_R \tag{53}$$

$$T_{ON\,min} = \pi\sqrt{L_s C_s} = \frac{t_R}{2} \tag{54}$$

$$T_{ON\,max} \cong T_p - \pi\sqrt{L_s C_s} = T_p - \frac{t_R}{2} \tag{55}$$

where t_R is the resonant period and T_P is the switching cycle.

6) If the sum of the transient intervals is allowed to be equal to at most 20% of the switching cycle as given in [9], for possible maximum switching frequency by using (53)

$$f_{p\,max} = \frac{1}{T_{P\,min}} \cong \frac{1}{5t_R} \tag{56}$$

is derived. In this case, for the minimum and maximum values of the duty ratio in the converter by using (54) and (55)

$$D_{min} = \frac{T_{ON\,min}}{T_{P\,min}} = 0.10 \tag{57}$$

$$D_{max} = \frac{T_{ON\,max}}{T_{P\,min}} \cong 0.90 \tag{58}$$

are achieved. A lower operation frequency selected results in a smaller minimum and a larger maximum duty ratio.

7) With reference to Fig. 3, for the control conditions

$$t_{d1} \cong t_{01} + t_{12} + t_{23} + \frac{t_{ZVT}}{2} \tag{59}$$

$$t_{d2} \cong t_{67} + \frac{t_{ZCT}}{2} \tag{60}$$

$$t_{ZVT} = t_{34} \tag{61}$$

$$t_{ZCT} = t_{78} + t_{89} \geq t_{f1} \tag{62}$$

can be written. In these equations, t_{d1} and t_{d2} are the delay time periods between the turn on signals of the main and auxiliary switches as shown in Fig. 3. t_{f1} is the fall time of the main switch, and only duration t_{78} is sufficient for providing the fall time condition (62) generally.

8) Leakage inductance of the snubber inductor L_s should be as small as possible to turn off the auxiliary transistor T_2 with soft switching, and to snubber additional resonances with high frequencies, and so to decrease additional losses. It can be realized by providing a good magnetic coupling between two half windings of L_s.

After the turn off of T_2 in both the ZVT and ZCT processes, a resonance with high frequency takes place between the leakage inductance of the lower L_S and the parasitic capacitance of T_2 as long as the snubber capacitor C_s is charged softly through the upper L_s. Also, after the charge of C_s in both of the same processes, a different resonance occurs between the lower L_s and the same parasitic capacitance while the voltage of T_2 falls hardly but in smaller amounts than that in normal ZVT converter [1].

These resonances cause small ripples on most voltage and current waveforms, and so little additional losses in the converter. These ripples can be made smaller by connecting a proper fast diode in serial with T_2 in the same direction.

IV. Converter Features

New ZVT-ZCT-PWM converter equipped with the proposed snubber cell combines most the desirable features of both the ZVT and ZCT converters, and overcomes most the drawbacks of these converters mainly. The features of this new converter can be briefly summarized as follows.

1) All semiconductor devices in this converter operate under soft switching conditions. The main switch is both turned on with ZVT and turned off with ZCT perfectly. The ZCS turn on and the ZVS turn off of the auxiliary switch are achieved. Also, the other devices operate with soft switching.
2) The main switch and the main diode are not subjected to any additional voltage and current stresses. Moreover, the stresses on the auxiliary devices are very low.
3) The soft switching operation of the new converter is maintained for the whole line and load ranges. Under light load conditions, in the ZVT process, the main switch voltage falls to zero earlier and then it stays at zero for a longer time because of the decreased intervals t_{01} and t_{12}, and the ZVT turn on of the main switch is still realized successfully at last.

   In the ZCT process, a decrease in the input current I_i is not effective on the ZCT turn off of the main switch. Because the maximum inductor current $I_{Ls\,max}$ and the maximum capacitor voltage $V_{Cs\,max}$ as well vary in proportion to nearly I_i, and also the intervals t_{67} and t_{78} concerning the ZCT process are always constant.

   Moreover, the new converter continues also to operate under soft switching conditions in the discontinuous current mode formed at very low load currents. Because the parasitic capacitors provide still an enough maximum inductor current for the soft switching at these low currents.
4) The converter can operate at considerably high frequencies, and acts as a normal PWM converter over most of the time, and also the circulating energy is quite small. Because the sum of the transient intervals is equal to only one resonant period, and so is a little fraction of the switching cycle. By comparison with this converter, a similar converter newly presented in [9] has two resonant periods.
5) The converter has ease of control. The delay time periods t_{d1} and t_{d2} are determined only by calculating, and they are selected flexibly because each of them includes an interval that can be selected freely. It is not required to change the delay periods when the input current even decreases, because the control conditions are still provided successfully. Also, the main and auxiliary switches have a common ground. All these features make control easy.
6) The new converter is nearly as simple and cheap as most of the ZVT and ZCT converters presented previously. Because only one quasi resonant circuit is used and there is not an important increase in the number of additional elements while both the ZVT turn on and ZCT turn off of the main switch are achieved in this converter.
7) The proposed new snubber cell can be easily applied to the other basic PWM converters.

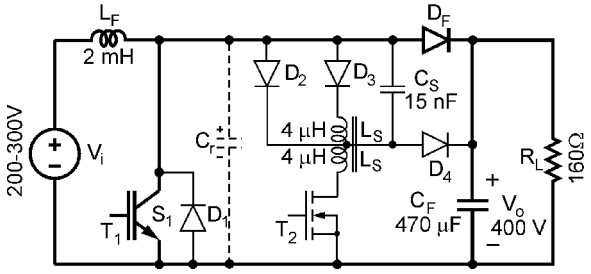

Fig. 4. Experimental circuit of a 1-kW and 100-kHz boost converter.

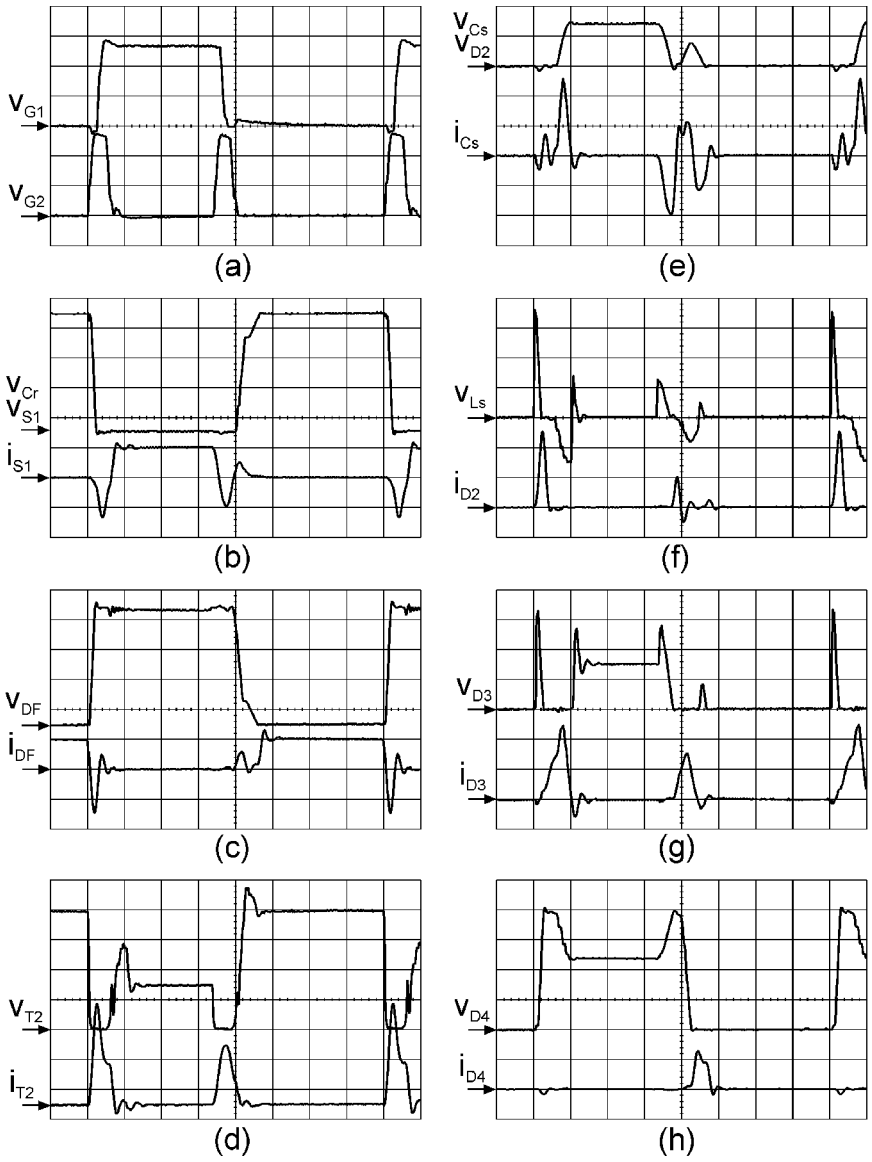

Fig. 5. Some oscillograms with the scales of 5 V/div and 1 μs/div for only (a), and 100 V/div, 4 A/div and 1 μs/div for the others. (a) Turn on signals of T_1 and T_2. (b) Voltage and current of S_1. (c) Voltage and current of D_F. (d) Voltage and current of T_2. (e) Voltage and current of C_s. (f) Voltage of L_s and current of D_2. (g) Voltage and current of D_3. (h) Voltage and current of D_4.

8) The converter does not require any additional passive snubber cells.
9) The existence of the leakage inductance with very small value is considered as a drawback of this new converter.

V. Experimental Results

A prototype of a 1-kW and 100-kHz boost converter shown in Fig. 4 was performed to verify the predicted analysis of the proposed ZVT–ZCT–PWM converter. The oscillograms given below were obtained from the operating circuit by a digital oscilloscope. The other experimental results were determined by measuring the voltage and current values of the input and output of the circuit, and by measuring the temperature rise rates of the heatsinks of the semiconductor devices. Moreover, the results in the hard switching case were estimated from the measurements obtained from the circuit operating at low frequencies.

With reference to the handbooks of the manufacturers, some nominal values of the IGBT as a main switch are $V = 600$ V, $I = 20$ A, $t_r = 35$ ns, and $t_f = 120$ ns. The values of the MOSFET as an auxiliary switch are $V = 500$ V, $I = 11,6$ A, $t_r = 21$ ns, and $t_f = 21$ ns The main diode owns $V = 600$ V, $I = 12$ A, and $t_{rr} = 100$ ns. Additionally, the other diodes own $V = 600$ V, $I = 8$ A, and $t_{rr} = 60$ ns values.

The turn on signals of T_1 and T_2 (a), the voltage and the current of the main switch S_1 containing T_1 and D_1 (b), the voltage and the current of the main diode D_F (c), the voltage and the current of the auxiliary transistor T_2 (d), the voltage and the current of C_s (e), the voltage of L_s and the current of D_2 (f), the voltage and the current of D_3 (g), and the voltage and the current of D_4 (h), are shown in the oscillograms given in Fig. 5, respectively.

In connection with Fig. 5(a), it is seen that both of the delay time periods t_{d1} and t_{d2} are about 350 ns and each of the turn

on time intervals of T_2 is nearly 600 ns. From Fig. 5(b), it can be mainly seen that T_1 operates at entirely soft switching conditions, no overlap between its voltage and current occurs, and so it has the only conduction loss. Its antiparallel diode D_1 stays in on state for a very short time before its turn on and off, and so its ZVT turn on and ZCT turn off processes are perfectly realized. Fig. 5(c) basically illustrates that D_F is turned on under ZVS and turned off under nearly ZCS and ZVS, and so its switching loss is very low. Both the main devices S_1 and the main diode D_F do not have any additional voltage and current stresses.

In Fig. 5(d), it is clearly seen that T_2 is switched in both ZVT and ZCT processes over one switching cycle. It is turned on under nearly ZCS, then conducts a current pulse with a short time, and at last turned off under nearly ZVS in both processes. Its current pulse in the ZCT process is smaller than that in the ZVT process due to the losses of the resonant circuits. Also, a small voltage spike is seen on it just after its every turn off because of the leakage inductance of the lower L_s and so these spikes cause a little switching loss in it. In the ZVT and ZCT processes, T_2 is subjected to a voltage pulse of almost twice the maximum voltage of C_s and to a pulse little larger than the output voltage V_o after its turn off, respectively.

From Fig. 5(e), it can be seen that C_s is maximally charged to a value of approximately $1/3V_o$ and to nearly $1/8V_o$ after the turn off of T_2 in the ZVT and ZCT processes, respectively. The voltages of C_s are effective on the voltage pulses, which T_2 is subjected to after its turn off. Complementary features are illustrated in Fig. 5(f)–(h). The current of the upper L_s is the same as the current of D_3, and the lower L_s current is the same as that of T_2. L_s takes on an amount energy as T_2 is turned on, and it commutates this energy to C_s through D_3 after the turn off of T_2. D_4 conducts a current only while the snubber energy is transferred to the load. Also, the diodes D_1, D_2, D_3, and D_4 operate under soft switching.

Generally, the reverse recovery currents and the parasitic capacitor charge currents of all diodes are shown on their current waveforms after their turn on and off processes. Small spikes and little collapses are seen on most of the voltage and current waveforms because of the turn on delay of the diodes at switching instants. Also, a resonance with high frequency takes place between the leakage inductance of the lower L_s and the parasitic capacitance of T_2 after every turn off of T_2. This resonance results in small ripples on most of voltage and current waveforms.

With reference to the theoretical analysis, the maximum inductor current $I_{Ls\,max}$ continues to flow by the closed circuit the lower $L_s - T_2 - D_1 - D_2$ over the free intervals t_{34} and t_{89}. In practice, the inductor produces a voltage by the total voltage drop of this circuit to keep flowing this current, and the voltages of two half windings are equal to each other because of their magnetic coupling. Therefore, the current $I_{Ls\,max}$ tends to be divided among two half windings, and so D_2 is turned off suddenly, and the lower L_s current falls and the upper L_s current rises simultaneously. This state is clearly seen on the practical waveform concerning it, and it has a good effect on the turn off of T_2 and so on the parasitic ripples.

Moreover, it is observed that the new converter operates in the discontinuous current mode as long as the load current is smaller that nearly 100 mA, and it can operate at a load current by about 5 mA with the minimum duty ratio. It is also observed that the new converter keeps operating under soft switching conditions successfully for the whole line and load ranges.

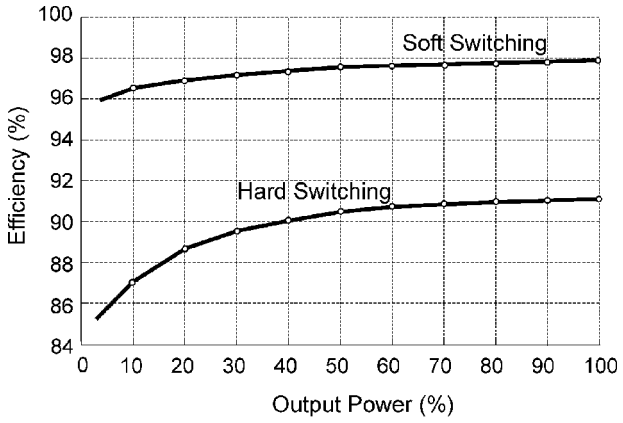

Fig. 6. Efficiency curves of the proposed SS and the HS converters compared.

From Fig. 6, it is seen that the overall efficiency of the new converter reaches a value of 98% at full output power of 1 kW and a switching frequency of 100 kHz. Also, this efficiency is almost equal to that in the similar converter presented in [9] although the similar circuit operates at 1 kW and 40 kHz nominally. It is also seen that the efficiencies at low output powers are relatively higher than most of the other SS converters. Because converter loss is dependent strongly on circulating energy generally, and it is very low and also it becomes lower as the load current falls in the new converter.

In finally, it was observed that all the experimental results exactly verified the theoretical analysis of the proposed new ZVT–ZCT–PWM converter.

VI. Conclusion

In this study, a new active snubber cell that provides ZVT turn on and ZCT turn off together for the main switch of a converter is presented to contrive a new family of the PWM converters. This new snubber cell is implemented by using only one quasi resonant circuit without an important increase in cost and complexity. Novel ZVT–ZCT–PWM converter equipped with the proposed snubber cell combines most of the desirable features of both ZVT and ZCT converters presented previously, and overcomes most of the drawbacks of these converters mainly.

Subsequently, all semiconductor devices operate under soft switching, the main devices are subjected to no additional voltage and current stresses, and the stresses on the auxiliary devices are very low in the proposed new converter. This new converter operates successfully under light load conditions for the whole line and load ranges and at very high frequencies. Also, it has a simple structure, low cost and ease of control.

Consequently, novel ZVT–ZCT–PWM boost converter equipped with the proposed new snubber cell was analyzed in detail. It was observed that the operation principles and the theoretical analysis of this converter were exactly verified by a prototype of a 1 kW and 100 kHz. Also, the overall efficiency of the converter reached a value of nearly 98% at full output power.

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