A Noise Optimization Technique for Integrated Low-Noise Amplifiers

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***Abstract*—Based on measured four-noise parameters and two-port noise theory, considerations for noise optimization of integrated low-noise amplifier (LNA) designs are presented. If arbitrary values of source impedance are allowed, optimal noise performance of the LNA is obtained by adjusting the source degeneration inductance. Even for a fixed source impedance, the integrated LNA can achieve near $NF_{\min}$ by choosing an appropriate device geometry along with an optimal bias condition. An 800-MHz LNA has been implemented in a standard 0.24-μm CMOS technology. The amplifier possesses a 0.9-dB noise figure with a 7.1-dBm third-order input intercept point, while drawing 7.5 mW from a 2.0-V power supply, demonstrating that the proposed methodology can accurately predict noise performance of integrated LNA designs.**

***Index Terms*—Amplifier noise, induced gate noise, low-noise amplifier, microwave amplifier, MOSFET amplifier, noise figure, random noise, semiconductor device noise.**

I. Introduction

THE FIRST stage of a receiver is typically a low-noise amplifier (LNA). The LNA design involves tradeoffs between many figures of merit, such as gain, noise, power, impedance matching, stability, and linearity. Since the primary role of the LNA is to lower the overall noise figure of the entire receiver, noise optimization is one of the most critical steps in the LNA design procedure. In traditional monolithic microwave integrated circuit (MMIC) design, active devices are given with fixed geometries and characteristics. For the given bias and frequency conditions, a source impedance Z_s is selected to minimize the noise figure [1]. Since the optimum source impedance for noise ($Z_{\rm opt}$) differs from the power-match condition in general, this technique often results in large power consumption or input mismatching. Even in full custom ICs, despite an important option that the designer can choose the desired device geometries, most designers still rely on the same optimization techniques [2]–[4] because no explicit guidance is generally available on how to best exercise the IC designer's freedom in tailoring device geometries. They can achieve an optimum noise figure with acceptable input mismatching (typically $s_{11} \approx -10$ dB) but do not fully exploit the potential of integrated LNAs. Recently proposed noise optimization techniques for CMOS RF circuits permit greater flexibility in the selection of device geometries as well as matching elements and biasing conditions to minimize the noise figure for a specified gain or power dissipation [5], [6]. However, they use simplified small-signal models as well as constant noise characteristics. These techniques also rely heavily on mathematical derivations that provide limited intuitive design guidance.

This paper presents considerations for noise optimization of LNAs based directly on measured noise parameters and two-port noise theory; the approach requires neither sophisticated noise modeling nor circuit simulation to be used. All the analyses are based on MOSFET designs, but the same methodology can be applied to other IC technologies, such as BiCMOS or heterojunction bipolar transistors (HBT). Section II reviews the basic concept of the noise figure and four-noise parameters. It also discusses the intrinsic noise model of the MOSFET and its relation to the measured noise performance of amplifiers. Section III explains how the noise performance of the LNA differs from that of the intrinsic device; design considerations for a CMOS-tuned LNA with power constraints are presented. Section IV presents experimental results for an implementation using integrated CMOS technology to realize an LNA.

II. Fundamental Noise Theory for CMOS Circuits

A. Concept of the Four-Noise Parameters

The noise performance of a circuit is usually characterized by a parameter called *noise factor* (F) or *noise figure* ($NF \triangleq 10\log F$) that represents how much the given system degrades the signal-to-noise ratio [1].

$$F \triangleq \frac{\left(\frac{S}{N}\right)_{\rm in}}{\left(\frac{S}{N}\right)_{\rm out}} \tag{1}$$

$$= \frac{\text{Total Output Noise Power}}{\text{Output Noise Power by Source Impedance}}. \tag{2}$$

At one frequency, the noise factor of a linear circuit shows a parabolic dependence on the source impedance driving the given circuit. This behavior results in constant noise circles on the Smith chart and can be characterized in terms of the four-noise parameters [7] as follows:

$$F = F_{\min} + \frac{\left[(G_s - G_{\rm opt})^2 + (B_s - B_{\rm opt})^2\right] R_n}{G_s} \tag{3}$$

Manuscript received January 23, 2001; revised April 15, 2002. This work was initiated by the Defense Advanced Research Projects Agency under Contract Army-DABT63-94-C-0055 and supported by Texas Instruments Incorporated through customized research under SRC Contract 99-NJ-695.

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Publisher Item Identifier 10.1109/JSSC.2002.800956.

where $F_{\min}$ is the minimum noise factor, G_s and B_s are real and imaginary parts, respectively, of the source admittance ($Y_s = 1/Z_s$); $G_{\rm opt}$ and $B_{\rm opt}$ are real and imaginary parts, respectively, of the optimum source admittance ($Y_{\rm opt} = 1/Z_{\rm opt}$, also known as the noise-matching condition), and R_n is the equivalent noise resistance. When Y_s is adjusted to $Y_{\rm opt}$, the circuit yields the best achievable noise performance $F_{\min}$. If Y_s differs from $Y_{\rm opt}$, its impact on F is amplified by R_n. Even if $F_{\min}$ is sufficiently low, large R_n and a poor proximity between Y_s and $Y_{\rm opt}$ result in an unacceptably large noise figure in the actual circuit. This problem becomes acute for MOSFET circuits because the reflection coefficient[1] for optimum noise ($|\Gamma_{\rm opt}|$) is nearly 1 and R_n is 3–10 times larger than for high electron mobility transistor (HEMT) devices [8].

B. High-Frequency Noise in MOSFETs

The thermal fluctuations of channel charge in the MOSFET produce effects that are modeled by drain and gate current noise generators [9]. These currents are partially correlated with each other because they share a common origin and possess a spectral power given by

$$\overline{i_d^2} \triangleq 4kT\Delta f \gamma g_{d0} \tag{4}$$

$$\overline{i_g^2} \triangleq 4kT\Delta f \delta g_g \tag{5}$$

$$\overline{i_g i_d^*} \triangleq c\sqrt{\overline{i_g^2}\,\overline{i_d^2}} \tag{6}$$

where g_{d0} is the drain output conductance under zero drain bias, $g_g \triangleq \zeta(\omega^2 C_{gs}^2)/(g_{d0})$ is the real part of gate-to-source admittance, and γ, δ, and c are bias-dependent factors. For long-channel MOSFETs, γ, δ, and c are, respectively, 2/3, 4/3, and $j0.395$ in the saturation region, but short-channel MOSFETs exhibit larger values [5], [10]. These expressions imply that the spectral power density scales with the device width W.

C. Scaling of the Noise Parameters

In realizing a custom IC design of the LNA, one of the key issues is to understand the device scaling effects on the noise parameters. The four-noise parameters can be derived[2] from current noise spectral power, given in (4)–(6), as follows:

$$F_{\min} \approx 1 + \frac{\omega}{\omega_T}\sqrt{\gamma\delta\zeta\,(1-|c|^2)} \tag{7}$$

$$R_n \approx \frac{\gamma g_{d0}}{g_m^2} \tag{8}$$

$$G_{\rm opt} \approx \frac{g_m \omega C_{gs}}{g_{d0}}\sqrt{\frac{\delta\zeta\,(1-|c|^2)}{\gamma}} \tag{9}$$

$$B_{\rm opt} \approx -\omega C_{gs}\left(1 - c\frac{g_m}{g_{d0}}\sqrt{\frac{\delta\zeta}{\gamma}}\right). \tag{10}$$

Equation (7) suggests that devices with shorter channel length yield better noise figures because the angular cutoff frequency ω_T is proportional to $1/L_{\rm eff}$ while $\sqrt{\gamma\delta\zeta(1-|c|^2)}$ becomes at most 6.5 times larger than the long-channel case, down to 0.25 μm [6]. Likewise, (8) also suggests that shorter devices improve R_n. Therefore, the selection of device geometries for the LNA design requires width scaling of the device, consistent with the shortest channel length that can be realized. In (7)–(10), g_{d0}, g_m, and C_{gs} scale linearly with the device width W, while noise factors γ, δ, ζ, and c are width independent. These results thus suggest the dependence of the four-noise parameters with respect to the device width as follows:

$$F_{\min} \quad \text{no width dependence} \tag{11}$$

$$R_n \propto 1/W \tag{12}$$

$$G_{\rm opt} \propto W \tag{13}$$

$$B_{\rm opt} \propto W. \tag{14}$$

Equations (3) and (12) imply that the larger device width offers the best chance of lowering noise figure. The upper limit of the width is set by the constrained power budget in integrated circuit implementations. When the supply voltage and power consumption are given, the device width of the input stage corresponding to each bias condition can be easily calculated from the current density. In other words, for a fixed drain current, lower gate biasing allows a larger device width and higher gate biasing demands to decrease the device width.

D. Noise Analysis of the Amplifier

This paper utilizes the two-port theory [11], [12] instead of analytical equations. The four-noise parameters and S-parameters were measured from a 0.24-μm nMOSFET with $W = 100$ μm, using the ATN NP5B system. The frequency range was from 0.5 to 6.0 GHz with 0.5-GHz step and the gate and drain bias conditions were from 0.5 to 2.5 V with 0.2-V step, respectively. The resulting data were then smoothed for the frequency as well as the bias dependences and used in the following analyses. The tuned amplifier illustrated in Fig. 1(a) is one of the most broadly used LNA architectures because it offers the potential of achieving the best noise performance [5], [6], [10]. To evaluate its noise performance, the amplifier is divided into three cascading stages as illustrated in Fig. 1(b).

An admittance noise matrix for the first stage ($\boldsymbol{C}_{Y,1\rm st}$) is found from the following network parameters:

$$\boldsymbol{Y}_{1\rm st} = \begin{bmatrix} \dfrac{1}{sL_g} & \dfrac{-1}{sL_g} \\ \dfrac{-1}{sL_g} & sC_p + \dfrac{1}{sL_g} \end{bmatrix}. \tag{15}$$

This noise matrix is then transformed to the $ABCD$ representation ($\boldsymbol{C}_{A,1\rm st}$).

In the second stage, an $ABCD$ noise matrix of $M_1(\boldsymbol{C}_{A,M_1})$ is obtained from the measured four-noise parameters and then transformed to the impedance noise matrix ($\boldsymbol{C}_{Z,M_1}$). The total noise of the second stage ($\boldsymbol{C}_{Z,2\rm nd}$) is the sum of $\boldsymbol{C}_{Z,M_1}$ and the one for the source inductor component ($\boldsymbol{C}_{Z,L_s}$). As done for the first stage, an $ABCD$ representation ($\boldsymbol{C}_{A,2\rm nd}$) is obtained by a transformation.

Finally, the noise matrix of the third stage ($\boldsymbol{C}_{A,3\rm rd}$) is acquired from the four-noise parameters of the

[1]Defined as $\Gamma_s = (Y_0 - Y_s)/(Y_0 + Y_s)$, where Y_0 is the characteristic admittance of the transmission line.

[2]Exact expressions can be derived based on the two-port theory [11], [12]. The approximated (7)–(10) neglect the distributed and Miller effects. Their derivations are found in [10].

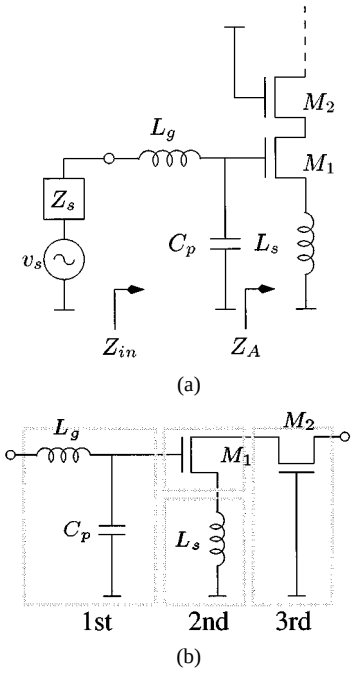


Fig. 1. (a) Tuned LNA architecture employing inductive source degeneration. (b) Noise performance evaluation sequence for an amplifier.

common-gate-mode MOSFET. Alternatively, it can be acquired through a conversion process presented in [13]. Note that the noise contribution from $Y_{\rm sub}$ needs to be subtracted from the second stage and added to the third stage.

The noise performance of the entire amplifier is given by cascading the three stages, as follows:

$$\boldsymbol{C}_{A,\rm Total} = \boldsymbol{A}_{\rm 1st}\boldsymbol{C}_{A,\rm 2nd+3rd}\boldsymbol{A}_{\rm 1st}^{\dagger} + \boldsymbol{C}_{A,\rm 1st} \tag{16}$$

$$\boldsymbol{C}_{A,\rm 2nd+3rd} = \boldsymbol{A}_{\rm 2nd}\boldsymbol{C}_{A,\rm 3rd}\boldsymbol{A}_{\rm 2nd}^{\dagger} + \boldsymbol{C}_{A,\rm 2nd}. \tag{17}$$

III. Design Considerations for a Tuned Amplifier

For the topology illustrated in Fig. 1(a), the desired input impedance of the amplifier is obtained for a narrow frequency band by choosing L_s and L_g independently. When $C_p = 0$, it is approximated as follows [5]:

$$Z_{\rm in} \approx s(L_g + L_s) + \frac{1}{sC_{gs}} + \omega_T L_s. \tag{18}$$

It is known that the source degeneration inductance L_s controls the noise performance of the given architecture [14], but the reasons are not well understood.

Suppose a power supply having a conjugately matched source impedance Z_s is connected to the LNA as illustrated in Fig. 1(a). This can mean that $L_g = C_p = 0$ and $Z_s = Z_{\rm in}^* = Z_A^*$, or that L_g and C_p transform a given Z_s to be conjugately matched to Z_A. Assuming the noise from passive components is negligible, based on the definition in (2), the noise factor of the given topology can be expressed as [6]

$$F = 1 + \frac{S_{M_1} + S_{M_2}}{S_{R_s}} \tag{19}$$

$$S_{R_s} = 4kT\Re[Z_s]\,|G_{m_1}|^2\,|A_{i_2}|^2 \tag{20}$$

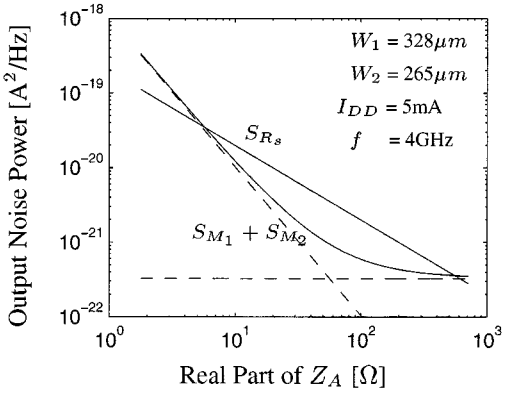


Fig. 2. Dependence of output noise power components on $\Re[Z_A]$ where Z_A is the input impedance at the gate electrode of M_1. A conjugate power match is assumed.

$$S_{M_1} = \frac{4kT\gamma_1 g_{d0_1}\chi\,|A_{i_2}|^2}{4} \tag{21}$$

$$S_{M_2} = 4kT\gamma_2 g_{d0_2}\xi \tag{22}$$

$$|G_{m_1}| = \frac{\omega_T}{2\omega_0\sqrt{\omega_T L_s \Re[Z_s]}} \tag{23}$$

$$A_{i_2} = \frac{g_{m_2}}{g_{m_2} + j\omega_0 C_{gs_2}} \tag{24}$$

$$\chi \triangleq 1 - 2\omega_0 L_s g_m |c|\kappa + \left(1 + \omega_0^2 L_s^2 g_{m_2}^2\right)\kappa^2 \tag{25}$$

$$\kappa \triangleq \frac{1}{\omega_0^2 C_{gs_1} L_s}\sqrt{\frac{\delta_1 g_{g_1}}{\gamma_1 g_{d0_1}}} \tag{26}$$

$$\xi \triangleq \eta\left(g_{ds_1}^2 + \omega_0^2 C_{\rm tot}^2\right) + \eta^2\rho\tau + \eta\tau^2 \tag{27}$$

$$\eta \triangleq \frac{1}{(g_{ds_1} + g_{m_2})^2 + \omega_0^2 C_{\rm tot}^2} \tag{28}$$

$$\rho \triangleq 2\omega_0 C_{\rm tot} g_{m_2}|c|\left[(g_{ds_1} + g_{m_2})^2 + \omega_0^2 C_{\rm tot}^2\right] \tag{29}$$

$$\tau \triangleq g_{m_2}\sqrt{\frac{\delta_2 g_{g_2}}{\gamma_2 g_{d0_2}}} \tag{30}$$

$$C_{\rm tot} \triangleq C_{db_1} + C_{sb_2} + C_{gs_2} \tag{31}$$

where $\Re[\,]$ denotes the real part of a complex number, and S_{R_s}, S_{M_1}, and S_{M_2} are current noise power components at the output of the LNA contributed by Z_s, M_1, and M_2, respectively. In Fig. 2, the device size and bias condition are fixed, then the impact of different $\Re[Z_A] \approx \omega_T L_s$ are examined. The result shows that each component has a different dependence on $\Re[Z_A]$. Since the feedback of L_s reduces the current gain, as L_s increases, the output noise contributions from the source resistance S_{R_s} and the induced gate noise of $M_1(S_{i_g,M_1})$ monotonically decrease, but their slopes are different due to different feedback gains. On the other hand, the contribution from the induced gate noise of $M_2(S_{i_g,M_2})$ is negligibly small. The contributions from drain current noise (S_{i_d,M_1} and S_{i_d,M_2}) have almost unity gain, and thus result in an L_s-independent term. Hence, the LNA yields the best noise figure when the L_s-dependent term (S_{i_g,M_1}) and L_s-independent term ($S_{i_d,M_1} + S_{i_d,M_2}$) give equal contributions, as illustrated in Fig. 2 by two dashed lines.

The four-noise parameters offer a more intuitive means of explanation for the phenomenon discussed above. The four-noise

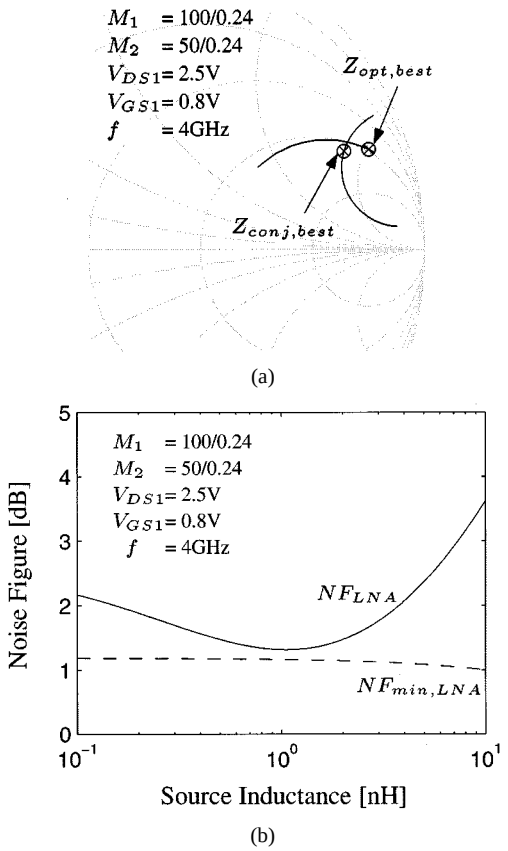


Fig. 3. Noise performance of the LNA for varying L_s. The noise contributions of M_1 substrate and M_2 are excluded and $C_p = 0$. (a) Optimum source impedance. (b) Noise figure.

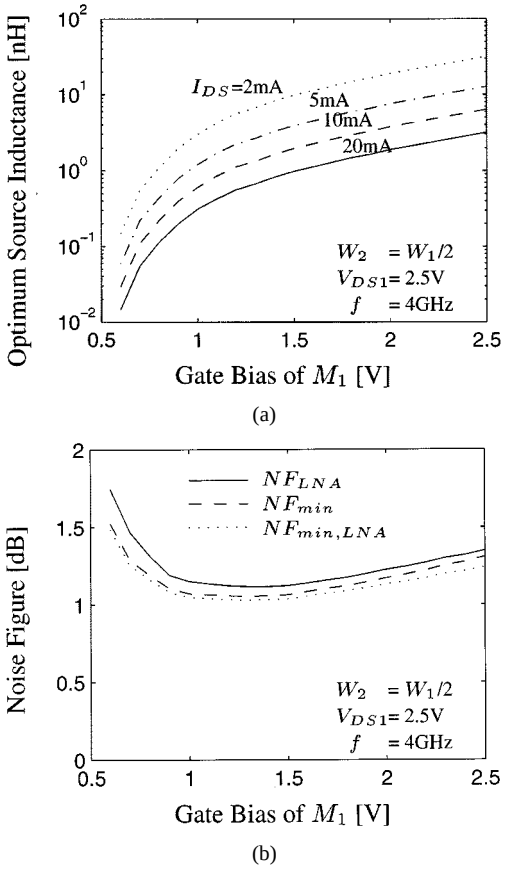


Fig. 4. (a) Optimum L_s yielding the best noise figure of the LNA for the given bias condition under the power constraint. (b) Best noise figure of the LNA with optimum L_s. The noise contributions of M_1 substrate and M_2 are excluded and $C_p = 0$.

parameters of the LNA are calculated for different values of L_s using $\boldsymbol{C}_{A,\text{2nd+3rd}}$ in Section II-D. Fig. 3(a) plots the power-matching condition ($Z_{\text{conj}} = Z_{\text{in}}^*$) and noise-matching condition ($Z_{\text{opt}} = Y_{\text{opt}}^{-1}$) together on the Smith chart for varying L_s from 0.1 to 10 nH. As L_s increases, the real part of Z_{in} proportionally increases and the power-matching condition moves downward counterclockwise. On the other hand, L_s dramatically changes the noise-matching condition as well, but it exhibits a totally independent trajectory to the left. An interesting fact is that those two conditions can come into a good proximity by an appropriate amount of the source degeneration. Since the proximity means $|Y_s - Y_{\text{opt}}|^2$ in noise performance calculation, a better proximity essentially leads to a lower noise figure.

Fig. 3(b) shows the noise figure when the source impedance (Z_s) is chosen to Z_{in}^* providing a perfect power match. The best achievable noise figure is obtained when L_s brings Z_{opt} and Z_{conj} to the point where they are in the closest proximity; those conditions are marked as $Z_{\text{opt,best}}$ and $Z_{\text{conj,best}}$ in Fig. 3(a). This fact implies that an accurate calculation of the input impedance is critical in the noise optimization process; approximate values are of limited use. Another beneficial impact of using a source inductance is that it substantially lowers R_n and slightly improves $F_{\min}$ as well. Thus, the LNA can potentially achieve a better noise figure than $NF_{\min}$ of the MOSFET alone if Z_{opt} coincides with Z_{conj}.

Since Z_{opt} is a function of the device size and bias condition, so is the optimum L_s. Fig. 4(a) demonstrates the optimum L_s is bias dependent and scales linearly with the specified current. However, the noise figure achieved by optimizing L_s is independent of the current specification and very close to the intrinsic $NF_{\min}$, as shown in Fig. 4(b).

A. Input Transistor Optimization

To achieve $Z_s \approx Z_{\text{opt}}$ for noise minimization, the designer has two options. The first approach is to adjust the source impedance to a predetermined Z_{opt}, which is set by a given MOSFET. The other approach is to adjust Z_{opt} to a prefixed Z_s by changing the geometries of the transistors, primarily the input device. The second option is very useful since the source impedance has a fixed value of 50 Ω in many RF applications; also, the linearity specification often limits the choice of L_s, which sets the real part of the input impedance. Thus, selection of the input device is the primary consideration in noise optimization of integrated circuits.

This section assumes that the source impedance is fixed to 50 Ω and seeks the optimum size of the input transistor. For different gate bias ranging from 0.6 to 1.5 V, the width of the input device M_1 with the shortest channel length is first adjusted to satisfy the given power constraint at each gate bias. To make the LNA be in a power-match condition, the inductor L_s is chosen to provide a 50-Ω real part of the input impedance for the LNA and then the value of L_g is adjusted to cancel of the imaginary part of the input impedance. For better accuracy, the input impedance

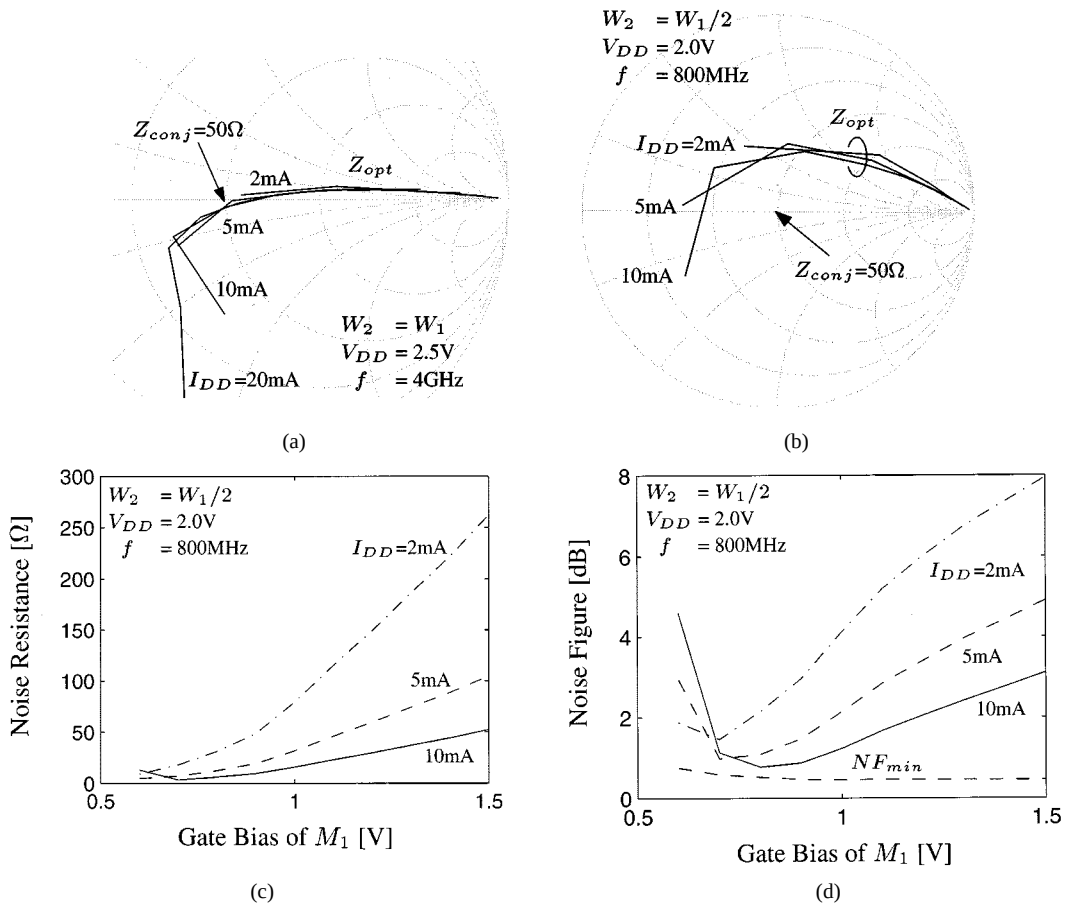


Fig. 5. Power-constrained noise performance of the LNA when $R_s = Z_{\rm in} = 50\ \Omega$. The noise contributions of M_1 substrate and M_2 are included and $C_p = 0$. (a) Optimum source impedance at $f = 4$ GHz. (b) Optimum source impedance at $f = 800$ MHz. (c) Equivalent noise resistance. (d) Noise figure.

is calculated based on the methodology in [13]. In that case, while the power-match condition $Z_{\rm conj}$ is fixed to 50 Ω, the noise-match condition $Z_{\rm opt}$ moves as shown in Fig. 5(a) and (b). As discussed in the previous section, the proximity of $Z_{\rm opt}$ to 50 Ω determines the noise figure. Even if $Z_{\rm opt}$ somewhat deviates from 50 Ω, however, this deviation does not substantially degrade the noise figure since the noise resistance of the LNA is reduced by a factor of as much as 5 in comparison to the MOSFET by itself, as shown in Fig. 5(c). In general, the current specification directly scales the allowable device width and lowering gate bias grants to use a larger device width for a fixed drain current. As the noise resistance is inversely scaled with the device width, it is evident that higher drain current specification and lower gate biasing make the noise figure less sensitive to a noise mismatch.

Fig. 5(d) clearly shows the optimum gate bias for noise. It also demonstrates that resulting noise figures are close to $NF_{\rm min}$. The valley-shaped noise figure profile can be described by an analytical expression as follows [6]:

$$F \approx 1 + \frac{\gamma g_{d0}}{G_s}\left(\frac{\omega_0}{\omega_T}\right)^2 + G_s\frac{\delta\zeta}{g_{d0}}. \tag{32}$$

The second and third terms include the drain conductance g_{d0}. Since it is linearly scaled with the width, it becomes smaller as the gate bias increases for a fixed current specification. In the second term, γ suggests that this term originates from the drain noise; g_{d0} in the numerator implies that this term is dominant when the gate bias is low due to width scaling. On the other hand, in the third term, δ suggests that this term originates from the induced gate noise; g_{d0} in the denominator proposes that this term is dominant when the gate bias is high. In other words, the given formula has two independent noise components that have the opposite gate bias dependence to each other. The noise figure thus has minima where they contribute equally to the noise figure. This fact highlights the importance of accurate gate noise modeling for circuit design.

B. Cascode Stage Design

The cascode stage has a relatively small impact on the overall noise figure if the input stage is not optimal. However, to squeeze out the best noise figure, it needs to be optimized as well. In fact, in Fig. 5(d), the difference between the minima of the noise figure valley and $NF_{\rm min}$ is primarily limited by the extra noise contribution from the cascode stage which is also subject to the given power constraint. Thus, the second step of the noise optimization is choosing a proper size for the cascode stage. For the topology shown in Fig. 5(b), $Z_{\rm opt}$ exhibits a larger deviation from the power-match condition. It is caused not by the operating frequency, but by the poorly optimized cascode stage. While it is known that increasing the width of the cascode device monotonically improves shielding from the output, its impact on the noise performance is not well understood.

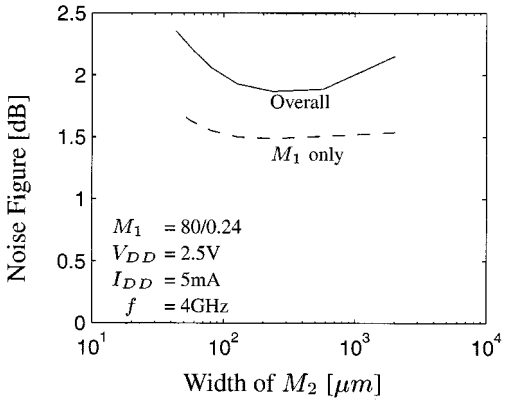


Fig. 6. Impact of the cascode transistor on the overall noise figure under the power constraint. $R_s = Z_{\text{in}} = 50\ \Omega$.

The bias of the cascode stage is tightly linked to its size. The width can increase until the bias of the cascode stage approaches the threshold voltage, or it can decrease until the input device reaches the linear region. In this section, the gate bias and size of the input device is fixed to the optimum values found in Fig. 5(d) and the width of the cascode stage device is swept with the minimum channel length. The inductors L_s and L_g are readjusted to keep the input impedance to 50 Ω. As the width of the cascode stage (W_2) increases, the generated noise power from the cascode stage also increases. Intuitively, this fact suggests that smaller W_2 improves the noise figure monotonically by reducing the noise contribution of M_2 as well as the capacitance at the intermediate node between M_1 and M_2. Due to the Miller effect, however, the required L_s for $\Re[Z_{\text{in}}] = 50\,\Omega$ increases as W_2 becomes smaller. Consequently, smaller W_2 yields a different noise-match condition as well as larger value of R_n. Eventually, the noise figure becomes worse if W_2 is too small. An optimal width exists as shown in Fig. 6. For the given topology, with $W_2 \approx 3W_1$, the cascode stage introduces 40% extra noise power to the input stage, which, in turn, increases NF by about 0.5 dB.

C. Pad Capacitance

In the process of practical LNA design, as illustrated in Fig. 1(a), the bonding pad introduces an extra ac current path to ground. In silicon technology, this can severely deteriorate the noise figure if the path contains a resistive component, such as the conductive substrate [15]. However, if the resistive component is suppressed by replacing the bottom plate of the pad capacitor from the substrate to a metal layer [15], the bonding capacitance simply increases the required inductance value for the designated input impedance. This consequently brings the noise-match condition closer to Z_{conj} and also diminishes the noise resistance further. In this section, the input device optimization process presented in Section III-A is performed again with the presence of the pad capacitance. An arbitrary value[3] of C_p is chosen first and then L_s and L_g are adjusted to make $Z_{\text{in}} = 50\ \Omega$. Fig. 7(a) and (b) demonstrates that the bonding pad capacitance mitigates the strong gate bias dependence of the noise figure. However, it is a tradeoff between the noise figure and gain.

[3]This is a part of the design rules in many cases.

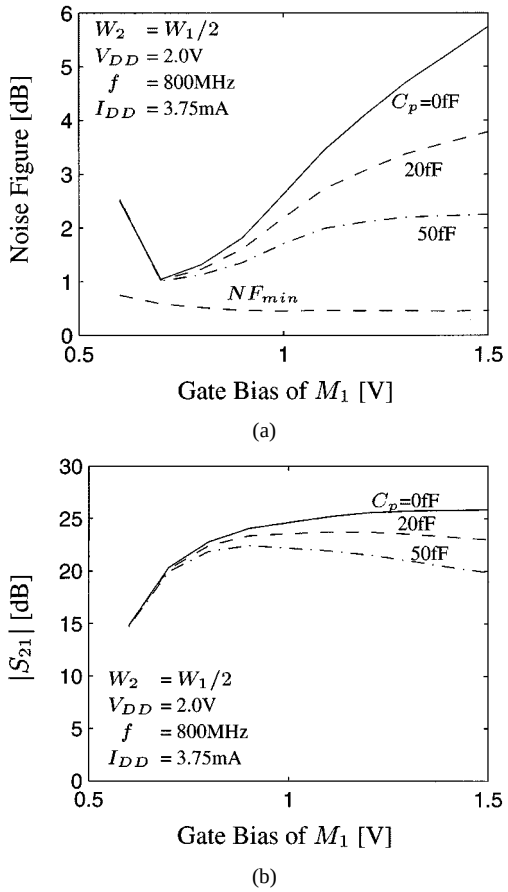


Fig. 7. Power-constrained noise performance of the LNA when $R_s = Z_{\text{in}} = 50\,\Omega$ for different pad capacitance. The noise contributions of M_1 substrate and M_2 are included. (a) Noise figure. (b) Gain.

IV. Experimental Results

To evaluate the LNA performance, a single-ended LNA intended to achieve 1.0 dB of noise figure was designed using a 0.24-μm silicide CMOS technology. The die photo of the LNA is given in Fig. 8. First, the minimum size pad was implemented using metal-5 and metal-1 layers to suppress extra noise, giving 47 fF of capacitance. The supply voltage was chosen to be 2.0 V to provide a voltage headroom for the cascode transistor.[4] The analysis in Fig. 5(d) suggests that at least 3.75 mA of bias current is required to achieve below 1.0 dB of noise figure. The gate bias was set to 0.7 V to achieve the best noise figure based on the characteristic in Fig. 7(a). The corresponding size of M_1 was 90/0.24 for the given power budget. At the time of design, the cascode stage was not fully optimized and the size of M_2 was chosen to be 45/0.24. For the given topology, it is expected to improve the noise figure by 0.1 dB with $W_2 = 80\ \mu$m. To minimize the distributed gate resistance, the MOSFETs were segmented into 5-μm-long gate fingers and each of the fingers was contacted at both ends [16]. The spiral inductor L_s was implemented using the metal-5 layer and its value was chosen to

[4]The threshold voltage is relatively high in the given technology. Further process adjustments can potentially reduce the supply voltage as well as the power consumption.

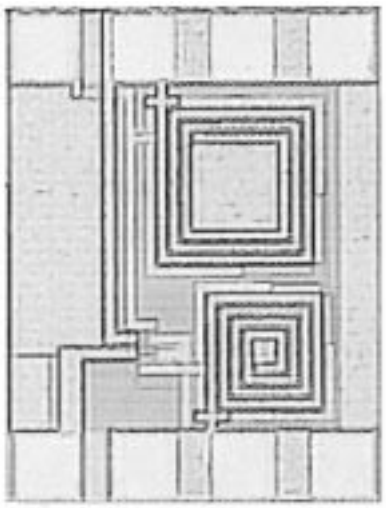


Fig. 8. Die photo of the LNA.

Fig. 9. Wire-bonding illustration of the LLP package.

be 1.1 nH to provide 50 Ω of real part of the input impedance, in combination with C_p. The inductor was designed based on the compact model presented by [17]; a patterned ground shield was employed to reduce the substrate parasitics of the spiral inductor [18]. Since the required gate inductor L_g to cancel out the imaginary part of the input impedance was 36 nH, which is too large to be integrated, an external inductor was used along with a bondwire inductor. Finally, to control the parasitic inductance from L_s to ground, the die was mounted on a special leadless leadframe package (LLP) which allows direct downbonding to the large ground plane, as shown in Fig. 9.

The complete schematic of the device under test (DUT) is shown in Fig. 10. The real term of the input impedance of the fabricated LNA was 54 Ω and was adjusted to 50 Ω using an off-chip tuner. To maximize accuracy in noise figure measurement, the output of the LNA is also impedance matched[5] using another off-chip tuner.

Fig. 11(a) and (b) shows measured third-order input intercept point (IIP3) and noise figure as well as the available gain. The measured performance of the LNA is summarized in Table I. With 3.75 mA of bias current, the LNA achieves about 0.9 dB of noise figure, which is the lowest reported noise figure with a perfect power match for a CMOS LNA, and it adds just 0.3 dB to the $NF_{\min}$ of the intrinsic MOSFET device. The measured noise figure is also quite close to the expected value and demonstrates that the proposed methodology accurately predicts the noise performance of custom integrated LNA designs.

[5]If the output is not matched, the measured noise figure needs a correction that may lead to errors [1].

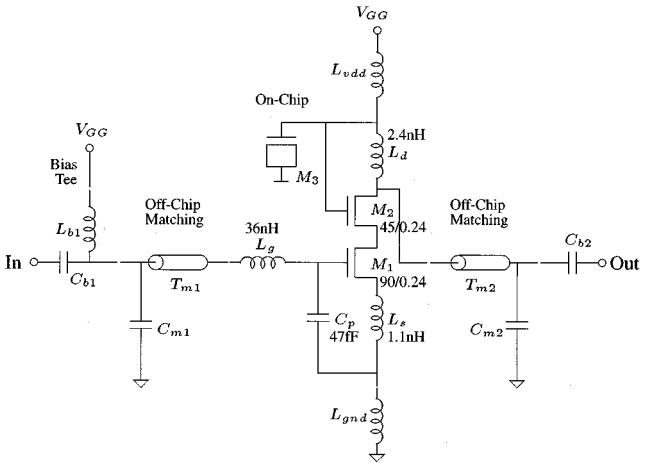
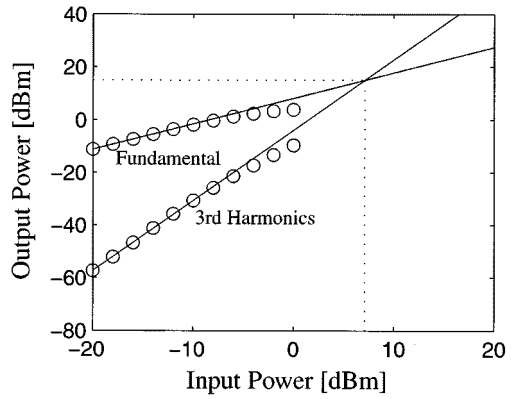
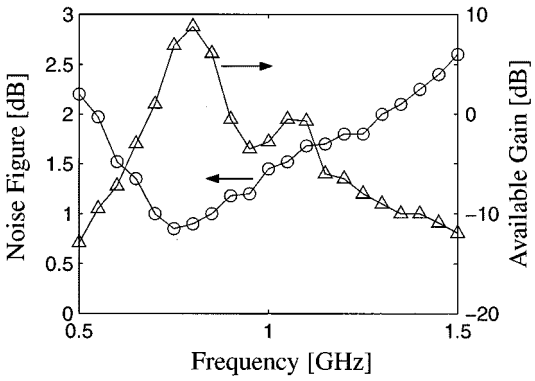


Fig. 10. Complete schematic of the LNA, including off-chip elements.



(a)



(b)

Fig. 11. Measured performance of the LNA. (a) IIP3 result. (b) Noise figure and gain.

V. Conclusion

Based on the measured noise parameters of the 0.24-μm MOSFET and on the results derived from two-port noise theory, considerations for a integrated LNA design are presented. The measured noise parameters can be scaled directly with the device width; device sizing can be utilized for power-constrained design. The noise performance of the tuned LNA is primarily controlled by the source degeneration inductance, which

TABLE I
MEASURED PERFORMANCE OF AN 800-MHz LNA

Parameters	Measured Value
Frequency	800 MHz
Supply Voltage	2.0 V
Power Consumption	7.5 mW
Noise Figure	0.9±0.2 dB
Available Gain	8.8 dB
s_{11}	-38.1 dB
$IIP3$	7.1 dBm
Die Area	0.19 mm^2

determines both the power-matching and the noise-matching conditions. Therefore, if arbitrary values of source impedance are allowed, the optimal LNA design can be obtained by adjusting the source inductance. Even if the source impedance is fixed, the integrated LNA can achieve noise performance near $NF_{\min}$ by choosing an appropriate device geometry and optimizing the bias conditions. The cascode stage usually introduces at least 40% extra noise power to the input stage; thus, its width needs to be optimized.

Although the demonstrated LNA uses a single-ended architecture, future LNA designs will require differential operation since further scaling of the device sizes requires smaller values of source inductance. Fully integrated inductors with large values and high quality factors required for L_g are an ongoing challenge. The results demonstrate that CMOS can be a good candidate for high-performance LNA designs, competitive with GaAs and bipolar LNAs.

ACKNOWLEDGMENT

The authors would like to thank Texas Instruments Incorporated for promoting and mentoring this project. Special thanks go to National Semiconductor for fabricating the chip and accommodating test equipment.

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