A Non-isolated Interleaved Boost Converter for High Voltage Gain Applications

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***Abstract*— the requirement for high voltage gain step-up DC-DC converters is becoming increasingly important in many modern power supply applications. They are an essential power conversion stage in systems such as grid connected renewables and electric vehicles. Unfortunately, achieving a low cost, high efficiency, power dense, step up converter with high voltage gain is not a trivial task; yet they are highly desirable when aiming for a green power supply solution. For this reason, this paper presents a new non-isolated interleaved dc-dc boost converter with Zero-Voltage-Switching (ZVS). The proposed converter is designed around a coupled inductor, with an active clamping circuit arrangement to recycle the coupled inductor leakage energy and reduce the voltage stress on the semiconductor devices. The lack of isolation transformer improves the power density of the system. Likewise, the interleaved circuit allows for high efficiency over a broad range of operating conditions. The theoretical behavior of the power converter is fully described, and the performance of the circuit is validated through experimental results. Importantly, the circuit is capable of achieving >10X voltage gains without the need to apply extreme modulation signals to the pulse width modulation (PWM) circuit.**

***Index Terms*— High-step-up, interleaved boost converter, non-isolated, winding coupled inductors, zero voltage switching (ZVS)**

I. INTRODUCTION

MANY green power supply applications call for a high efficiency, high step-up dc-dc converter in the power conversion stage. Typical examples include electric drives [1], grid connected inverters [2-4], electric vehicle drive trains [5], uninterruptible power supplies system (UPS) [6], telecommunication power systems, and high intensity discharge lamps [7]. Furthermore, high voltage step up gains are increasingly required when the system is powered by low voltage energy sources such as Li-ion batteries, solar arrays and fuel cells.

Theoretically, conventional non-isolated boost and buck-boost converters are the simplest pulse width modulation (PWM) controlled topologies for voltage step-up. However, these converters typically have to operate under extreme duty ratios to achieve high voltage gains. As a consequence, significant voltage and current stresses are incurred by the converter devices and poor dynamic characteristics can result in the controlled output response. Furthermore, the output diodes often sustain short, but high amplitude, current

pulses due to the narrow turn off time; which can induce reverse recovery loss [7, 8]. The power device rating increases as the output voltage increases, resulting in conduction losses which also degrade the efficiency. Rather than a conventional single stage boost converter, a cascade boost converter is an attractive solution to enlarge the voltage gain without extreme duty ratio operation. However, the controllers must be synchronized and the stability of the converter can be of concern [9]. In addition, the second stage may experience severe reverse recovery related losses in high power applications. Furthermore, the energy has to be converted twice, which obviously has an impact on overall efficiency.

Magnetically coupled converters such as forward, flyback [10, 11], push full [12], and full bridge converters [13], can achieve high voltage gain by carefully selecting the turns ratio of the high frequency transformer. However, the transformer leakage inductance can induce additional voltage stress and increase the switching losses. To go some way to mitigating these effects, energy recycling techniques can be adopted to recycle the leakage energy [7]. Transformer volume and weight is another problem that inhibits developing a compact, high power density converter. Thus, whilst functional, these types of converters do not offer an optimal solution in cost sensitive green power supply applications.

Switched capacitor and switched inductor converters [14, 15], provide an alternative method to enlarge the voltage gain without extreme duty ratio operation. Furthermore, they reduce the voltage stress on the devices. Switched capacitor technique utilizes capacitor charge transference. However, many switched capacitor stages are required to achieve very high conversion ratio; thus the circuit is typically complex. The major drawback of the switched inductor technique is the power device voltage stress is equal to the output voltage; again high voltage rated devices potentially cause significant conduction losses.

Rather than an isolation transformer, a coupled inductor can be used to overcome many of the previously mentioned problems in order to achieve efficient high voltage gain operation. In particular, large PWM duty ratios can be avoided by proper coupling inductor turns ratio design. Furthermore, only one magnetic component is required with simpler winding structure, which reduces the cost, volume, weight, and losses. Various single phase, non-isolated, high step-up converters with coupled inductors and voltage multiplier cells have been proposed to extend the voltage gain, reduce the semiconductor switching voltage stress and alleviate the output diode reverse recovery problem. However, the input current ripple is particularly large in high power applications [16-20]. The leakage energy of the coupled inductor induces significant voltage stress on the power device if no method of recycling the energy is adopted. A resistor-capacitor-diode (RCD) snubber can suppress

the device voltage stress, but the leakage energy dissipates within the snubber contributing to the losses. A passive loss-less clamp can recycle the leakage energy and reduce the device voltage stress [7], but most of these converters operate under hard switching PWM techniques [16, 17]. An active clamp circuit is usually adopted to replace the passive clamp in order to achieve Zero Voltage Switching (ZVS) for main and clamp switches [18, 20].

Interleaving is usually adopted as an effective solution in high power applications to reduce the passive component size, increase the power level, minimize the current ripple, improve the transient response, and realize thermal distribution. Various interleaved converters with passive loss-less clamps, or active clamps, have been proposed [21-27]. An interleaved active clamp coupled inductor based flyback-forward converter is proposed in [26]. In this topology, all the active switches achieve ZVS operation and the switching losses are significantly reduced due to the existence of parallel capacitors C_{s1} and C_{s2}. The voltage stress across the semiconductor devices is also reduced. However, to achieve large voltage conversion ratios, a higher coupling inductor turns ratio is required. The greater this turns ratio is, the greater the copper losses and the leakage inductance of the coupled inductor.

In this paper, a new ZVS interleaved, non-isolated, high step-up boost converter with active clamping circuit is proposed. The circuit topology is shown in Fig. 1. The converter uses two coupled inductors in both forward and flyback mode and a switched capacitor to achieve high conversion ratio. Interleaving is adopted on the primary side to share the input current and cancel the current ripple of the coupled inductors and reduce the switch conduction losses. Importantly, a low turns ratio can be employed to achieve high conversion ratios which reduces the copper losses and leakage inductance of the coupled inductor. The secondary windings of the coupled inductor are connected in series to achieve winding coupled configuration and sustain the high voltage at the output. Furthermore, the voltage stress of the active switches and diodes are reduced. By using active clamping, ZVS is achieved for all the switches. The diode reverse recovery problem is alleviated for all the diodes, hence switching losses are further reduced yielding an efficient green power supply solution.

II. Proposed Converter and its Steady State Analysis

A. Circuit Configuration and Description

Fig. 1(a) shows the structure of the proposed interleaved high step-up converter with coupled inductors and voltage multiplier cell. The converter employs two coupled inductors ($L_1$and L_2) with the same number of turns in the primary and secondary sides. The primary winding of the coupled inductor $L_{1a}$and L_{2a} serve as filter inductors like a conventional interleaved boost converter and are coupled to their corresponding secondary

windings L_{1b} and L_{2b}. The primary and secondary windings are denoted by n_1 and n_2, and the coupling references denoted by ‘’o’’ and ‘’*’’. The primary windings are in parallel to handle the large input current on the low voltage side. The secondary windings are in series on the high voltage side to achieve winding coupled configuration and enlarge the voltage gain. There are two sets of active clamp circuits, with S_{C1} and S_{C2} as the corresponding clamp switches. The voltage multiplier cell comprises of secondary windings of the coupled inductor L_{2a} and L_{2b}, the output and regenerative diodes D_O and D_r and the switched capacitor C_m.

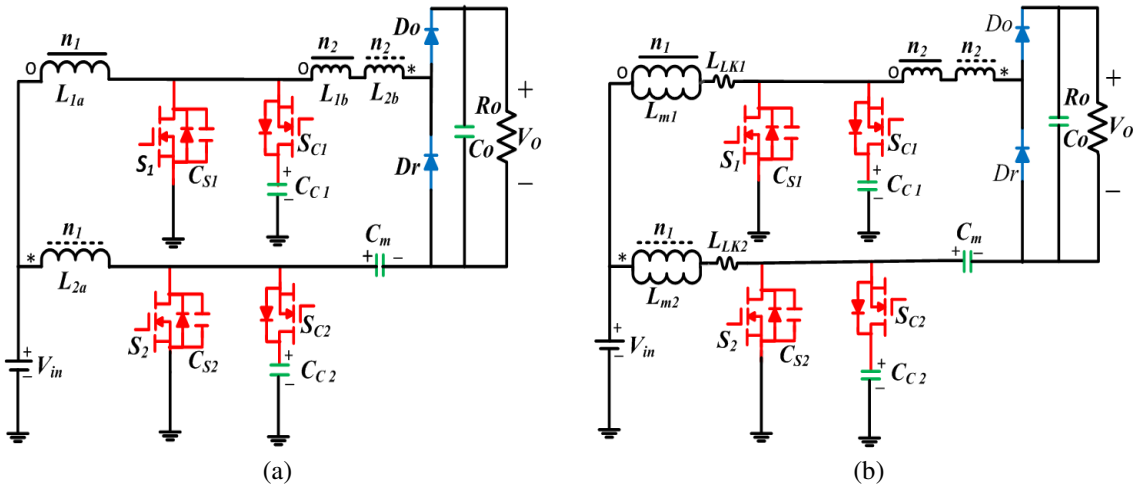


Fig.1 Proposed interleaved non-isolated boost converter
(a) Proposed coupled inductor boost converter. (b)Equivalent circuit

Fig. 1(b) shows the equivalent circuit of the proposed converter. The coupled inductors can be modeled as an ideal transformer with defined turns ratio. The primary winding of the ideal transformer is in parallel with the magnetizing inductor and in series with leakage inductance [17- 20]. L_{m1}, $L_{m2}$are the magnetizing inductance of the coupled inductors whilst L_{LK1}, L_{LK2} represent the leakage inductances of the coupled inductor in the primary side. S_1, S_2 are the main switches whereas S_{C1}, S_{C2} are the corresponding clamp switches. C_{C1}, C_{C2} are the clamp capacitors. C_{S1} and C_{S2} are the added parallel capacitors to implement ZVS, and include the parasitic capacitance of the main and clamp switches. C_O denotes the output capacitor and V_{in} and V_O represent the input and output voltages respectively.

B. Steady State Operational Analysis

The proposed converter is designed to operate in continuous conduction mode (CCM), the duty cycle D of the main switches S_1 and S_2 are the same and phase shifted 180°. During steady-state operation the duty cycle is higher than 0.5. The gate signal of the clamp switches S_{C1} and S_{C2} are complimentary to their corresponding main switches S_1 and S_2. The steady state theoretical waveform of the converter is shown in in Fig. 2. There

are sixteen modes of operation in one switching cycle. The equivalent circuits corresponding to each mode are shown in Fig. 3. In order to simplify the analysis, the leakage inductances L_{LK1} and L_{LK2} were reflected from primary to the secondary side as equivalent leakage inductance and denoted by L_K.

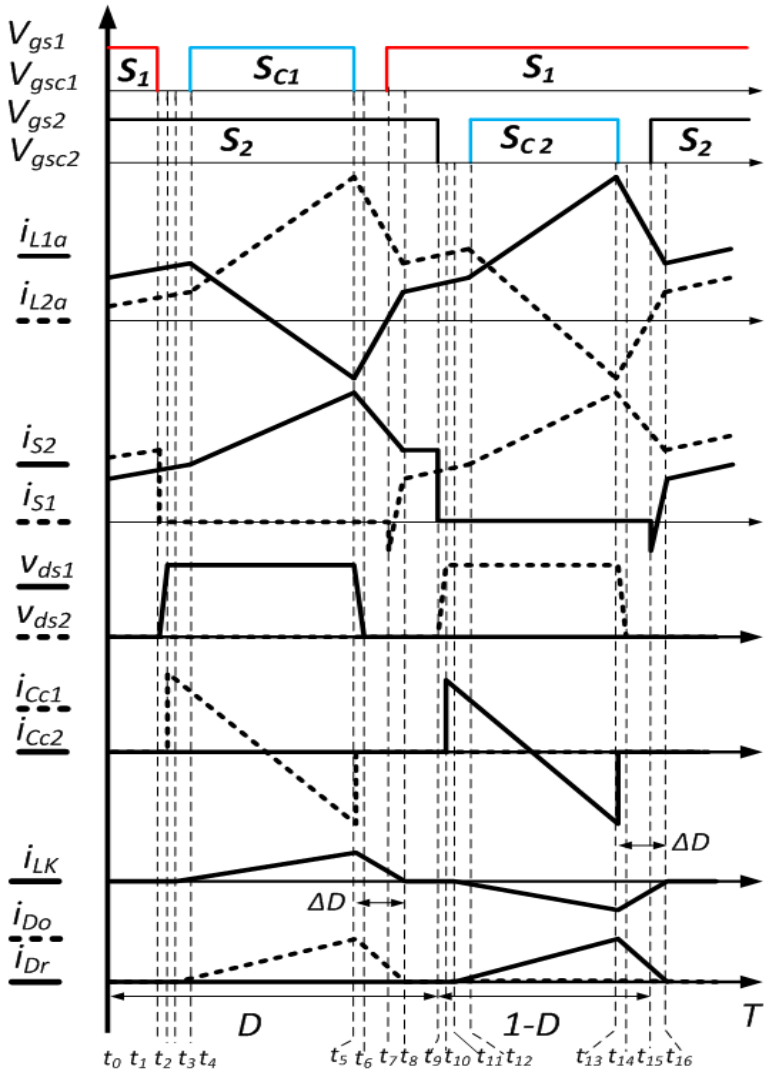


Fig. 2 Steady state theoretical waveforms

Mode 1 $[t_0 - t_1]$ (Fig. 3a): During this state, the main switches $S_1$and S_2 are on, the clamp switches S_{C1} and S_{C2} are off. The output and regenerative diodes D_O, D_r are reversed biased. Magnetizing inductors $L_{m1}$and L_{m2} are charged linearly by the input voltage, as demonstrated by (1) and (2).The load is supplied by the energy stored in the output capacitor.

$$i_{Lm1}(t) = I_{Lm1}(t_0) + \frac{V_{in}}{L_{m1}}(t - t_0) \tag{1}$$

$$i_{Lm2}(t) = I_{Lm2}(t_0) + \frac{V_{in}}{L_{m2}}(t - t_0) \tag{2}$$

Mode 2 $[t_1 - t_2]$ (Fig. 3b): The main switch S_1 turns off at time t_1, the drain source voltage increases linearly, due to parallel capacitor C_{S1}, the main switch S_1 turns off with ZVS. The magnetizing inductor current is high and requires very short time to charge the capacitor C_{S1}. The equivalent leakage inductance current I_{Lk} rises linearly.

$$v_{ds1}(t) \approx \frac{I_{Lm1}(t_1)}{C_{s1}}(t - t_1) \tag{3}$$

Mode 3 $[t_2 - t_3]$ (Fig. 3c): At time t_2, the drain source voltage of main switch S_1 started to be slightly higher than the clamp capacitor voltage V_{Cc1}, and the drain source voltage of the clamping switch S_{C1} reduces to zero which causes the antiparallel diode to conduct. The magnetizing inductor current is commutated to the antiparallel diode, and current begins to flow through to the clamping capacitor C_{c1}, since it is much larger than C_{s1}. The voltage of the main switch S_1 is clamped to the voltage of C_{c1}.

$$v_{ds1}(t) \approx \ V_{ds1}(t_2) + \frac{I_{Lm1}(t_2)}{C_{C1}}(t - t_2) \tag{4}$$

Mode 4 $[t_3 - t_4]$ (Fig 3d): The output diode starts conducting at t_3, the energy is transferred to the load. Consequently, the coupled inductor L_1 acts as a filter inductor and L_2 acts as a transformer. The secondary windings of the coupled inductors and the switched capacitor C_m serve as voltage sources that enlarge the voltage gain. The rate of change of current through the output diode is controlled by the equivalent leakage inductance L_K. The input voltage still charges the magnetizing inductor L_{m2} linearly. During this stage

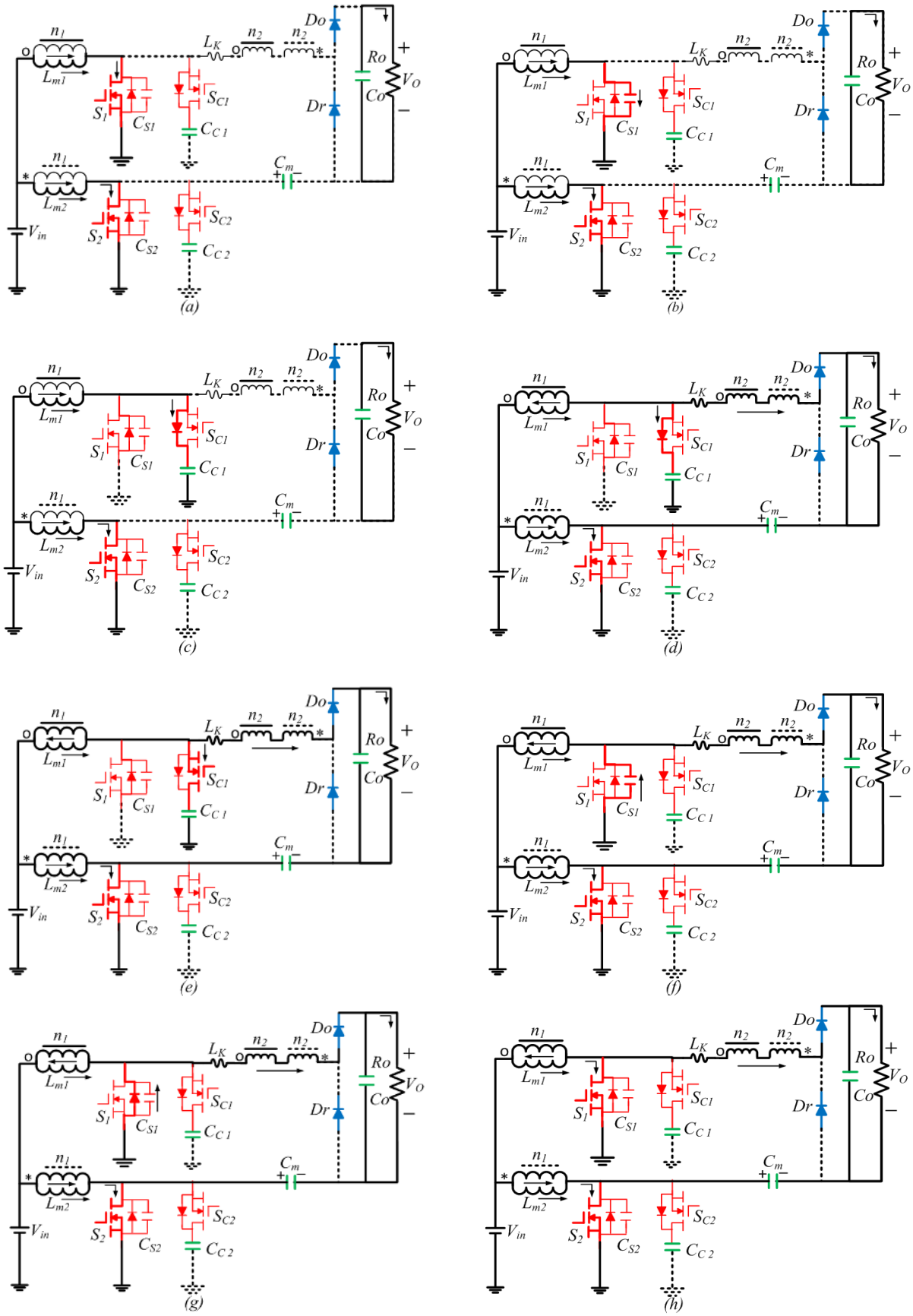
$$i_{Lm1}(t) = I_{Lm1}(t_3) - \frac{\left[\left(V_o - V_{Cm}(t_3)\right)\right]/N - V_{in}}{L_{m1}}(t - t_3) \tag{5}$$

$$i_{Lk}(t) = \ i_{Cm}(t) = \frac{[N+1]V_{Cc1} + V_{Cm} - V_O}{L_K}(t - t_3) \tag{6}$$

Where *N* is defined as the turn's ratio of the coupled inductor n_2/n_1

Mode 5 $[t_4 - t_5]$ (Fig. 3e): The gate signal of S_{C1} can be applied at t_4 since its antiparallel diode is conducting. The clamp switch S_{C1} turns-on with ZVS, and the energy stored in the magnetizing inductor current continues to flow to the clamping capacitor C_{c1}.

Mode 6 $[t_5 - t_6]$ (Fig. 3f): At time t_5, S_{C1} turns-off, and the clamp circuit is therefore disconnected. The voltage of the parallel capacitor C_{S1} decreases, while that of the clamp switch S_{C1} increases from zero at the same rate. Therefore the clamp switch S_{C1} turns off with ZVS. The equivalent leakage inductor current i_{Lk} reaches its peak and starts to decrease linearly at the end of this mode.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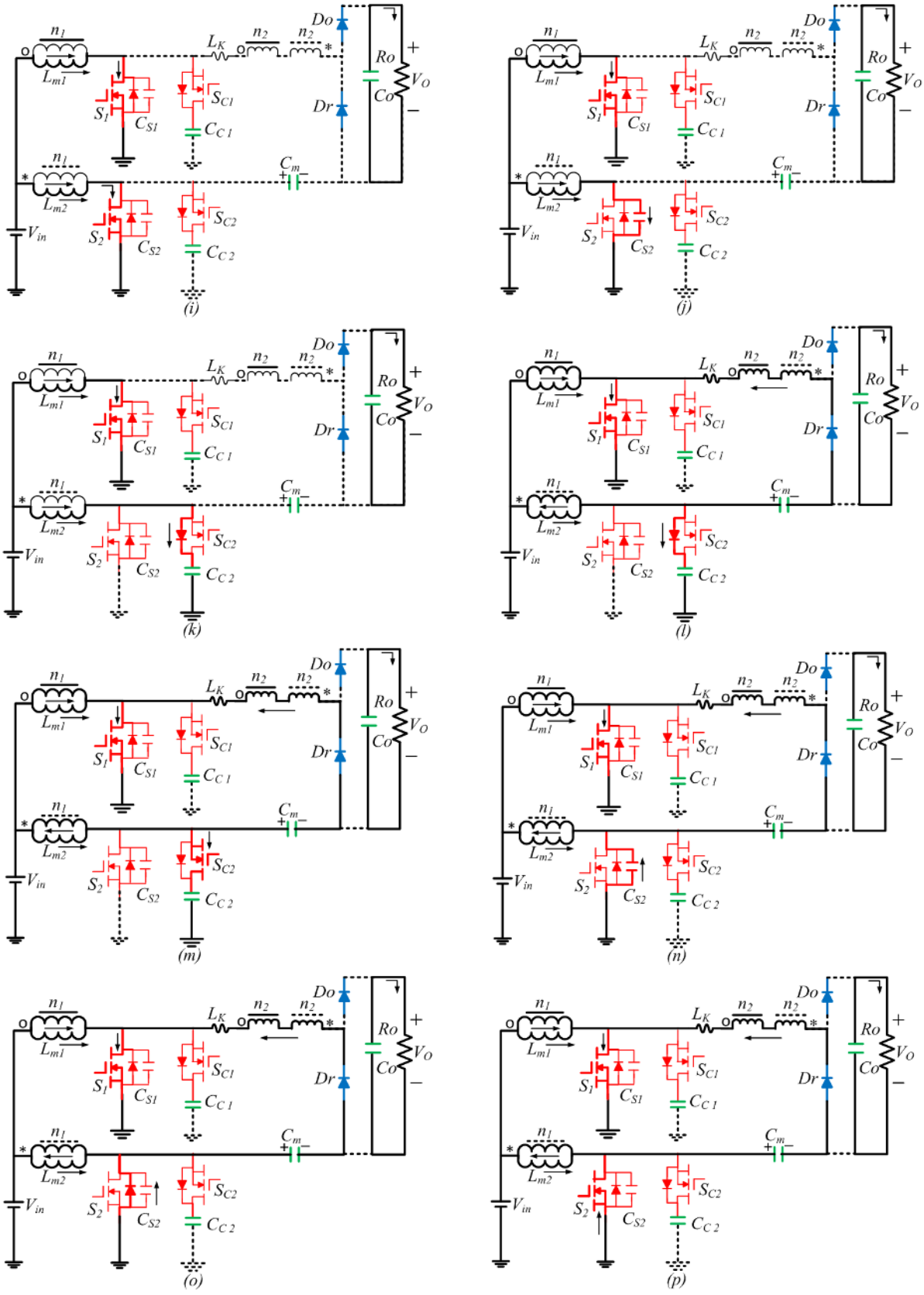


Fig. 3 Equivalent circuits

(a) Mode 1[t_0 - t_1], (b) Mode 2 [$t_1 - t_2$], (c) Mode 3 [$t_2 - t_3$], (d) Mode 4 [$t_3 - t_4$], (e) Mode 5 [$t_4 - t_5$], (f) Mode 6 [$t_5 - t_6$], (g) Mode 7 [$t_6 - t_7$], (h) Mode 7 [$t_7 - t_8$], (i) Mode 8[$t_8 - t_9$], (j) Mode 9 [$t_9 - t_{10}$], (k) Mode 10 [$t_{10} - t_{11}$], (l) Mode 11 [$t_{11} - t_{12}$], (m) Mode 12 [$t_{12} - t_{13}$], (n) Mode 13 [$t_{13} - t_{14}$], (o) Mode 14 [$t_{14} - t_{15}$], (p) Mode 15 [$t_{15} - t_6$].

Mode 7 [$t_6 - t_7$] (Fig. 3g): At t_6, the voltage across C_{s1} reduces to zero, and its antiparallel diode begins to conduct. The output diode current decreases linearly, the current falling rate is controlled by the leakage inductance L_{LK1}

Mode 8 [$t_7 - t_8$] (Fig. 3h): The gate signal of main switch S_1 is applied at this instant, since its antiparallel diode is conducting main switch S_1 turns on with ZVS. Output diode D_O is still conducting. At the end of this mode D_O turns off softly with zero-current-switching (ZCS) and the equivalent leakage inductance current i_{Lk} reaches zero.

Mode 9 [$t_8 - t_9$] (Fig. 3i): Before t_9, main switches S_1 and S_2 are conducting, the clamp switches S_{C1} and S_{C2} are off. The regenerative and output diode D_r, D_O are reversed biased. Magnetizing inductors L_{m1} and L_{m2} are charged linearly by the input voltage. The output capacitor supplies the load. The equivalent circuit of this mode is exactly the same with that of Fig 3(a).

Mode 10 [$t_9 - t_{10}$] (Fig. 3j): The main switch S_2 turns off at t_9. The parallel capacitor C_{S2} is then charged by the magnetizing current of i_{Lm2}. Due to parallel capacitor C_{S2}, the main switch S_2 turns off with ZVS.

Mode 11 [$t_{10} - t_{11}$] (Fig. 3k): At t_{10}, the drain source voltage of the main switch S_2 reaches the clamp capacitor voltage V_{Cc2}, the current through the main switch S_2 is commutated to the antiparallel diode of clamp switch S_{C2} and S_{C2} begins to conduct. The main switch voltage S_2 is clamped to the clamp capacitor voltage.

Mode 12 [$t_{11} - t_{12}$] (Fig. 3l): At t_{11} the regenerative diode begins to conduct. As a result, the coupled inductor L_1 works as a filter inductor and L_2 works as transformer thus, the switched capacitor is C_m charged. The magnetizing inductor L_{m1} is still charge by the input voltage.

Mode 13 [$t_{12} - t_{13}$] (Fig. 3m): The turn on gate signal to S_{C2} is applied at t_{12} to implement ZVS whilst the antiparallel diode is conducting.

Mode 14 [$t_{13} - t_{14}$] (Fig. 3n): The clamp switch S_{C2} turns off at t_{13}. The active clamp circuit is disconnected. Due to the parallel capacitor C_{S2}, the clamp switch S_{C2} turns off under ZVS conditions.

Mode 15 [$t_{14} - t_{15}$] (Fig. 3o): At t_{14}, the parallel capacitor of main switch S_2 is discharged by the coupled inductor primary current and reflected leakage inductor current. Therefore, its antiparallel diode starts conducting.

Mode 16 [$t_{15} - t_{16}$] (Fig. 3p): The turn on gate signal to S_2 is applied at t_{15}, to implement ZVS conditions whilst its antiparallel diode is conducting. At the end of this mode the equivalent leakage inductor current decreases to zero and the regenerative diode turns off with ZCS conditions. A new switching cycle then ensues in similar fashion.

III. STEADY STATE CONVERTER ANALYSIS

A. Voltage Gain

Under ideal condition, the coupled inductors are assumed to be perfectly coupled and the leakage inductance is considered to be zero. The power switches are lossless with zero conduction voltage drops; all the capacitors voltages are assumed to be constant. The parallel capacitors are ignored. Hence the voltage on the main and clamp switches are equal to those on the clamp capacitors. They are denoted by

$$V_{ds1} = V_{ds2} = V_{dsc1} = V_{dsc2} = \frac{V_{in}}{(1-D)} \tag{7}$$

During the interval in which main switch S_1 is off and main switch S_2 is on, the energy is delivered to the load and the output voltage can be expressed as

$$V_o = V_{cc} + NV_{in} + N(V_{cc} - V_{in}) + V_{cm} \tag{8}$$

Applying volt-second balance on the equivalent leakage inductance during modes [2-8], the voltage across the switched capacitor is derived as

$$V_{cm} = \frac{V_o}{2} \tag{9}$$

From (7), (8), and (9) the ideal voltage gain is given by

$$M_{ideal} = \frac{V_o}{V_{in}} = \frac{2N+2}{(1-D)} \tag{10}$$

From (10), it is obvious that a high conversion ratio can be obtained without an extreme duty cycle operation. Two degrees of freedom exist to enlarge the voltage gain (duty cycle and coupled inductor turns ratio). These features make the converter suitable in high step-up applications. However, the inherent leakage inductance of the coupled inductors is responsible for achieving the ZVS of both main and clamp switches and control the current falling rate of the regenerative and output diodes. The leakage inductance should not be ignored, once it is considered the voltage gain can be derived.

In Fig. 2 a parameter ΔD is define as the time interval $(t_5 - t_8)$ which represent the time it takes the equivalent leakage inductor current to fall from its peak value to zero. Using this parameter and applying the volt second balance equation to the equivalent leakage inductor L_K, during the interval $(t_3 - t_8)$ gives

$$\frac{V_{Cm}}{V_{Cc}} = \frac{(1-D)(N+1)}{(1-D+\Delta D)} \tag{11}$$

From (7), (9) and (11) the voltage gain is derived as

$$M = \frac{V_o}{V_{in}} = \frac{2N+2}{(1-D+\Delta D)} \tag{12}$$

Using the slope of the equivalent leakage inductor current waveform in Fig. 2, the peak value of the regenerative and output diode currents can be expressed as

$$I_{Do\_pK} = I_{Dr\_pK} = \frac{[N+1]V_{Cc} + V_{Cm} - V_O}{L_K}(1-D)T_s \tag{13}$$

Where T_s is the switching period. The average value of the output current is the same with the average value of the diode currents, the peak diode current can be denoted by

$$I_{Do\_pK} = I_{Dr\_pK} = \frac{2I_O}{(1-D+\Delta D)} \tag{14}$$

From (7), (9) and (12)-(14), the parameter ΔD is derived as

$$\Delta D = \frac{4I_O L_{LK} f_S}{2(N+1)V_{in} - V_O(1-D)} - (1-D) \tag{15}$$

From (12) and (15), the voltage gain is derived as

$$M = \frac{V_o}{V_{in}} = \frac{4(N+1)}{(1-D) + \sqrt{(1-D)^2 + Q}} \tag{16}$$

Where $Q = 16 \cdot f_s \cdot L_k / R_O$. Q is the parameter that represents the effect of equivalent leakage inductance and R_O is the load resistance. Once the leakage inductance is zero, equation (16) is exactly the same with (10). From (16), the relationship between Q and N as a function of duty ratio D is shown in Fig. 4

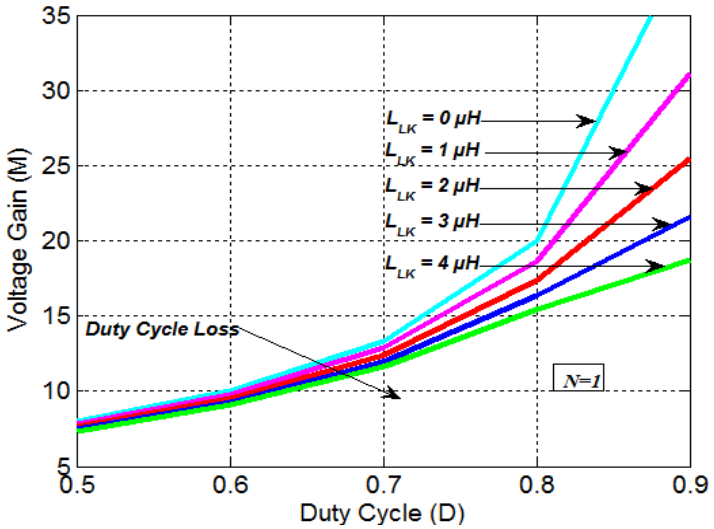


Fig. 4 Voltage gain characteristic of the converter for various Q and N values as a function of duty ratio D

B. Voltage Stress Analysis

The voltage stress of the main and clamp switches of the converter are the same and are derived in (7), by neglecting the voltage ripple on the clamp capacitors. The voltage stress related to the output voltage is given by

$$V_{ds1} = V_{ds2} = V_{dsc1} = V_{dsc2} = \frac{V_O}{2(N+1)} \tag{17}$$

The voltage stress of the diodes is equal to the output voltage and expressed as

$$V_{Do} = V_{Dr} = V_O \tag{18}$$

C. ZVS Soft Switching performance

The ZVS turn on and turn off is due to the existence of the clamp circuit and parallel capacitors C_{s1} and C_{s2}. To ensure ZVS of the main switches, the drain-source voltage of S_1 should be decreased to zero before it turn-on gate signal is applied. It can be seen from Fig. 3h, the parallel capacitor C_{S1} is discharged by coupled inductor primary current I_{L1a} at time t_7, to ensure ZVS of the main switch (19) the should be satisfied

$$L_{Lk1} I_{L1a}^2 (t_7) \geq \frac{C_{S1} V_{Cc}^2}{2N^2} \tag{19}$$

The coupled inductor primary current I_{L1a} is the difference between the equivalent leakage inductor current and magnetizing inductor current, which is derived as

$$I_{L1a}(t) = I_{LK}(t) - I_{Lm1}(t) \tag{20}$$

The peak value of the equivalent leakage inductor current is derived in (6). And the magnetizing inductor current at time (t_7) given by (21)

$$I_{Lm1}(t_7) = \frac{P_o}{2\,V_{in}} - \frac{V_{in} D}{2 L_{m1} f_s} \tag{21}$$

From (6), and (20)-(21), the coupled inductor primary current is obtained as (22).

$$I_{L1a} = \frac{V_{in}^2\big(L_k D + 2L_{m1}(N+1)\big) - V_{in} V_o L_{m1}(1-D) - K}{2\,V_{in}\,L_{m1}\,L_k f_s} \tag{22}$$

where $K = P_o\,L_{m1}\,L_k\,f_s$. From (19) and (22) the ZVS range of the main switch as function of input voltage and output power can be obtained.

IV. Design Considerations

A. Coupled Inductor Turns Ratio Design

The main design step is to select the proper turns ratio that will allow low voltage rated devices to be used. The coupled inductors turns ratio is obtained from (10), once the duty cycle is chosen and is given by

$$N = \frac{n_2}{n_1} = \frac{(1-D)V_O}{2V_{in}} - 1 \tag{23}$$

B. Leakage Inductance Design

The leakage inductance is designed to ensure (ZVS) of the main and clamp switches, and to limit the current falling rate of output and regenerative diodes. It is derived from (16) and expressed as

$$L_K \leq \frac{2R_0(N+1)^2 - MR_0(N+1)(1-D)}{2M^2 f_s} \tag{24}$$

By assuming that all the coupled inductance have the same leakage inductance, each coupled inductor leakage inductance reflected to the primary side is

$$L_{Lk1} = L_{Lk2} = \frac{L_k}{2N^2} \tag{25}$$

C. Magnetizing Inductor Design

A good criterion for designing the magnetizing inductance is to maintain the continuous inductor current mode, and set an acceptable current ripple in the magnetizing inductor such that

$$L_{m1} = L_{m2} = \frac{V_{in}D}{\Delta I_{Lm} f_s} \tag{26}$$

Where ΔI_{Lm} is the magnetizing inductor current ripple.

D. Clamp and Switched Capacitor Design

The voltage ripple is the main consideration in designing the clamp and switched capacitors. To suppress the voltage spikes of the main switch and avoid resonant ringing. The clamp capacitor can be chosen from (27)

$$C_C = \frac{(N+1)I_O}{4\Delta V_{Cc} f_s} \tag{27}$$

The switched capacitor serves as a voltage source in the converter. During steady state, the capacitor stores half of the output voltage and the average output current flow through it. The ripple voltage should be limited to a reasonable value.

$$C_m = \frac{I_O}{\Delta V_{Cm} f_s} \tag{28}$$

Where ΔV_{Cc} and ΔV_{Cm} are the voltage ripple of the clamp and switched capacitors.

V. EXPERIMENTAL VALIDATION

To validate the theoretical analysis a 500 W prototype is built and tested. The parameters of the converter along with the component ratings are shown in Table I. The experimental results are shown in Fig. 5. under full load condition with $V_{in} = 12\ V$.

TABLE I

CONVERTER PARAMETERS

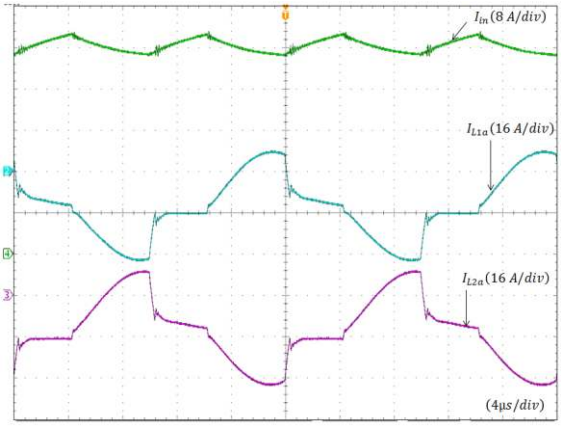
Output Power (P_O)	500 W
Input Voltage (V_{in})	12-14 V
Output Voltage (V_O)	120 V
Switching Frequency (f_s)	50 KHz
Main Switches $(S_1 \; and \; S_2)$	FDP047AN
Clamp Switches $(S_{C1} \; and \; S_{C2})$	FDP047AN
Output and Regenerative Diodes $(D_O \; and \; D_r)$	MBUR42050G
Clamp capacitors $(C_{C1} \; and \; C_{C2})$	10 µF
Switched Capacitor (C_m)	10 µF
Output capacitor (C_O)	22 µF
Turns Ratio (n_2/n_1)	13:13
Magnetizing Inductance $(L_{m1} \; and \; L_{m2})$	35 µH
Leakage Inductance $(L_{k1} \; and \; L_{k2})$	1.6 µH

Fig. 5(a) shows the input current and primary currents of two coupled inductors, thus illustrating the interleaving effect, although the primary current ripple is large, but the input current ripple is small. Fig. 5(b) shows the ZVS of the main switch S_1 and clamp switch S_{C1}, similarly the ZVS performance of the main switch S_2 and the corresponding clamp switch S_{C2} is shown in Fig. 5(c). It can be seen that both devices are switched with ZVS operation. Fig. 5(d) shows the clamp circuit performance, when either of the main switches turns off; the current starts to follow through the corresponding clamp switch to the clamp capacitor. The drain source voltage of the main switch is then clamped to that of the clamp capacitor and the voltage spikes of the leakage inductance are suppressed. The clamp capacitor current and voltage waveforms are shown in Fig 5(e). It can be seen that the clamp capacitor voltage stress is the same for all the active devices.

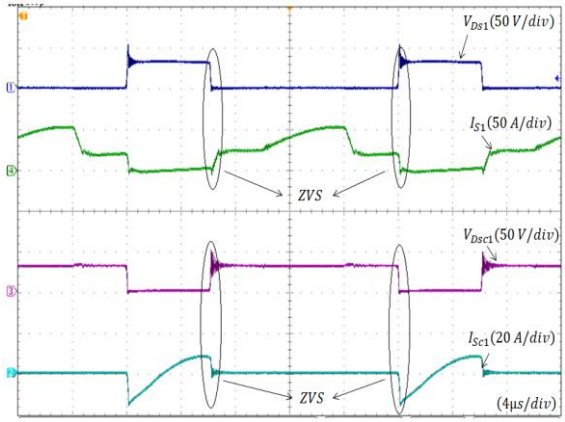
Fig. 5(f) illustrates the regenerative and output diode current and voltage waveforms. It can be seen both diodes turn off softly with ZCS leading to alleviation of the reverse recovery related losses. The voltage stresses of the diodes are equal to the output voltage. It is worth mentioning that the duty ratio of the converter is 0.7 which shows the impact of proper turns ratio design. Importantly, the results are consistent with the theoretical analysis. Fig. 6 demonstrates the closed loop transient and steady state performance of the converter. Here, a step change in load resistance is applied, causing a step increment in output power from 100 W to 500 W and vice versa. The results clearly show that the desired output voltage is well regulated, with zero steady state error. Likewise, at the point of load change, the transient characteristics are well within acceptable limits for a

converter of this type; the output voltage peak overshoot is <5% and the settling time is approximately 0.02 µs. Fig. 7 shows the measured efficiency of the prototype converter corresponding to different loads to the circuit.

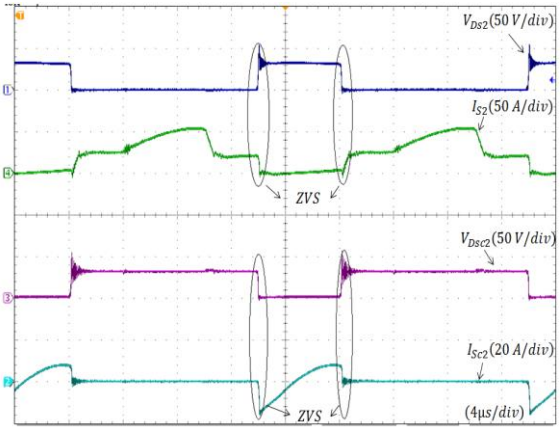
A maximum efficiency of 96.8% is recorded at 150 W and the lowest efficiency is 91.2% at 500 W. The computed Euro efficiency (an averaged operating efficiency over a yearly power distribution corresponding to middle-Europe climate) of the converter is 94.46%. Based on the experimental nature of the prototype converter, in which printed circuit board (PCB) design compromises are necessary to demonstrate the full switching operation of the circuit, further efficiency improvement should be possible in a production ready circuit. It is also worth mentioning that careful attention to the design of the coupling inductor is key to achieving optimum circuit performance; higher efficiency and excellent coupling between the windings is essential to reduce the duty cycle loss cause by the leakage inductance which degrade the efficiency.



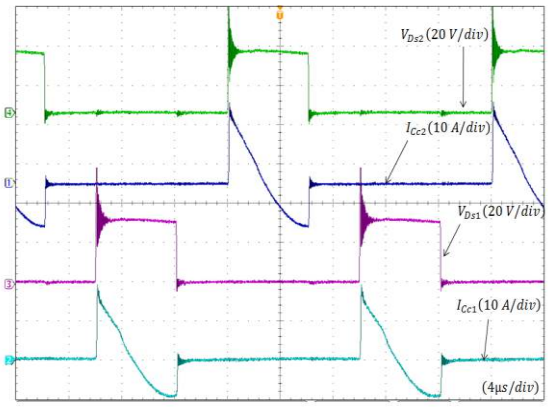
(a)



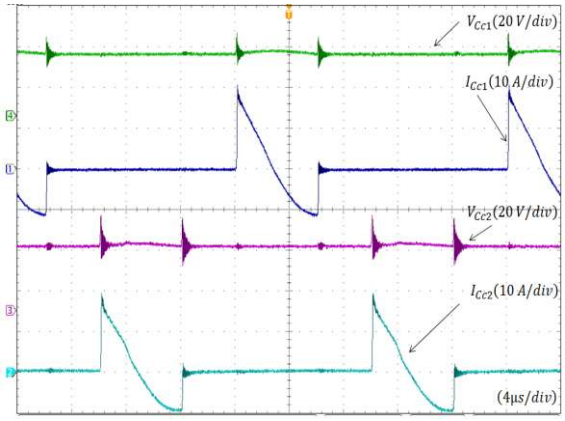
(b)



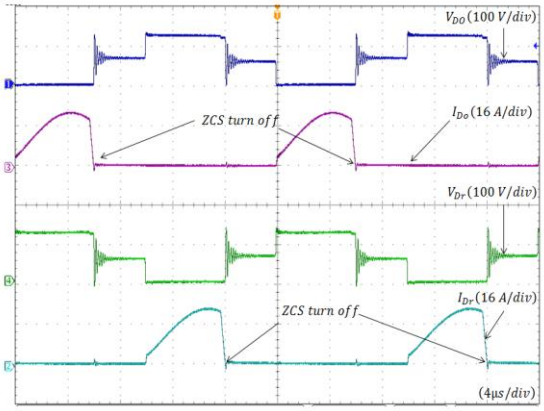
(c)



(d)



(e)



(f)

Fig. 5 Experimental results
(a) Input currents (b) ZVS of main and clamp switch (c) ZVS of main and clamp switch (d) Clamp circuit Performance (e) Clam capacitor voltage and current waveforms (f) ZCS turn off of Diodes

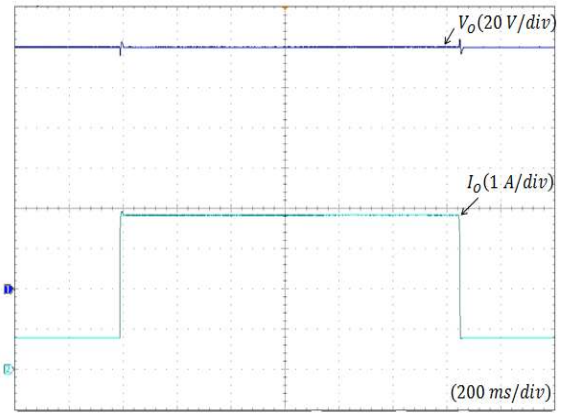


Fig. 6 Load variation between P_o= 100 W (20 % load) and Po= 500 W (full load)

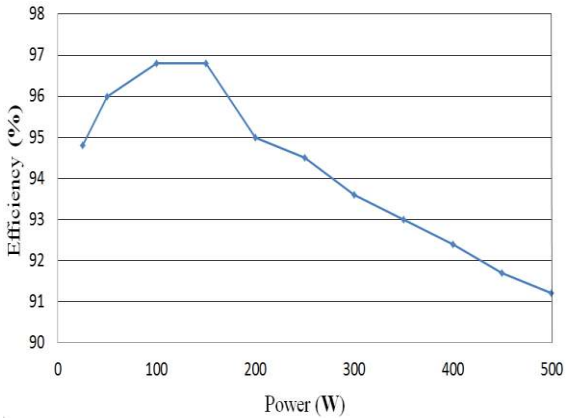


Fig. 7 Measured Efficiency of the converter

VI. CONCLUSION

This paper presents a new interleaved, non-isolated, ZVS converter; based around a winding coupled inductor approach. The circuit is specifically designed for high voltage gain applications, which are becoming increasingly more widespread. In an era of energy conservation, and a requirement for green credentials, the power converter topology minimizes conduction and switching losses, recycles leakage energy from the coupled inductor, and reduces the voltage stress across semiconductor devices. This paper presents a full analysis of the circuit's principle of operation. Experimental results from a 500 W, 10x voltage gain, prototype dc-dc converter validate the proposed theory.

Importantly, the results demonstrate that the circuit is capable of achieving excellent output voltage regulation, a rapid transient response to step load changes, and achieves high efficiency operation over a wide range of load conditions. Unlike many other solutions, the proposed circuit does not require extreme PWM modulation signals to achieve high boost ratios. Such characteristics make the proposed power converter a strong candidate in many emerging dc-dc power supply applications.

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