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Research Article

A Nonisolated Single-Switch Coupled Inductor-Based DC-DC Converter with High Voltage Gain for Renewable Power Generation Systems

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This article proposed a new structure of nonisolated high step-up DC-DC converter based on a three-winding coupled inductor and voltage multiplier cells (VMCs) for renewable energy systems applications such as PV power generation. Continuous input current with low ripple, common ground between output and input ports, low voltage stress across semiconductors, low number of components, high voltage gain, and high efficiency are the main advantages of the proposed converter. In order to further increase the output voltage, the windings of the coupled inductor are combined with VMC. The combination of coupled inductor and VMC technique leads to a high voltage gain with low duty cycle, and therefore the conduction loss of power switch is reduced. Additionally, the diodes' reverse recovery currents are reduced which improve the presented topology's efficiency. On the other hand, the used VMCs clamp the voltage, and the peak voltages across power switch are decreased. The operational modes, steady-state, and efficiency analysis are discussed. Also, to demonstrate the performance of the recommended converter, an experimental prototype with 580 W output power and 400 V output voltage with the switching frequency of 25 kHz is built and the experimental results are presented. Also, another 1 kW, 400 V with the switching frequency of 50 kHz has been implemented and tested.

1. Introduction

Due to increased energy consumption, environmental degradation, and the decrease of fossil resources, the generation of electricity from renewable energy sources such as photovoltaic (PV) and wind has increased dramatically in recent years [1, 2]. However, owing to uncertain climatic circumstances, these types of energy sources have low output voltage and nonregulated output power with low dependability [3, 4]. DC-DC converters are used to improve and manage the output voltage of renewable energy sources [5, 6]. The traditional boost PWM converter may be used to increase the voltage. However, due to voltage gain limitations, it cannot be employed for high voltage applications [7, 8]. In fact, to increase the voltage conversion ratio even more, the power switch of this converter should be set to a high number [9]. As a result, there is a large conduction power loss and a low efficiency [10, 11]. The peak voltage on the power switch and diode of the traditional boost design, on the other hand, is equivalent to the output voltage [12]. As a result, high-rated semiconductors should be employed for this converter's implementation. To address this issue, high step-up converters with higher voltage conversion ratios are proposed for renewable energy producing systems, as seen in Figure 1 [13]. Isolated/nonisolated, unidirectional/bidirectional, soft switched/hard switched, current feed/voltage feed, and nonminimum phase/minimum phase are the several categories of high step-up topologies [14]. Various methods for increasing voltage gain are also presented, including switched capacitors, VMC, magnetic coupling (magnetically coupled based, tapped inductor, isolated, and built-in transformer), and multistage techniques such as interleaved, multilevel, and cascaded (hybrid and quadratic) [15].

Isolated high step-up converters with a single switch are proposed in [16, 17]. An isolated transformer achieves

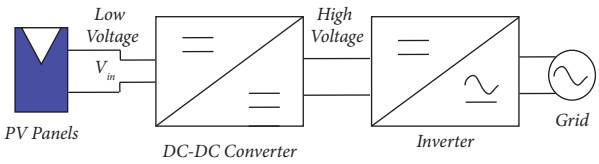


Figure 1: Application of the high step-up DC-DC converter in grid-connected PV systems.

galvanic isolation between the input and output sides. Furthermore, these topologies offer exceptional efficiency due to semiconductor ZVS and ZCS. Nonisolated structures are less in size, volume, and cost than isolated topologies. Furthermore, common ground between input and output ports is possible. The magnetic coupling approach can be employed as a coupled inductor in this sort of DC-DC converter. In addition, the windings of the coupled inductor are paired with VMCs to enhance the output voltage even further. Another advantage of the coupled inductors is that they have two or three windings on a single magnetic core. As a result, the converter's volume is decreased [18].

There are numerous high step-up DC-DC converters topologies published in the articles. Reviewing all the converters is not possible. However, some more competitive ones are surveyed here. Heidari et al. and Wong et al. [19, 20] suggested nonisolated boost converters based on VMC and coupled inductor. These topologies benefit from high voltage gain, high power efficiency, and low voltage stress across semiconductors. However, the coupled inductor's main side is in series with the input side. As a result, the fundamental shortcoming of these converters is input current with excessive ripple. On the input side, a low-pass filter can be used to decrease the ripple of the input current. However, this process increases the cost and volume. Khalilzadeh and Abbaszadeh [21] described a nonisolated high step-up converter with high voltage gain and low voltage stress. The main benefits of this converter are its high efficiency, ease of control, and recycling of leakage energy. However, this topology has a pulsating high-ripple input current. For renewable energy applications, a low input current ripple high step-up SEPIC-based nonisolated DC-DC converter is presented in [22]. The limited number of components in this topology results in good efficiency. However, its voltage gain is lower than that of other comparable converters. Alghaythi et al. and Kurdkandi and Nouri [23, 24] presented an interleaved high step-up coupled inductor-based converter with high voltage gain for renewable energy applications. The interleaved structure results in reduced input current ripple. Nonetheless, because of the large number of the diodes and the capacitors, these topologies are high-volume and expensive topologies.

In this article, a topology of nonisolated high step-up DC-DC converter is proposed for renewable applications such as PV power generation. The presented converter is designed based on coupled inductor and VMC technique. The main benefits of the presented topology are as follows:

(1) Continuous input current with low ripple
(2) Low voltage stress across semiconductors
(3) Common ground between input and output ports
(4) High voltage gain
(5) Low volume and cost
(6) High power efficiency

To attain a high output voltage, the secondary side of the coupled inductor is combined with VMC, which leads to a high voltage gain with low duty cycle, and as a result, the conduction loss of the power switch is reduced. The used VMCs act as voltage clamps, and the peak voltage on the power switch is reduced. The converter is presented and its operation modes are analyzed in Section 2. Its steady-state analysis is presented in Section 3. The converter design considerations and its efficiency analysis are given in Sections 4 and 5, respectively. The comparative studies and experimental results are presented in Sections 6 and 7, respectively.

2. The Proposed Topology and Its Operation Modes Analysis

The circuit of the suggested topology is depicted in Figure 2. Based on the figure, there are four power didoes (D_1, D_2, D_3, and D_4), one power switch (S), five capacitors (C_1, C_2, C_3, C_4, and C_5), an input inductor (L_{in}), and one coupled inductor with three windings in the presented converter's structure. The coupled inductor is assumed as an ideal transformer including leakage and magnetizing inductances (L_k and L_m) and turns ratio $N = n_3/n_1 = n_2/n_1$. The input inductor is used to reduce the input current ripple, which is essential for renewable energy sources. The windings of the coupled inductor are combined the voltage multiplier (diode/capacitor) cells to increase the output voltage. This combination leads to a high voltage gain with low power switch's duty cycle.

The key waveforms are depicted in Figure 3. There are two operation modes in each switching period (T_s). These modes are explained in the rest of this section.

2.1. Mode 1 ($t_0 < t < t_1$). This mode starts at $t = t_0$, when power switch S is turned ON by applying PWM pulse to the gate. During mode 1, only D_2 is forward biased, and other diodes are turned OFF. The voltage across input inductor L_{in} is equal to V_{in}. Therefore, its current is increased. The voltage over leakage and magnetizing inductances is equal to $(V_{C1} - V_{C5})$, which is a negative voltage. Thus, i_{Lk} and i_{Lm} are decreased. Capacitor C_3 is discharged to the coupled inductor's secondary side and capacitor C_2 through diode D_2. Furthermore, capacitors C_4 and C_5 are discharged to the output load. This mode ends when power switch S and diode D_2 are turned OFF. The equivalent structure of mode 1 is depicted in Figure 4(a):

$$V_{L_{\text{in}}} = V_{\text{in}}, \tag{1}$$

$$NV_{L_m} = V_{C_3} - V_{C_2}, \tag{2}$$

$$V_{L_m} = V_{C_1} - V_{C_5}, \tag{3}$$

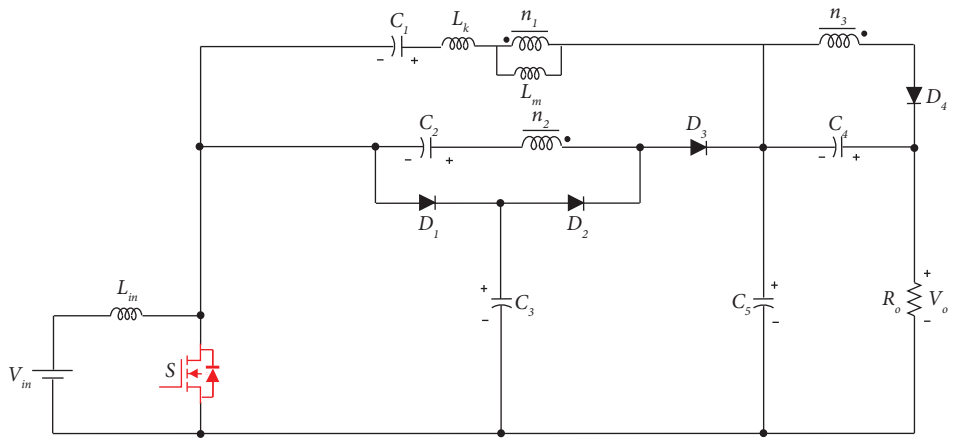


Figure 2: The proposed converter.

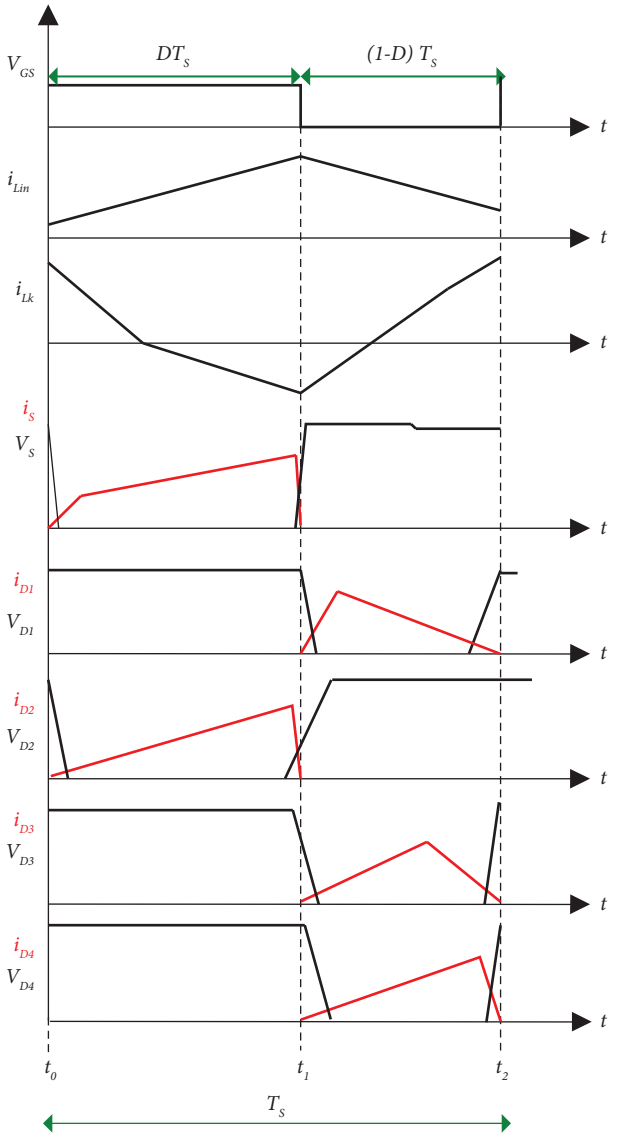


Figure 3: The key waveforms of the presented topology.

$$V_o = V_{C_4} + V_{C_5}, \tag{4}$$

$$\begin{aligned} i_{C_3} &= -i_{D_2} = i_{C_2} = i_{n_2}, \\ i_{C_5} &= i_o + i_{C_1}. \end{aligned} \tag{5}$$

2.2. Mode 2 ($t_1 < t < t_2$). At $t = t_1$, power switch S is turned OFF, and diodes D_1, D_3, and D_4 are forward biased. The equivalent circuit of mode 2 is demonstrated in Figure 4(b). Based on the figure, the voltage across input inductor L_{in} is equal to $(V_{\text{in}} - V_{C3})$. This negative voltage makes a negative slope on i_{Lin}. Additionally, the voltage over leakage and magnetizing inductances is V_{C4}/N. Thus, their currents are increased linearly. During this mode, capacitors C_3, C_4, and C_5 are charged, and capacitors C_1 and C_2 are discharged. According to the configuration of mode 2, the following equations can be expressed:

$$V_{L_{\text{in}}} = V_{\text{in}} - V_{C_3}, \tag{6}$$

$$(1 + N)V_{L_m} = V_{C_1} - V_{C_2}, \tag{7}$$

$$NV_{L_m} = V_{C_4}, \tag{8}$$

$$V_{L_m} = V_{C_1} + V_{C_3} - V_{C_5}, \tag{9}$$

$$\begin{aligned} i_{C_3} &= i_{\text{Low}} - i_{\text{High}}, \\ i_{C_3} &= i_{D_1}, \\ i_{C_2} &= i_{n_2} = -i_{D_3}. \end{aligned} \tag{10}$$

3. Steady-State Analysis

In this section, the proposed structure's voltage gain ($M = V_o/V_{\text{in}}$), voltage of capacitors, peak voltage across semiconductor components, and current of each element are calculated and presented.

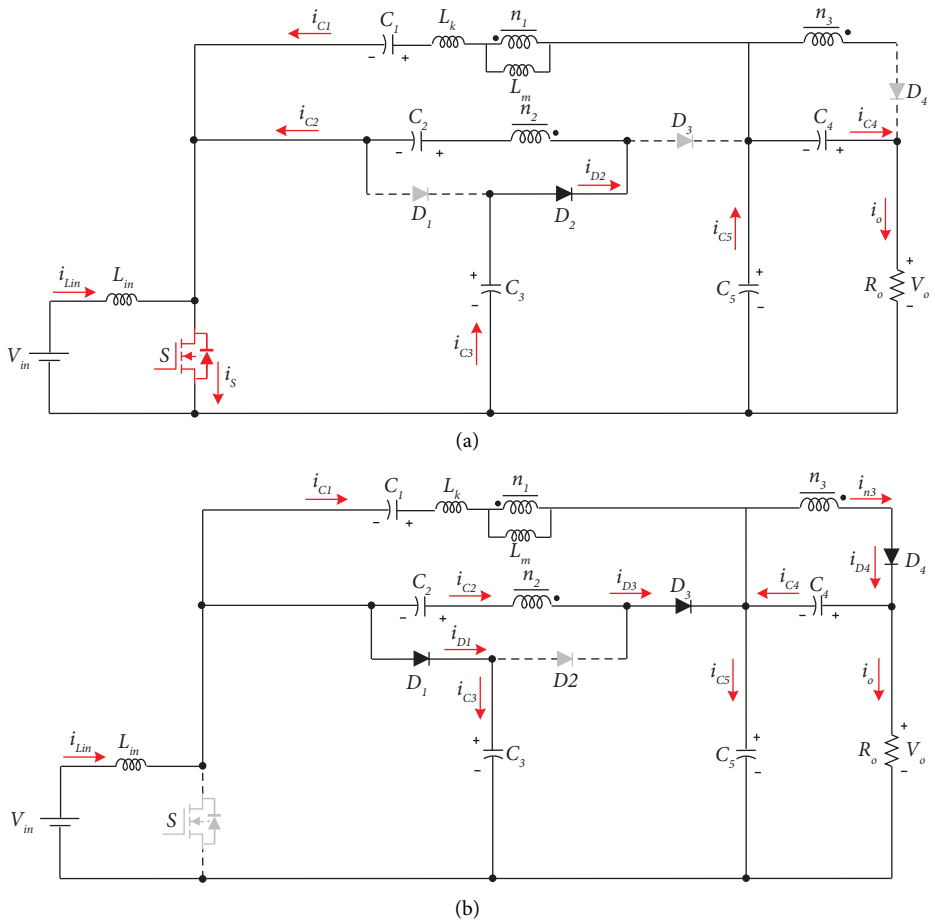


Figure 4: The equivalent circuits of operation modes. (a) Mode 1. (b) Mode 2.

3.1. Voltage Calculation. Using equations (1) and (6) and volt-second balance principle on the input inductor L_{in}, the following equation is achieved:

$$\langle V_{L_{\text{in}}} \rangle_{T_s} = 0 \longrightarrow DV_{\text{in}} + (1-D)\left(V_{\text{in}} - V_{C_3}\right) = 0. \quad (11)$$

With the simplification of equation (11), the voltage of capacitor C_3 can be expressed versus V_{in}:

$$V_{C_3} = \frac{1}{1-D} V_{\text{in}}. \quad (12)$$

Using equations (3) and (9) and volt-second balance principle on the input inductor L_m, the relation between V_{C1}, V_{C5}, and V_{in} is obtained as follows:

$$\begin{aligned} \langle V_{L_m} \rangle_{T_s} = 0 \longrightarrow & D\left(V_{C_1} - V_{C_5}\right) \\ & + (1-D)\left(V_{C_1} + V_{C_3} - V_{C_5}\right) = 0, \end{aligned} \quad (13)$$

$$V_{C_5} - V_{C_1} = V_{\text{in}}. \quad (14)$$

Replacing equation (14) in equation (3), the voltage across V_{Lm} at mode 1 can be calculated as follows:

$$V_{L_m} = -V_{\text{in}}. \quad (15)$$

Replacing equations (12) and (15) into equation (3), the voltage of capacitor C_2 is achieved as follows:

$$V_{C_2} = NV_{\text{in}} + V_{C_3} = \frac{1 + (1-D)N}{1-D} V_{\text{in}}. \quad (16)$$

Using equations (2) and (8) and volt-second balance principle on the input inductor L_m, the voltage of capacitor C_4 is obtained as follows:

$$\langle V_{L_m} \rangle_{T_s} = 0 \longrightarrow \frac{D}{N}\left(V_{C_2} - V_{C_3}\right) + \frac{(1-D)}{N} V_{C_4} = 0, \quad (17)$$

$$V_{C_4} = \frac{ND}{1-D} V_{\text{in}}. \quad (18)$$

Replacing equation (18) into equation (8), the voltage across V_{Lm} at mode 2 can be determined as follows:

$$V_{L_m} = \frac{1}{N} V_{C_4} = \frac{D}{1-D} V_{\text{in}}. \quad (19)$$

Replacing equations (16) and (19) into (7), the voltage of capacitor C_1 is achieved as follows:

$$V_{C_1} = \frac{1 + N + D}{1-D} V_{\text{in}}. \quad (20)$$

Using equations (15), (20), and (3), the voltage across capacitor C_5 can be written as follows:

$$V_{C_5} = \frac{2+N}{1-D} V_{\text{in}}. \tag{21}$$

Finally, replacing equations (18) and (21) into (4), the voltage gain (output voltage versus input voltage) is calculated as follows:

$$V_o = V_{C_4} + V_{C_5} = \frac{(1+D)N+2}{1-D} V_{\text{in}} \longrightarrow M = \frac{V_o}{V_{\text{in}}} = \frac{(1+D)N+2}{1-D}. \tag{22}$$

Figure 5 depicts the variation of the voltage gain (M) versus N and D.

Using equations (12)–(21), the maximum blocking voltage of diodes D_1, D_3, and D_4 is calculated based on Figure 4(a), as follows:

$$\begin{aligned} V_{D_1} &= V_{C_3} = \frac{1}{1-D} V_{\text{in}}, \\ V_{D_3} &= V_{C_5} - V_{C_3} = \frac{1+N}{1-D} V_{\text{in}}, \\ V_{D_4} &= V_{C_4} + NV_{\text{in}} = \frac{N}{1-D} V_{\text{in}}. \end{aligned} \tag{23}$$

Also, the maximum blocking voltage of power switch S and diode D_2 can be obtained at the second operation mode as follows:

$$\begin{aligned} V_S &= V_{D_1} = V_{C_3} = \frac{1}{1-D} V_{\text{in}}, \\ V_{D_2} &= V_{D_3} = V_{C_5} - V_{C_3} = \frac{1+N}{1-D} V_{\text{in}}. \end{aligned} \tag{24}$$

The normalized maximum voltage stresses across semiconductors are summarized as follows:

$$\begin{cases} \dfrac{V_{D_1}}{V_o} = \dfrac{V_S}{V_o} = \dfrac{1}{2+N(1+D)}, \\ \dfrac{V_{D_2}}{V_o} = \dfrac{V_{D_3}}{V_o} = \dfrac{1+N}{2+N(1+D)}, \\ \dfrac{V_{D_4}}{V_o} = \dfrac{N}{2+N(1+D)}. \end{cases} \tag{25}$$

The normalized maximum voltage stresses across semiconductors versus diverse values of N and D are shown in Figure 6.

3.2. Currents Calculation. The input average current is obtained versus I_o as follows:

$$I_{L_{\text{in}}} = I_{\text{in}} = \frac{2+N(1+D)}{1-D} I_o. \tag{26}$$

Based on the proposed converter's configuration, diodes average currents are equal to I_o.

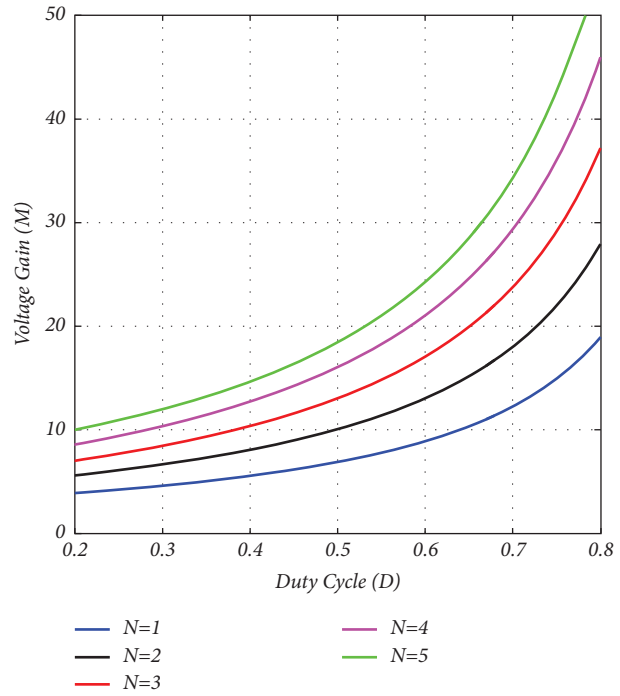


Figure 5: Voltage gains versus coupled inductor's turns ratio (N) and power switch's duty cycle (D).

$$I_{D_1}^{\text{avg}} = I_{D_2}^{\text{avg}} = I_{D_3}^{\text{avg}} = I_{D_4}^{\text{avg}} = I_o. \tag{27}$$

Using equations (26) and (27), the power switch's average current can be calculated as follows:

$$I_S^{\text{avg}} = I_{L_{\text{in}}} - I_{D_1}^{\text{avg}} = \frac{(1+D)(1+N)}{1-D} I_o. \tag{28}$$

Using average currents, the peak currents of diodes are archived as follows:

$$i_{D_1}^{\text{Peak}} = \frac{1}{1-D} I_o, \tag{29}$$

$$i_{D_2}^{\text{Peak}} = \frac{2}{D} I_o, \tag{30}$$

$$i_{D_3}^{\text{Peak}} = i_{D_4}^{\text{Peak}} = \frac{2}{1-D} I_o. \tag{31}$$

The input inductor's peak current can be expressed versus average current and current ripple as follows:

$$i_{L_{\text{in}}}^{\text{Peak}} = I_{L_{\text{in}}} + \frac{DT_s V_{\text{in}}}{2L_{\text{in}}} = \frac{2+N(1+D)}{1-D} I_o + \frac{DT_s V_{\text{in}}}{2L_{\text{in}}}. \tag{32}$$

The current of capacitor C_1 at mode 1 and 2 is obtained as follows:

$$\begin{aligned} i_{C_1}^{\text{mode-1}} &= \frac{2N}{D} I_o + \frac{DT_s V_{\text{in}}}{2L_m}, \\ i_{C_1}^{\text{mode-2}} &= \frac{-2N}{1-D} I_o - \frac{D^2 T_s V_{\text{in}}}{2(1-D)L_m}. \end{aligned} \tag{33}$$

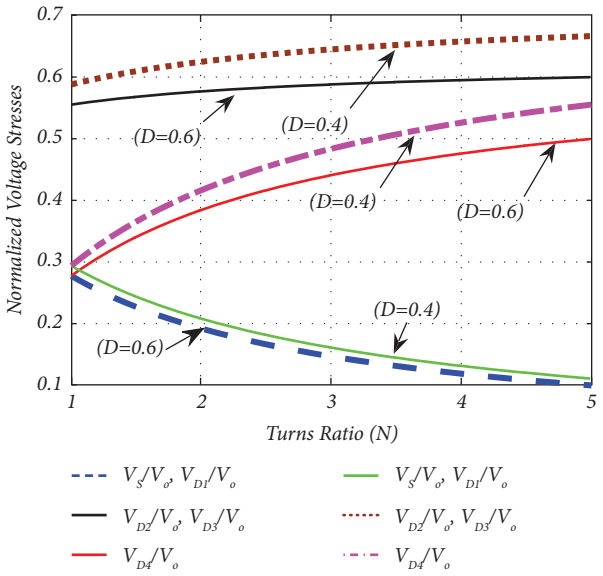


FIGURE 6: Normalized voltage stresses versus turns ratio (N) duty cycle (D).

Based on configuration of mode 1, the power switch's peak current can be written as follows:

$$i_S^{\text{Peak}} = i_{L_{\text{in}}}^{\text{Peak}} + i_{D_2}^{\text{Peak}} + i_{C_1}^{\text{mod}\,e-1},$$
$$= \left(\frac{2+N(1+D)}{1-D} + \frac{2(1+N)}{D}\right) I_o + \frac{DT_s V_{\text{in}}(L_{\text{in}} L_m)}{2(L_{\text{in}} + L_m)}. \tag{34}$$

Finally, the current of C_2, C_3, C_4, and C_5 are calculated as follows:

$$i_{C_2}^{\text{mod}\,e-1} = i_{D_2}^{\text{Peak}} = \frac{2}{D} I_o, \tag{35}$$

$$i_{C_2}^{\text{mod}\,e-2} = \frac{-2}{1-D} I_o, \tag{36}$$

$$i_{C_3}^{\text{mod}\,e-1} = i_{D_1}^{\text{Peak}} = \frac{1}{1-D} I_o, \tag{37}$$

$$i_{C_3}^{\text{mod}\,e-2} = \frac{-1}{D} I_o, \tag{38}$$

$$i_{C_4}^{\text{mod}\,e-1} = i_{C_5}^{\text{mod}\,e-1} = -I_o, \tag{39}$$

$$i_{C_4}^{\text{mod}\,e-2} = i_{C_5}^{\text{mod}\,e-2} = \frac{D}{1-D} I_o. \tag{40}$$

4. Design Considerations

This section presents the design procedure of inductors and capacitors.

4.1. Inductors. To obtain continuous conduction operation, the current ripples of input and magnetizing inductors are considered as $\Delta i_L \le 2I_L^{\text{avg}}$. Minimum values of L_{in} and L_m are determined as follows:

$$L_{\text{in}} \ge \frac{DV_{L_{\text{in}}}}{2f_s I_{L_{in}}} = \frac{DV_{in}}{2f_s M I_o}, \tag{41}$$

$$L_m \ge \frac{DV_{L_m}}{2f_s I_{L_m}} = \frac{DV_{\text{in}}}{2f_s (1-D)\Delta i_{L_m}}. \tag{42}$$

In equation (42), Δi_{L_m} is the magnetizing inductance's current ripple, which can be determined using the following equation:

$$\Delta i_{L_m} = \Delta i_{L_m}^{\text{mod}\,e-1} = \left|\Delta i_{L_m}^{\text{mod}\,e-2}\right| = I_{L_m}^{\max} - I_{L_m}^{\min}. \tag{43}$$

Using the current of capacitor C_1 in modes 1 and 2, the minimum ($I_{L_m}^{\min}$) and maximum ($I_{L_m}^{\max}$) currents of L_m are achieved as follows:

$$I_{L_m}^{\min} = -i_{C_1}^{\text{mod}\,e-1} = \frac{-2N}{D} I_o - \frac{DT_s V_{\text{in}}}{2L_m},$$
$$I_{L_m}^{\max} = -i_{C_1}^{\text{mod}\,e-2} = \frac{2N}{1-D} I_o + \frac{D^2 T_s V_{\text{in}}}{2(1-D)L_m}. \tag{44}$$

Additionally, using equation (22), turns ratio of the coupled inductor can be calculated versus input voltage, output voltage, and power switch's duty cycle:

$$N = \frac{V_0/V_{\text{in}}(1-D) - 2}{1+D}. \tag{45}$$

The magnetizing inductance maximum current is used for designing of the coupled inductor. As a result, the magnetizing inductance must be specified as equation (42). The magnetizing inductance maximum and RMS current can be written as follows:

$$I_{Lm}^{\text{Max}} = I_{Lm}^{\text{avg}} + \Delta i_{Lm}, \tag{46}$$

$$I_n^{\text{RMS}} = \sqrt{D\left(\frac{2N}{D} I_o + \frac{DT_s V_{in}}{2L_m}\right)^2 + (1-D)\left(\frac{-2N}{1-D} I_o - \frac{D^2 T_s V_{in}}{2(1-D)L_m}\right)^2}. \tag{47}$$

In the next step, using equation (7), the core size can be calculated using the following relation:

$$k_{\text{core}} \ge \frac{\rho L_m I_n^{\text{RMS}} \left(I_{Lm}^{\text{Max}}\right)^2 \times 10^8}{\left(B_{\text{Max}}\right)^2 P_{\text{core}} k_u}. \tag{48}$$

The primary side number of winding turns in the coupled inductor is obtained using the following equation:

$$n_1 = \frac{L_m I_{Lm}^{\text{Max}} \times 10^4}{B_{\text{Max}} A_{\text{core}}}. \tag{49}$$

Then, the percentage of window area allotted to each winding is determined as follows:

$$e_1 = \frac{n_1 I_{n1}}{I_{n1}^{\text{RMS}}}, e_2 = \frac{n_2 I_{n2}}{I_{n2}^{\text{RMS}}}, \text{and } e_3 = \frac{n_3 I_{n3}}{I_{n3}^{\text{RMS}}}. \tag{50}$$

Also, the wire size can be obtained using the following equation:

$$a_{w1} = \frac{e_1 k_{\text{core}} W_a}{n_1}, a_{w2} = \frac{e_2 k_{\text{core}} W_a}{n_2}, \text{and } a_{w3} = \frac{e_3 k_{\text{core}} W_a}{n_3}. \tag{51}$$

In the experimental prototype, an EE55 Ferrite Core is used. The magnetizing inductance is selected at 300 μH, and for this value, the number of windings in obtained as $n_1 = n_2 = n_3 = 34$. Using equation (52), if $L_m = 300\,\mu$H and coupling coefficient is considered 0.98, the value of leakage inductance is obtained which is almost $6\,\mu$H.

$$k = \frac{L_m}{L_m + L_k}. \tag{52}$$

4.2. Capacitors. In order to minimize the voltage ripple across capacitors, the following equation is assumed:

$$\Delta V_C \le 0.02 V_C. \tag{53}$$

Therefore, the minimum values of C_1~C_5 can be calculated as follows:

$$C_j \ge \frac{Di_{C_j}}{0.02 f_s V_{C_j}}, j = 1, 2, 3, 4, 5. \tag{54}$$

5. Efficiency Analysis

The total power losses of the proposed converter can be calculated using the following equation [13]:

$$\text{Power}_{\text{Losses}} = \text{Loss}_{\text{Switch}} + \text{Loss}_{\text{Diodes}} + \text{Loss}_{\text{Capacitors}} + \text{Loss}_{\text{Magnetics}}. \tag{55}$$

In equation (55), $\text{Loss}_{\text{Switch}}$ is the power switch's power losses and presented in the following equation:

$$\begin{aligned} \text{Loss}_{\text{Switch}} &= \text{Loss}_{\text{Conduction}} + \text{Loss}_{\text{Switching}}, \\ &= R_{DS\_on}\left(I_S^{\text{RMS}}\right)^2 + \frac{1}{2} f_s \left(t_R + t_f\right) I_S^{\text{avg}} V_S. \end{aligned} \tag{56}$$

In equation (56), t_R and t_f are the rise and fall time which are the characteristics of the power-electronics switch. $\text{Loss}_{\text{Diodes}}$ presents the total loss of diodes, which includes conduction and forward losses as follows:

$$\begin{aligned} \text{Loss}_{\text{Diode s}} &= \sum_{i=1}^{\text{Num.diodes}} \left(\text{Loss}_{\text{Conduction}} + \text{Loss}_{\text{Forward}}\right) \\ &= \sum_{i=1}^{\text{Num.diodes}} \left[r_{D_i} \left(I_{D_i}^{\text{RMS}}\right)^2 + V_{D_i} I_{D_i}^{\text{avg}} \right]. \end{aligned} \tag{57}$$

$\text{Loss}_{\text{Capacitors}}$ and $\text{Loss}_{\text{Magnetics}}$ are the power losses of the capacitors and the magnetic components which can be obtained as follows:

$$\text{Loss}_{\text{Capacitors}} = \sum_{i=1}^{\text{Num.capacitors}} \left[r_{C_i} \left(I_{C_i}^{RMS}\right)^2 \right], \tag{58}$$

$$\begin{aligned} \text{Loss}_{\text{Magnetics}} &= \text{Loss}_{\text{L}_{\text{in}}} + \text{Loss}_{\text{CL}}. \\ &= r_{L_{\text{in}}} \left(I_{L_{\text{in}}}^{\text{RMS}}\right)^2 + \sum_{i=1}^{\text{Num.windings}} \left[r_{L_{n-i}} \left(I_{L_{n-i}}^{\text{RMS}}\right)^2 \right]. \end{aligned} \tag{59}$$

In equations (57)–(59), the RMS currents are required. RMS currents are calculated and summarized as follows:

$$I_{D_1}^{\text{RMS}} = \frac{1}{\sqrt{1-D}} I_o, \tag{60}$$

$$I_{D_2}^{\text{RMS}} = \frac{2}{\sqrt{D}} I_o, \tag{61}$$

$$I_{D_3}^{\text{RMS}} = I_{D_4}^{\text{RMS}} = \frac{2}{\sqrt{1-D}} I_o, \tag{62}$$

$$I_S^{\mathrm{RMS}} = \sqrt{D\left(\left(\frac{2+N(1+D)}{1-D}+\frac{2(1+N)}{D}\right)I_o+\frac{DT_sV_{\mathrm{in}}\left(L_{\mathrm{in}}L_m\right)}{2\left(L_{\mathrm{in}}+L_m\right)}\right)^2}, \tag{63}$$

$$\begin{aligned} I_{C_1}^{\mathrm{RMS}} &= I_{n_1}^{\mathrm{RMS}}, \\ &= \sqrt{D\left(\frac{2N}{D}I_o+\frac{DT_sV_{\mathrm{in}}}{2L_m}\right)^2+(1-D)\left(\frac{-2N}{1-D}I_o-\frac{D^2T_sV_{\mathrm{in}}}{2(1-D)L_m}\right)^2}, \end{aligned} \tag{64}$$

$$I_{C_2}^{\mathrm{RMS}} = I_{n_2}^{\mathrm{RMS}} = 2I_o\sqrt{\frac{1}{D(1-D)}}, \tag{65}$$

$$I_{C_3}^{\mathrm{RMS}} = I_o\sqrt{\frac{1}{D(1-D)}}, \tag{66}$$

$$I_{C_4}^{\mathrm{RMS}} = I_{C_5}^{\mathrm{RMS}} = I_o\sqrt{\frac{D}{1-D}}, \tag{67}$$

$$I_{n_3}^{\mathrm{RMS}} = I_o\sqrt{\frac{1}{1-D}}. \tag{68}$$

6. Comparison Study

This part presents a comparison among the presented high voltage topology and other similar coupled inductor-based topologies ([1, 3, 5, 7, 9, 10, 12, 25–30]). For this purpose, the number of used components, including the number of switches, diodes, capacitors, and magnetic devices (inductors and coupled inductors), voltage gain, normalized maximum peak voltage over semiconductors, and input current ripple are taken into account. Based on Table 1, topologies in [3, 30] have a lower components count. In [30], only one magnetic core was used. However, this topology suffers from high peak voltage across diodes, and the maximum voltage stress of [30] is equal to the output voltage. In [26, 29], two power switches were used, which is more than that of the others. Comparison of voltage gains is shown in Figure 7(a). In the figure, the coupled inductor turns ratio is assumed to be equal to 1.

The proposed converter and topology of [7] present higher voltage gain than other structures. However, for $D > 0.55$, the suggested converter has high voltage gain than that of [7]. Also, the topology in [7] suffered from high input current ripple, while the proposed topology has an input current with low ripple, which is suitable for renewable energy sources. The comparison results of voltage stress across switches and diodes are shown in Figures 7(b) and 7(c). For $N = 1$, the presented topology has lower voltage over switch than other introduced converters. For $N > 1.5$, the peak voltage across switches of [29] was lower than that of the proposed converter. However, it is clear that, for higher values of the turns ratio, the power loss is increased. According to Figure 7(c), in the converters presented in [1, 5, 10], and [25] the peak voltage on the diodes is lower than that of the suggested topology. However, these converters obtain low voltage gain with high peak voltage on switches. Therefore, considering the comparison results, it can be deduced that the proposed converter has a high voltage conversion ratio with low voltage stresses across semiconductors. Additionally, this high voltage gain is obtained with reasonable components count and low input ripple. The low input current is an important characteristic in DC-DC converters especially in those applied in renewable energy systems. However, some high gain converters present higher input current ripples [31, 32].

7. Experimental Results

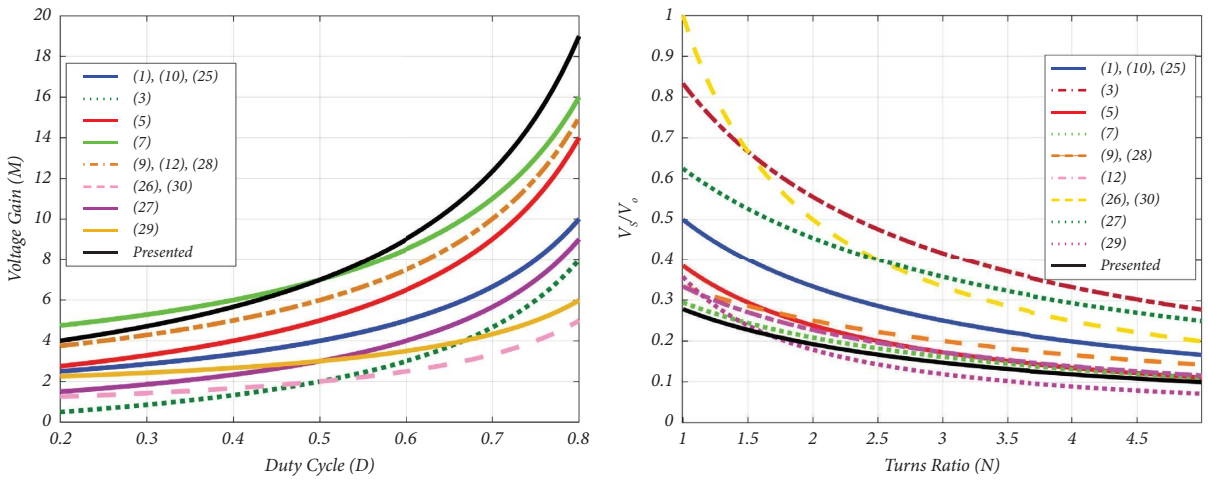
This section presents the experimental results of the proposed converter. For this work, a 580 W, 46 V to 400 V prototype is built and tested. The photo of the experimental prototype is shown in Figure 8. Specifications of this prototype are given in Table 2. Based on the table, the switching frequency is equal to 25 kHz. It should be mentioned that another prototype with the power rating of 1 kW and the switching frequency of 50 Hz has been implemented and tested and its experimental results are also included.

The voltage across capacitors C_1~C_5 are shown in Figures 9(a)–9(d). According to Figure 9(a), the voltage over capacitor C_1 is measured 284 V. This result can verify equation (20). The voltage across C_2 and C_3 is obtained as 148 V and 114 V, respectively. Thus, equations (12) and (16) are proved. Voltage waveforms of capacitors C_4 and C_5 are depicted in Figure 9(d). Using these results, equations (18) and (21) can be verified.

The voltage waveforms of diodes D_1~D_4 and power switch S are demonstrated in Figures 10(a)–10(d). Based on

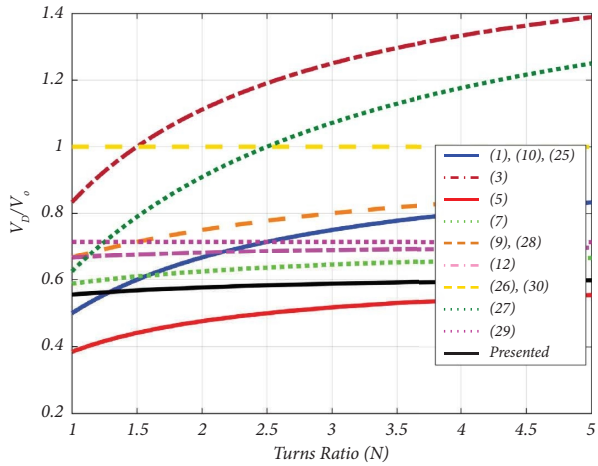
Table 1: Comparison results.

Topologies	Number of elements				Total number of elements	Voltage gain	Max. volt. stress on switches	Max. volt. stress on diodes	Input ripple
	S	D	C	Magnetics					
[1]	1	3	4	L: 1 CL: 1	10	$(1+N)/(1-D)$	$1/(1+N)$	$N/(1+N)$	Low
[3]	1	2	3	L: 1 CL: 1	8	$[D(1+N)]/(1-D)$	$1/[(1+N)D]$	$N/[(1+N)D]$	Low
[5]	1	4	5	L: 1 CL: 1	12	$[1+N(1+D)]/(1-D)$	$1/[1+N(1+D)]$	N/[1 + N(1 + D)]	Low
[7]	1	4	4	L: 0 CL: 1	10	[2+(2 − D)N]/(1 − D)	1/[2+(2 − D)N]	$(N+1)/[2+(2-D)N]$	High
[9]	1	3	4	L: 1 CL: 1	10	$(2+N)/(1-D)$	$1/(2+N)$	$(1+N)/(2+N)$	Low
[10]	1	3	4	L: 1 CL: 1	10	$(1+N)/(1-D)$	$1/(1+N)$	$N/(1+N)$	Low
[12]	1	4	5	L: 1 CL: 1	12	$[N(2-D)+(1+D)]/(1-D)$	1/[N(2-D)+(1+D)]	(1+N)/[N(2-D)+(1+D)]	Low
[25]	1	3	4	L: 1 CL: 1	10	$(1+N)/(1-D)$	$1/(1+N)$	$N/(1+N)$	Low
[26]	2	2	3	L: 1 CL: 1	9	$N/(1-D)$	$1/N$	1	Low
[27]	1	4	3	L: 1 CL: 1	10	$(DN+1)/(1-D)$	$1/(DN+1)$	$N/(DN+1)$	High
[28]	1	3	4	L: 1 CL: 1	10	$(2+N)/(1-D)$	$1/(2+N)$	$(1+N)/(2+N)$	Low
[29]	2	5	3	L: 0 CL: 1	11	$[(2-D)N]/(1-D)$	$1/[(2-D)2N]$	$1/(2-D)$	High
[30]	1	2	2	L: 0 CL: 1	6	$N/(1-D)$	$1/N$	1	Low
Presented	1	4	5	L: 1 CL: 1	12	$[2+N(1+D)]/(1-D)$	$1/[2+N(1+D)]$	$(N+1)/[2+N(1+D)]$	Low



(a) (b)

Figure 7: Continued.



(c)

Figure 7: Comparison results. (a) The voltage gain (M) versus the duty cycle (D), (b) V_S/V_o, and (c) V_D/V_o.

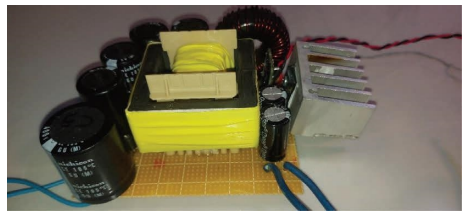


Figure 8: The experimental prototype.

Table 2: Specifications of the experimental prototype

Parameters and components	Value
V_o	400 V
P_o	580 W
V_{in}	46 V
f_s	25 kHz
L_{in}	300 μH
C_1	220 μF/350 V
C_2	220 μF/200 V
C_3	220 μF/200 V
C_4	220 μF/100 V
C_5	470 μF/450 V
Switch S	IRF 260
D_1	MUR 1560
D_2	MUR 1560
D_3	MUR 1560
D_4	MUR 1560
Coupled inductor	Ferrite core EE55 $L_m = 300\,\mu$H $L_k = 3\,\mu$H Turns ratio $(N) = 1$
Duty cycle	0.6

the figures, the peak voltage across D_1~D_4 is measured equal to 115 V, 230 V, 230 V, and 115 V, respectively. Also, the maximum V_s is about 125 V. Therefore, the presented equations in (25) are verified. A comparison of theoretical and experimental results of the capacitors and semiconductors voltage is presented in Table 3.

The current waveforms of the input inductor and coupled inductor are depicted in Figures 11(a) and 11(b), respectively. As can be seen in Figure 11(a), the proposed converter has a low input current ripple, which is suitable for renewable energy applications.

To regulate the output voltage versus disturbance in input voltage, a closed-loop system is designed, as shown in Figure 12. The open-loop and closed-loop output voltage of the suggested converter is measured and shown in Figures 13(a) and 13(b). At the rated power (580 W), output voltage and current are measured as 400 V and 1.45 A, respectively. For closed-loop output voltage regulation, a PI controller is adjusted as $k(1 + sT)/(sT)$, where $k = 0.001$ and $T = 0.022$. Based on Figure 13(b), when the input voltage is changed, the output voltage is regulated at 400 V with minimum oscillation.

In order to show the ability of the proposed converter for operating in high switching frequency (50 kHZ) and high power level (1 kW), the experimental results provided in these conditions are shown in Figure 14. The voltage across the switch is shown in Figure 14(a) which indicates that its maximum off-state voltage is 145 V. The output voltage and current are shown in Figure 14(b). The average value of the output voltage is about 390 V and the average output current is about 2.40 A resulting in output power of 936 W.

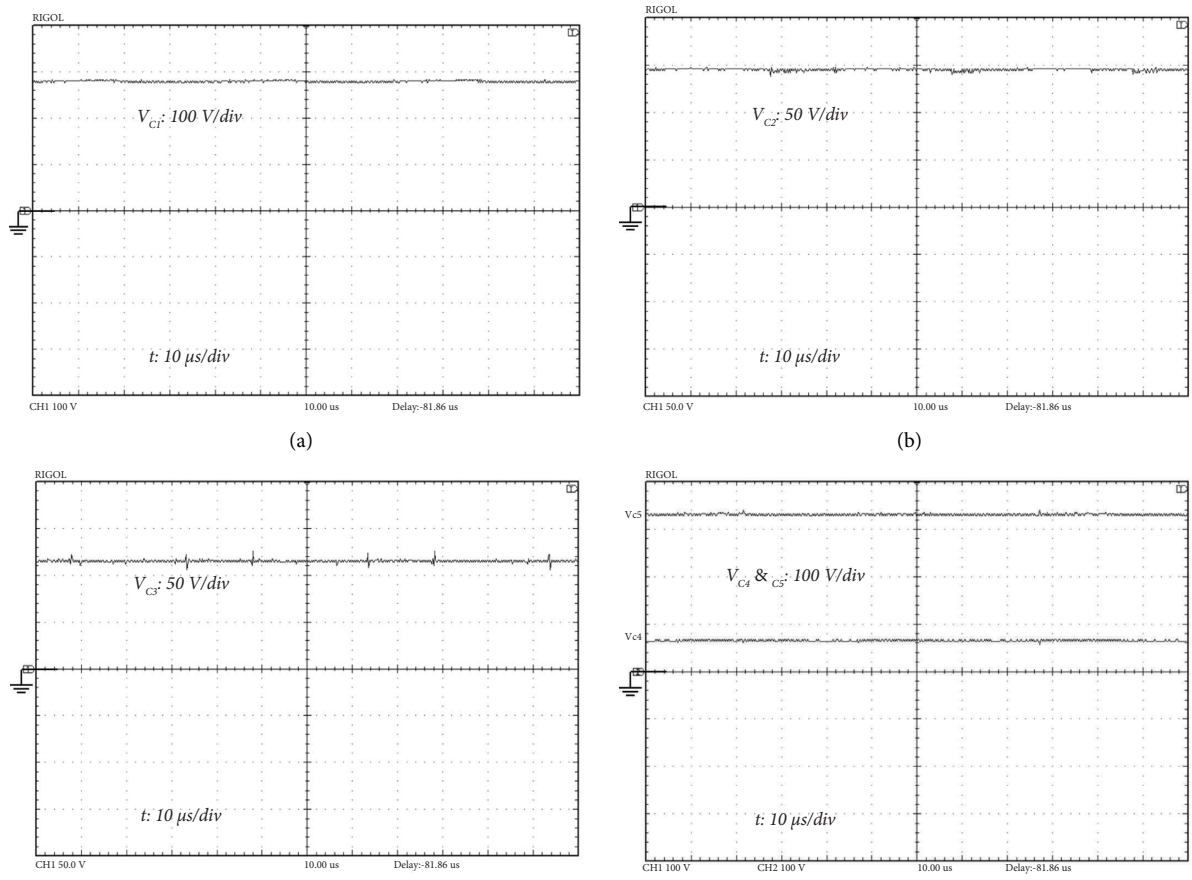


Figure 9: Experimental results for the voltage on the capacitors. (a) V_{C1}, (b) V_{C2}, (c) V_{C3}, (d) V_{C4}, and V_{C5}.

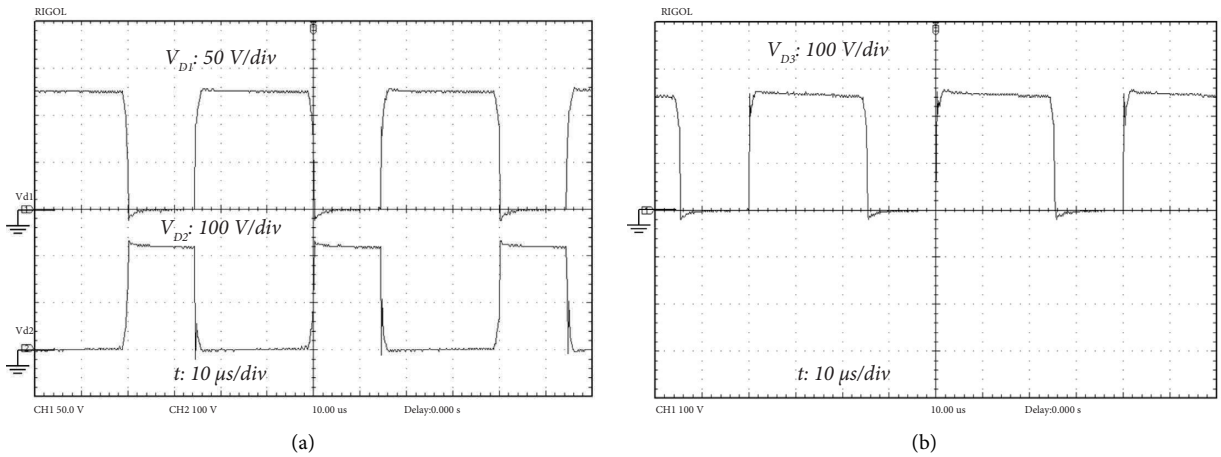
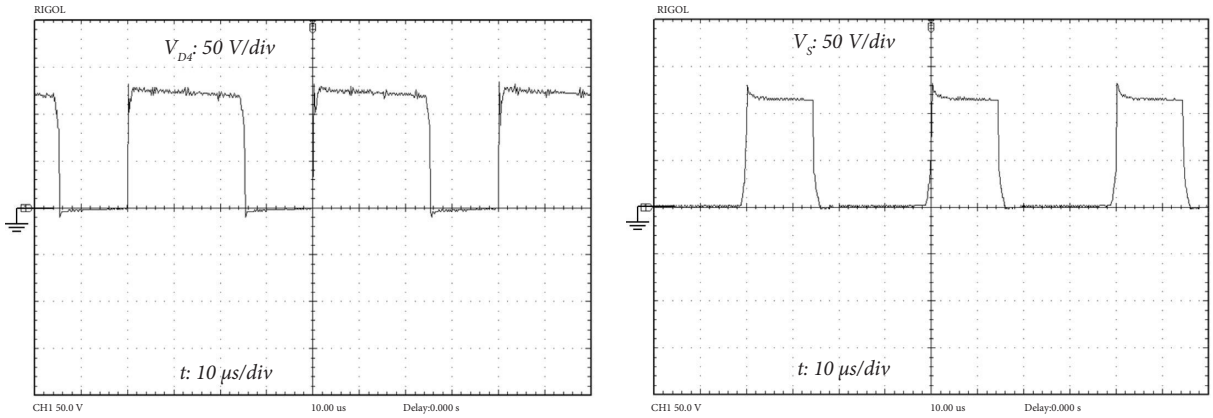


Figure 10: Continued.

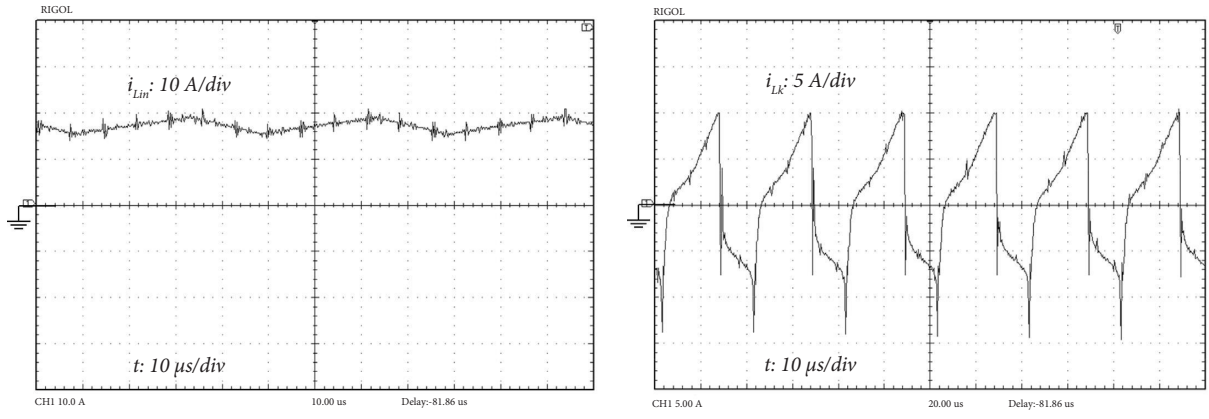


(c) (d)

Figure 10: Experimental results for the voltage on the semiconductor devices. (a) V_{D1} and V_{D2}, (b) V_{D3}, (c) V_{D4}, and (d) V_S.

Table 3: Comparison between experimental and theoretical results.

Parameters	Experimental (V)	Theoretical (V)
V_{C1}	284	299
V_{C2}	148	161
V_{C3}	114	115
V_{C4}	64	69
V_{C5}	336	345
V_{D1}	110	115
V_{D2}	225	230
V_{D3}	220	230
V_{D4}	110	115
V_S	110	115
V_o	400	414



(a) (b)

Figure 11: Experimental result of (a) input current and (b) coupled inductor's current.

The measured efficiency versus output power (P_o) and loss distribution are depicted in Figures 15(a) and 15(b), respectively. It should be noticed that efficiency is measured for a wide range of output power (50~ 580 W). The maximum efficiency is measured at $P_o = 400$ W, which is equal to 96.11%. Also, at the rated power, efficiency is obtained as

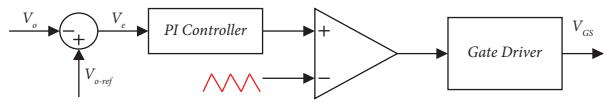
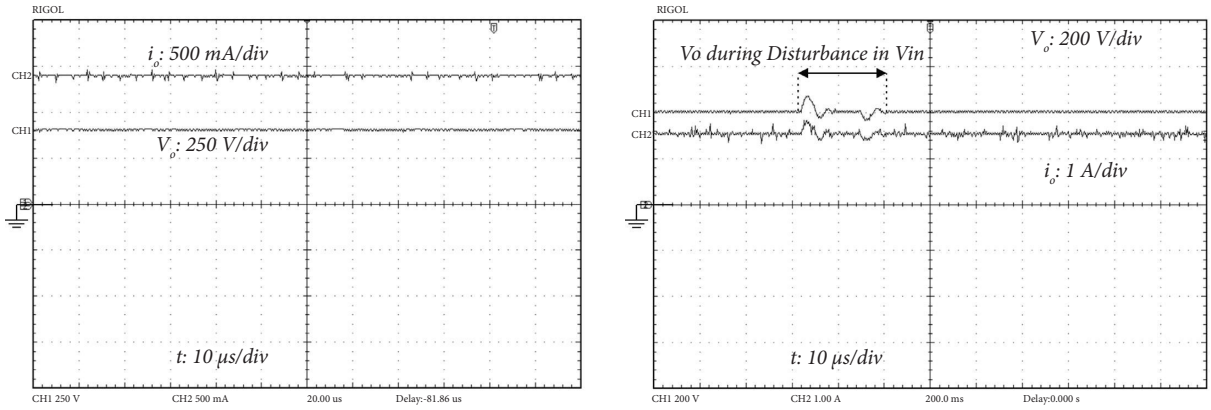
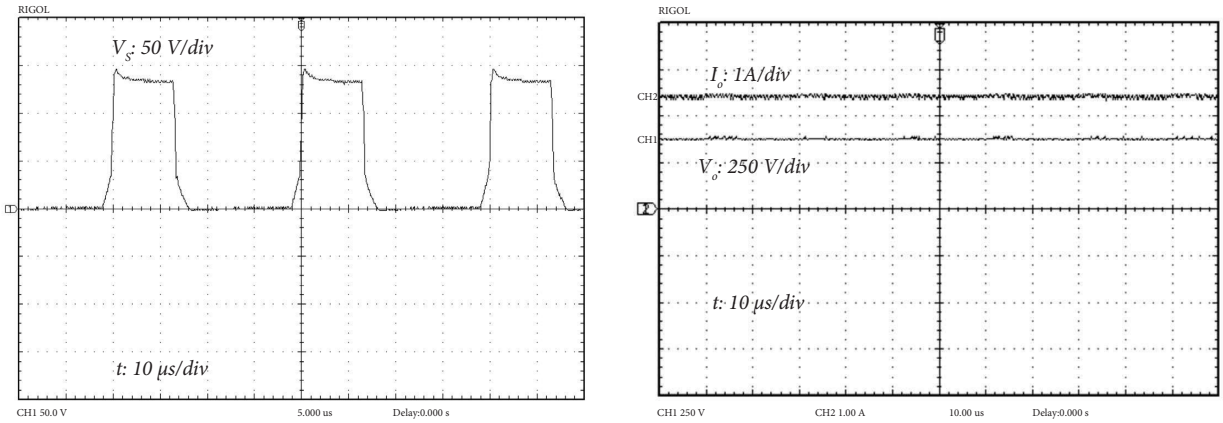


Figure 12: Closed-loop regulation of the output voltage.



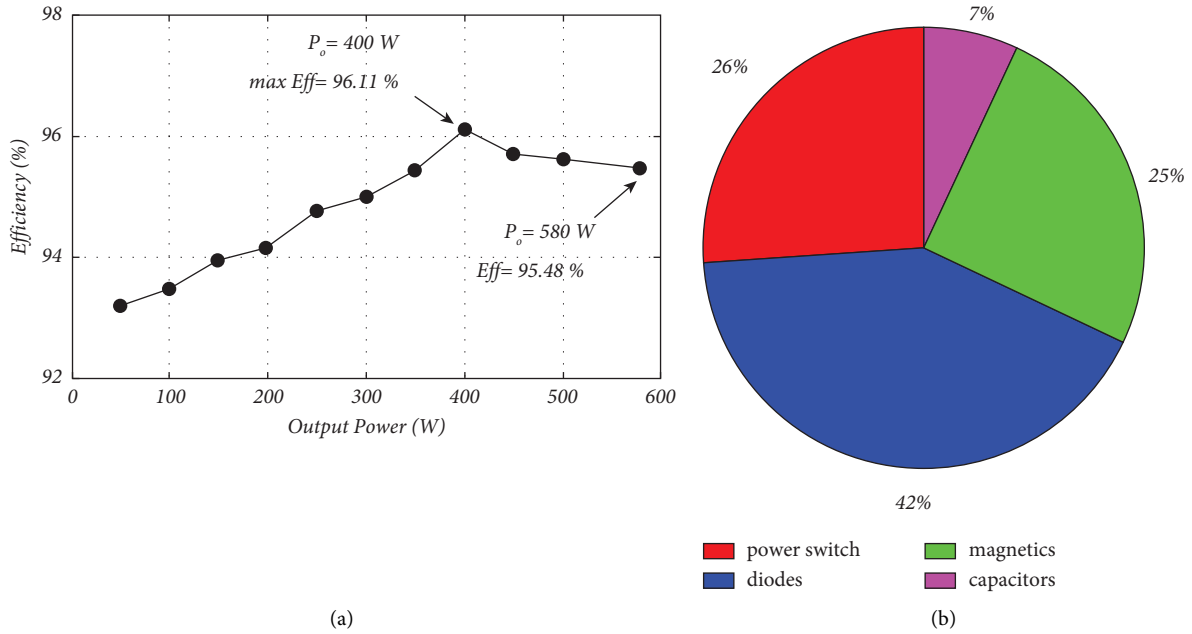
(a) (b)

Figure 13: Experimental waveform of V_o. (a) Open-loop. (b) Closed-loop.



(a) (b)

Figure 14: Experimental waveforms in $f_s = 50\,\text{kHz}$ and $P_o = 1\,\text{kW}$. (a) V_s and (b) V_o and I_o.



(a) (b)

Figure 15: Experimental efficiency. (a) Efficiency curve. (b) Loss distribution.

95.48%. The minimum efficiency is measured at 50 W, which is 93.11%. Therefore, $P_o = 50\sim580$ W, and the efficiency is obtained between 93 and %96.2.

8. Conclusion

This article proposed a topology of nonisolated high step-up DC-DC converter with high voltage conversion ratio for renewable usages such as PV power systems. The suggested topology is designed based on three coupled inductors and VMC technique. The major benefits of the proposed topology are continuous input current with low ripple, low voltage stress across semiconductors, common ground between input and output ports, high voltage gain, low volume and cost, and high efficiency. To obtain a high output voltage, the windings of the coupled inductor are combined with VMC, which leads to a higher output voltage with lower duty cycle. Therefore, the conduction power losses of the power-electronic switch are decreased. A 580 W, 400 V, 25 kHz and another 1 kW, 400 V, 50 kHz prototypes are built, and the experimental results are presented to indicate the validity of mathematical analysis and effectiveness of the suggested structure. The experimental results indicated that the high voltage gain is achieved with low power losses while maintaining the continuous input current and low voltage stress on the active switch.

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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