A Nonlinear Dynamic S/H-ADC Device Model Based on a Modified Volterra Series: Identification Procedure and Commercial CAD Tool Implementation

Pier Andrea Traverso, Domenico Mirri, *Member, IEEE*, Gaetano Pasini, *Member, IEEE*, and Fabio Filicori, *Member, IEEE*

***Abstract*—A nonlinear, dynamic empirical model, based on a Volterra-like approach, was previously proposed by the authors for the time-oriented characterization of sample/hold (S/H) and analog-to-digital conversion (ADC) devices. In this paper, the experimental procedure for model parameter measurement is presented, as well as techniques devoted to the implementation of the model in the framework of the main commercial CAD tools for circuit analysis and design. Examples of simulations, performed both in the time and frequency domain on the model obtained for a commercial device, are proposed, which show the model's capability of pointing out the dynamic nonlinear effects in the S/H-ADC response.**

***Index Terms*—Analog-to-digital conversion (ADC) modeling, ADC converter, nonlinear dynamic model, nonlinear dynamic system, sample-hold (S/H), Volterra series.**

I. Introduction

THE Volterra series behavioral approach has been largely applied in recent years for the empirical "black-box" modeling of nonlinear dynamic systems. Typical examples are associated with the characterization of transformers, electromechanical transducers, weakly nonlinear electronic and communication subsystems, as well as applications in the field of hydrology, physiology, and plasma physics. Several important contributions to the identification of general-purpose techniques for the practical measurement of Volterra kernels can be found in literature [1]–[4]. However, when the nonlinear effects in the system behavior become relevant, the number of kernels, which must be taken into account in the truncation of the Volterra series in order to achieve a good accuracy of the model, quickly increases. In such conditions, model extraction from experimental data could be unreliable or even impossible, due to the complexity of the experimental procedures and mathematical methods involved in higher order kernel measurement. In addition, even when the dynamic system is characterized by weak nonlinearities (i.e., the series can be truncated to the third or fourth-order contribution), these approaches allow the estimation of kernels only over a reduced grid of points in the multidimensional frequency domain, making use to this aim of complex input test signals and/or high-order statistics. Finally, kernel measurement techniques are often based on recursive algorithms, whose results can strongly suffer from relevant errors due to experimental data uncertainty propagation.

In order to overcome such limitations, the authors previously proposed a "modified" Volterra series [5] which, besides preserving the same generality and theoretical validity of the classical approach,[1] can be practically applied also in presence of strong nonlinearities (if mild hypotheses on the duration of system memory time are satisfied) or, when the nonlinear effects are weak, associated with a simple experimental procedure based on conventional measurements and reliable algorithms. Sample/hold (S/H) and analog-to-digital conversion (ADC) device modeling represents an interesting application of the modified series, which allows characterization of not only static, but also dynamic nonlinearities. In the past, the authors proposed a nonlinear dynamic S/H-ADC model which described the input/output device behavior in the frequency-domain [6]. More recently, a time domain-oriented model has been identified [7]. Its analytical formulation allows the measurement of S/H-ADC model parameters directly in the time-domain, leading to an improvement in model predictive capabilities of system dynamic behavior.

In this paper, details about the experimental procedure for model parameter measurement will be presented. Moreover, it will be shown that the proposed model can be easily implemented in the framework of main commercial CAD tools for circuit analysis and design, by means of standard components available at the user-interface level, without the need for approximations or high-level additional packages. Examples of the techniques exploited for model implementation purposes, as well as analysis results carried out both in time and frequency-domain, which point out model prediction capabilities will complete the discussion.

II. Discrete Time Convolution S/H-ADC Model

A previously proposed [6] convenient functional description for the S/H-ADC input/output relationship is shown in Fig. 1;

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[1]It is easy to show that the modified kernels of any order can be expressed directly starting from the conventional ones (see [5] for details).

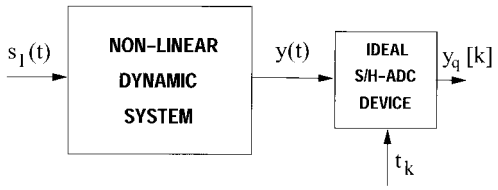

Fig. 1. S/H-ADC functional description previously proposed for the characterization of nonlinear dynamics.

the actual device with input $s_I(t)$ is modeled as an *ideal* component sampling and converting to digital the signal $y(t)$ generated at the output of a nonlinear dynamic system controlled by $s_I(t)$, which takes into account all of the nonidealities (both *static* and *dynamic*) of the S/H-ADC. The nonlinear dynamic system is then further represented as the cascade of two subblocks (Fig. 2). The first element of the cascade is a purely linear system, which describes the memory effects introduced by the input signal conditioning circuits (amplifiers, filters, etc.) and the sample-hold process. It can be identified by the conventional convolution integral of its pulse response, without any assumption on the memory time duration (i.e., the width of the integration interval). Clearly, a one-dimensional transfer function $H(f)$, corresponding to the time-domain pulse response, can be used to describe the linear block as well.

The second block in the cascade, controlled by the linear transformation result $s(t)$ and providing the ideal device input signal $y(t)$, is a nonlinear system with a memory time which can be considered not only finite, but also "short" if compared to the typical minimum period of the input signal $s_I(t)$. This hypothesis is justified by the nature of the dynamic nonlinearities, which can be considered related only to the active electron devices, usually characterized by fast dynamics. Under such conditions, the modified Volterra series approach can be applied to the second block of the cascade, taking into account only the zero-order and first-order terms of the series expansion and without introducing relevant truncation errors [5]. The two contributions can be expressed, respectively, as

$$y^{(S)}(t) = z_0[s(t)] = y_0 + \sum_{r=1}^{\infty} \frac{1}{r!} a_r s^r(t) \tag{1}$$

$$y^{(D)}(t) = \int_{-T_A}^{T_B} w\left[s(t), \tau\right] \cdot \left[s(t-\tau) - s(t)\right] d\tau \tag{2}$$

with

$$y(t) = y^{(S)}(t) + y^{(D)}(t). \tag{3}$$

The zero-order term $y^{(S)}(t)$ is an algebraic function with respect to s, which coincides with the dc characteristic $z_0[\cdot]$ of the S/H-ADC device.[2] In Fig. 2, this contribution to $y(t)$ is represented as the output of a nonlinear, memoryless subsystem (dotted line). Parameters a_r can be analytically derived from conventional Volterra kernels of corresponding order by means of the relation

$$a_r = \int \cdots \int_{-\infty}^{\infty} h_r\left(\tau_1, \tau_2, \ldots, \tau_r\right) d\tau_1 \cdots d\tau_r,\ r = 1, 2, \ldots \tag{4}$$

As far as the series first-order term $y^{(D)}(t)$ is concerned, it represents a purely dynamic contribution, where $w[s(t), \tau]$ is the first-order modified kernel, nonlinearly controlled by the signal s. It can be shown that also w can be expressed with respect to conventional Volterra kernels. By discretizing the nonlinear memory interval $[t - T_B, t + T_A]$ into the sequence of $(P_A + P_B)$ elementary subintervals of equal width $\Delta\tau$ ($P_A\Delta\tau = T_A; P_B\Delta\tau = T_B$), the purely dynamic, purely nonlinear response $y^{(D)}(t)$ in Fig. 2 can be written as

$$y^{(D)}(t) \cong \sum_{\substack{p=-P_A \\ p\neq 0}}^{P_B} \left[s(t - p\Delta\tau) - s(t)\right] \sum_{n=1}^{N} \beta_{pn} s^n(t) \tag{5}$$

where each term $w[s(t), p\Delta\tau]\Delta\tau$ in (2) has been expanded into a homogeneous polynomial series truncated to the Nth-order, β_{pn} being the coefficients of the pth expansion.

The functional description represented in Fig. 2, derived from model analytical formulation, shows the clear separation between "sources" of dynamic linear and, respectively, memoryless and purely dynamic nonlinear effects. This feature of the S/H-ADC model allows to separately measure the parameters which characterize each block, by means of quasiindependent steps performed using conventional instrumentation. Moreover, the analytic description of the three subsystems is suitable for a *direct* implementation in the framework of all those CAD tools which make available simple user-defined devices, preserving the accuracy of model predictive capabilities.

III. Model Experimental Characterization

The nonlinear dynamic S/H-ADC model described by the behavioral equations (1) and (5) was identified in a previous work [7] for a SPICE-based digital acquisition device, by means of input/output data obtained through time-domain simulations. In the present paper, the experimental procedure which was followed in order to characterize the model parameters for a commercial successive approximation 12-bit digital acquisition board is described. The 250-kS/s S/H-ADC device under test (DUT) was connected to the PCI interface of a PC station and directly controlled by means of National Instruments LabVIEW package. Since the nonlinear block of Fig. 2 with output $y^{(D)}(t)$ is purely dynamic, and it is always possible to impose, without any loss of generality, H(0) = 1 to the transfer function of the linear subsystem, the memoryless nonlinear block is characterized by a response $y^{(S)}(t)$ which coincides, at static operating conditions, with the dc characteristic of the DUT. Thus, conventional dc measurements, performed over the device operating region [−5 V, 5 V], allowed to identify the function z_0 [i.e., offset y_0 and coefficients a_r, up to the fifth-order, of its polynomial expansion (1)].

As far as the characterization of the purely linear network is concerned, it can be shown [6] that at zero-bias, small-signal operation the nonlinear dynamic block is characterized by a

[2]It is always possible to superimpose, without any loss of generality, the value H(0) = 1 to the linear block transfer function.

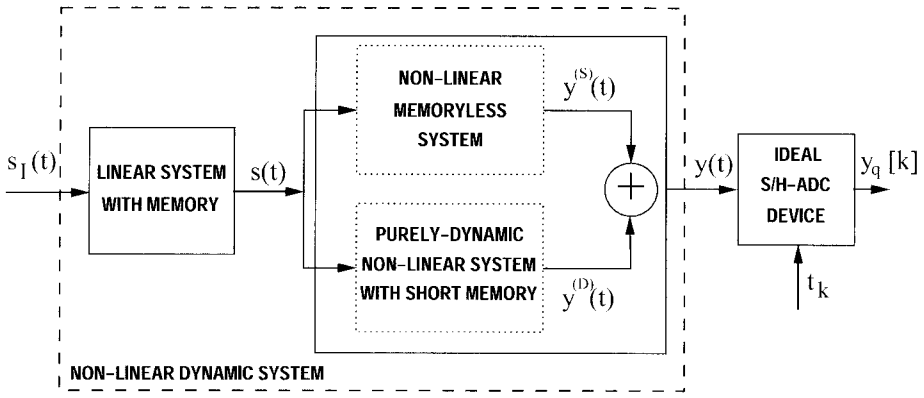

Fig. 2. S/H-ADC representation deriving from the proposed model analytical formulation.

response $y^{(D)}(t) \equiv 0$. A 80-MHz function generator, synthesizing a low-amplitude zero-offset sinusoidal signal, was then used as an input source for the DUT. Since the first derivative g_{DC_0} with respect to $s \equiv 0$ can be computed for function z_0, starting from data obtained in the previous experimental step, the transfer function $H(f)$ was characterized, at different frequency values f_i, by exploiting the expression

$$H(f_i) = \frac{Y(f_i)}{g_{\mathrm{DC}_0} \cdot S_I(f_i)} \tag{6}$$

where $Y(f)$ is the discrete transform of $y(t)$ deduced by means of the samples acquired by the DUT. $S_I(f_i)$ is instead the complex representation of the sinusoidal input signal, which was accurately characterized by a reference 5-MS/s digital acquisition board (REF in the following) sampling the same signal $s_I(t)$ applied to the input of the DUT device. The REF device was chosen in order to guarantee better overall performances than the DUT in terms of accuracy, analog bandwidth and linearity. Function $H(f)$ was measured through this procedure not only in the small-signal bandwidth of DUT declared by the manufacturer, but also at higher frequencies (up to 1 MHz), where the linear dynamics of the device introduce a relevant attenuation.

In order to measure parameters β in (5), which characterize the purely dynamic nonlinear contribution $y^{(D)}(t)$ to the output of DUT device, a third experimental step was followed. A set of R large-amplitude (0.5 V) sinusoidal test signals $s_{Ir}(t)$, for different equally-spaced bias values in the interval [−4V, 4 V] and at different frequencies f_k (from 1 kHz up to 1 MHz) were synthesized by the waveform generator and applied to the input of both DUT and REF devices, through a suitable splitting access network. The two signal paths were accurately characterized in order to measure the time delay t_0 suffered from the wave propagation along one path with respect to the other; sample time instants, corresponding to data at the output of REF device, were shifted by this delay to guarantee a ideally identical signal transmission toward the input of the two acquisition boards. In addition, DUT and REF were connected through a timing bus, controlled by a trigger generator, in order to synchronize the time axes of both S/H-ADC devices.

By sampling each input signal $s_{Ir}(t)$ in M time instants t_m, an over-determined system of $R \cdot M$ linear equations in the $(P_A + P_B)N << R \cdot M$ unknowns β_{pn} was obtained from (5) and (3) ($P_A = P_B = 3$; $\Delta\tau = 20$ ns):

$$\begin{aligned}\sum_{\substack{p=-P_A \\ p\neq 0}}^{P_B} &\left[s_r(t_m - p\Delta\tau) - s_r(t_m)\right] \sum_{n=1}^{N} \beta_{pn} s_r^n(t_m) \\ &= y_r^{(D)}(t_m) \\ &= y_r(t_m) - z_0\left[s_r(t_m)\right] \ (r = 1, \ldots, R)(m = 1, \ldots, M).\end{aligned} \tag{7}$$

Samples $y_r(t_m)$ were available directly at the output of the DUT device. Delayed signal samples $s_r(t_m - p\Delta\tau)$ were instead computed from the input Fourier transform $\tilde{S}_{Ir}(f)$ (derived through empirical data acquired by the REF device) by applying to it the linear transformation

$$H_p(f) = H(f)\exp(-j2\pi f p\Delta\tau). \tag{8}$$

Analogously, the discrete function $H(f) \cdot \tilde{S}_{Ir}(f)$ was inverted in order to obtain the samples $s_r(t_m)$ at the output of the linear block, allowing to separate the nonlinear dynamic contribution from the static response samples $z_0[s_r(t_m)]$. Thus, model parameters β_{pn} can be identified by means of well-known methods for the least-square solution of a linear system of equations. This represents an important feature of the proposed approach, since other nonlinear optimization algorithms, devoted to the fitting of empirical data, usually suffer from convergence problems due to the presence of local minima in the behavior of goal functions.

IV. Model Implementation

The S/H-ADC model analytical formulation described by (1), (3), and (5) allows to easily implement the characterized device in the framework of most common CAD packages for circuit analysis and design by means of standard user-interface tools without the need for any additional approximation or low-level code programming. In the following, practical examples showing the schematic components to be used and the techniques suggested in order to import model parameters are described for both Agilent-ADS and Orcad-PSPICE simulators.

The purely linear network, which represents the first element in the cascade of Fig. 2, was characterized by measuring values of its transfer function $H(f)$ on a set of points in the frequency-domain. Since the ADS package allows the definition of linear

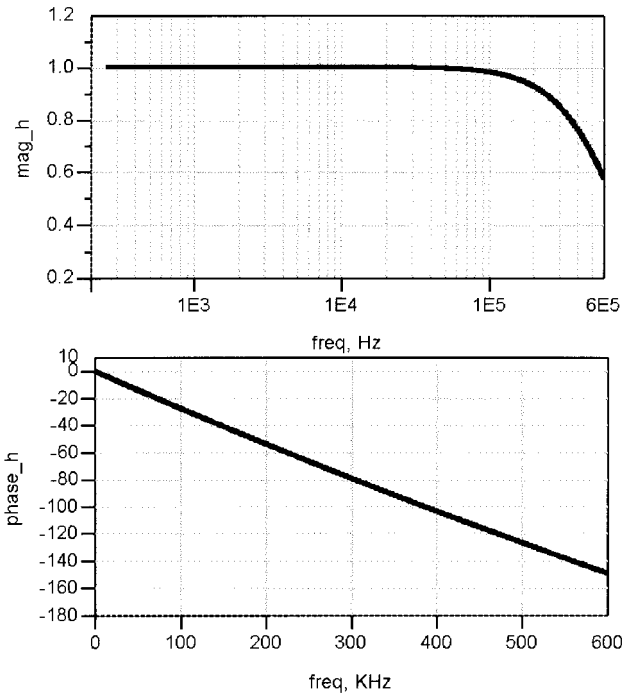

Fig. 3. Magnitude and phase of the linear network transfer function, obtained by an ac simulation in ADS environment.

blocks, based on "look-up" tables of data in the frequency-domain (in TOUCHSTONE format, for example), the implementation of the linear subsystem in this simulator is immediate. In the case of SPICE, instead, a linear block can be defined, in the frequency-domain, only by providing a polynomial expansion of its transfer function in the form $N(j\omega)/D(j\omega)$; coefficients in this expression can be obtained by means of a preliminary elaboration of the empirical data (a general-purpose mathematical tool like MATLAB can be used to this aim). Fig. 3 shows magnitude and phase of function $H(f)$, obtained by performing an ADS ac analysis on the implemented linear block.

The nonlinear blocks of Fig. 2 can be suitably implemented in a ADS schematic by means of a standard tool available at the user-interface level. More precisely, the M-port symbolically defined device (SDD) is particularly useful to the aim of implementing equation-based nonlinear blocks. In Fig. 4, a simplified representation of a two-port SDD is shown: current instantaneous values (i_1, i_2) at the ports of the device can be expressed as nonlinear functions of the applied voltages (v_1, v_2). Designer can choose to provide functions (f_1, f_2) in an analytical explicit form or just refer to an array of samples (stored into look-up tables), defined on a grid of points in their domain; the environment, in the latter case, automatically performs the correct run-time interpolation during the analysis, according to the preferred method (piecewise linear, cubic, splines, etc.). Before each current value is evaluated, the device allows a further elaboration by applying to the spectrum of $i_k(t)$ a *weighting function* $H_k(f)$ defined in the frequency-domain. This powerful feature allows to synthesize delayed, integral or derivative signals. A two-port SDD can be then used to implement the nonlinear memoryless block of Fig. 2; the signal $s(t)$ is applied to port #1, while a current $i_2 = -z_0[v_1]$ is imposed at port #2. If the

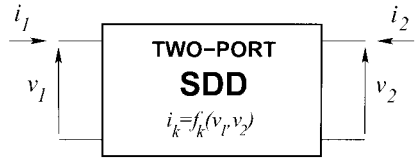

Fig. 4. Schematic representation of a two-port symbolically defined device, available in the ADS CAD tool.

device is loaded on a 1-Ω resistor, the expression for voltage at port #2 is $v_2(t) = y^{(S)}(t)$. The polynomial expansion (1) for $z_0[s]$ can be directly inserted in the SDD programming card. An (M + 2)-port SDD [where $M = (P_A + P_B)$] can be exploited instead in order to implement the purely dynamic nonlinear subsystem with response $y^{(D)}(t)$. In fact, by applying signal $s(t)$ to port #(M + 1) (*input* port) and loading each of first M ports (*auxiliary* ports) on a 1-Ω resistor, shifted signals $s(t - p\Delta\tau)$ $(p = \cdots -2, -1, 1, 2 \ldots)$ can be obtained by imposing a current $i_m(t) = -v_{M+1}(t)$ at the m-th auxiliary port and weighting the spectrum of $i_m(t)$ by means of the function

$$H_m^{(p)}(f) = \exp(-j2\pi fp\Delta\tau). \tag{9}$$

Finally, signal $y^{(D)}(t)$ can be synthesized at port #(M + 2) (SDD *output* port) by loading it on a 1-Ω resistor and imposing a current value $-i_{M+2}(t)$ which matches expression (5), where each value $s(t - p\Delta\tau)$ is substituted by the voltage at the appropriate auxiliary port. Model parameter β_{pn} can be directly inserted in the expression of the current at output port or referred as elements of a file-based array. In Fig. 5, the actual implementation of both nonlinear blocks is shown, in the case of $(P_A + P_B) = 6$. Suitable current probes can be inserted at the output of each subsystem in order to carry out contributions $y^{(S)}(t)$ and $y^{(D)}(t)$, respectively. Model overall output signal $y(t)$ can be read directly as the voltage on the 1-Ω resistor.

As far as the case of SPICE simulator is concerned, the nonlinear memoryless block can be easily imported into the environment by means of a nonlinear two-port symbolical device, available as a standard tool, which allows the designer to impose its input/output relationship in the algebraic analytical form $v_2 = f(v_1)$. Some problems arise when considering the purely dynamic nonlinear subsystem; in fact, the anticipative (5) cannot be directly implemented in the schematic interface, due to the nature of SPICE time analysis numerical algorithms, which allow to compute signal values at the generic discrete instant t_i by means of operators with respect to only previously evaluated samples at "past" instants $(t_{i-1}, t_{i-2}, \ldots)$. In order to overcome such a limitation, the overall time axis of the analysis can be shifted in the "future" by an offset $T_A = P_A\Delta\tau$ [i.e., the nonlinear anticipative memory time which appears in (2)]. By means of this strategy, a cascade of M ideal transmission lines, each characterized by a propagation delay $\Delta\tau$, can be used to synthesize signals $s(t-p\Delta\tau)$. If t' is the new analysis time axis, the instantaneous value at the output of the linear block becomes $s(t' - P_A\Delta\tau)$ and each p-indexed signal in (5) coincides with $s(t' - (P_A + p)\Delta\tau)$. Once signals $s(t - p\Delta\tau)$ are obtained at the output of the transmission lines, an array of M two-input symbolic devices (similar to that used for the static characteristic) can be suitably defined

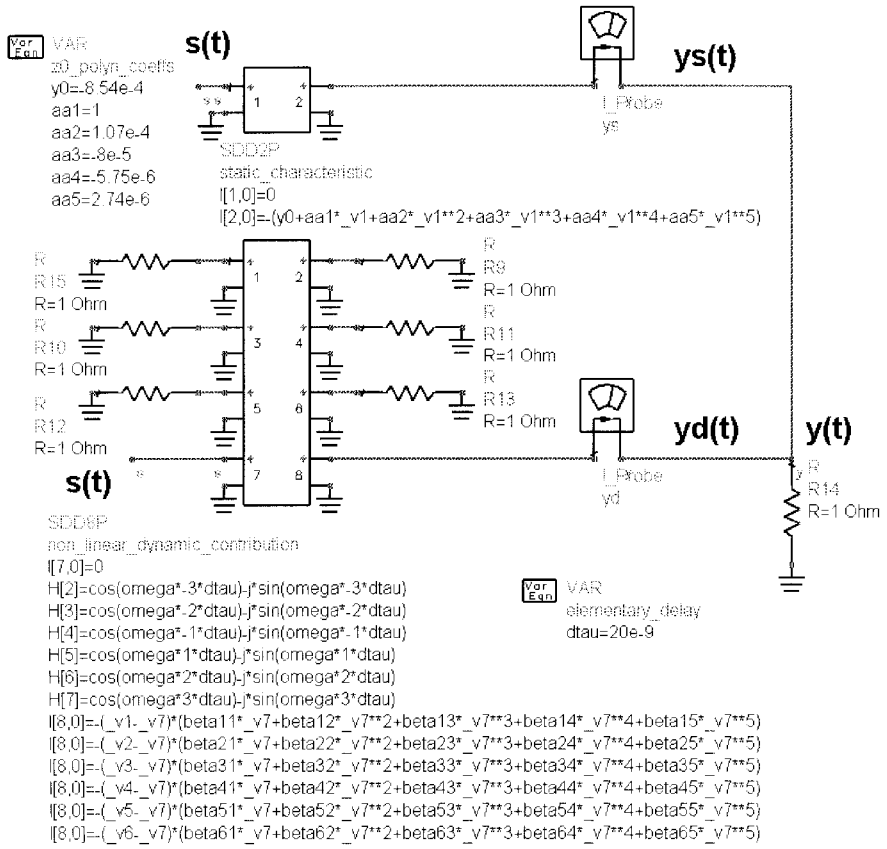

Fig. 5. Actual implementation of S/H-ADC model nonlinear blocks in the framework of ADS CAD package ($P_A = P_B = 3$; $N = 5$).

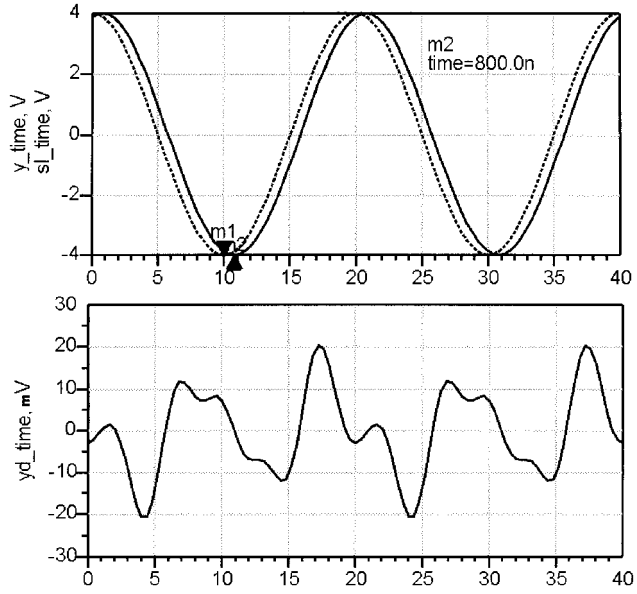

Fig. 6. ADS analysis performed on the modeled device. Above: output response (solid line) with a 50-kHz sinusoidal input (dashed). Below: purely dynamic nonlinear contribution $y^{(D)}(t)$ to the output (time unit: 1e-6 s).

and a summation node introduced to obtain a signal which matches expression (5). The result of the time analysis must be obviously depurated from the same offset $T_A = P_A \Delta\tau$, in order to return to the analytical time axis t.

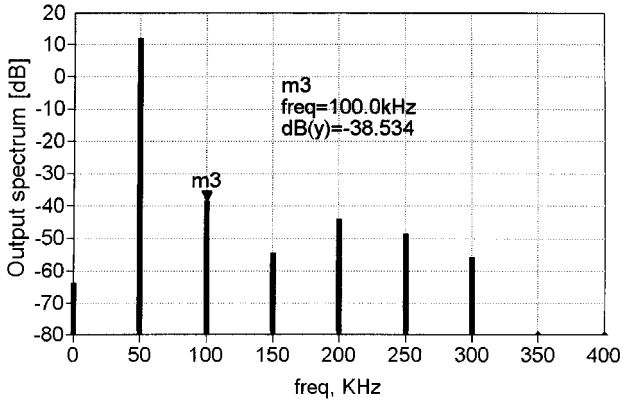

Fig. 7. Spectral components of S/H-ADC device response with input signal shown in Fig. 6 (ADS harmonic-balance analysis).

V. Experimental Results

The proposed S/H-ADC model, experimentally characterized for the 250-kS/s digital acquisition board, has been fully implemented in both ADS and SPICE CAD tools, following the procedures described in the previous section. In order to point out model capabilities of characterizing not only static, but also purely dynamic nonlinearities in the device behavior, results of significant analyzes are presented, both in frequency and time-domain. Fig. 6 shows the device response $y(t)$ when sampling a 50-kHz, 4-V amplitude sinusoidal input signal

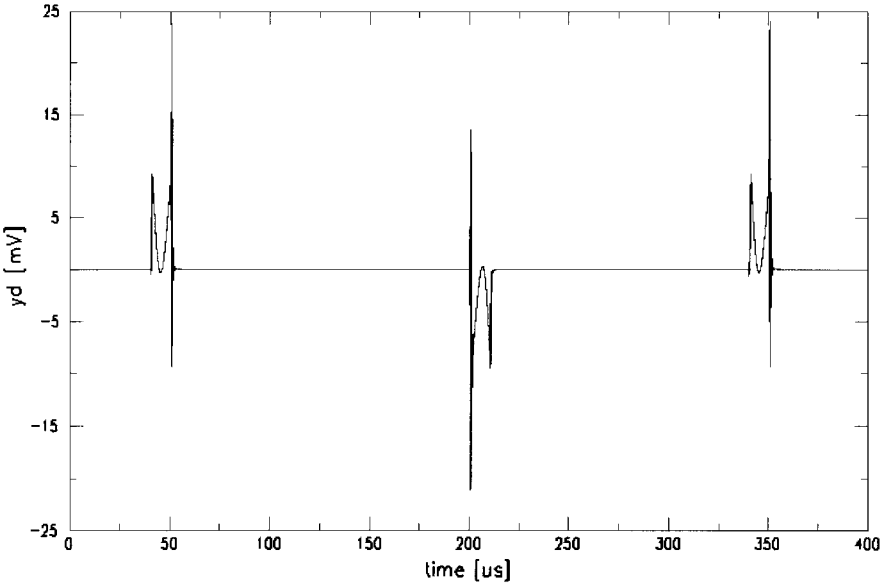

Fig. 8. Purely dynamic nonlinear contribution $y^{(D)}(t)$ to the modeled device response, when a bipolar square waveform is applied at the input (SPICE time analysis).

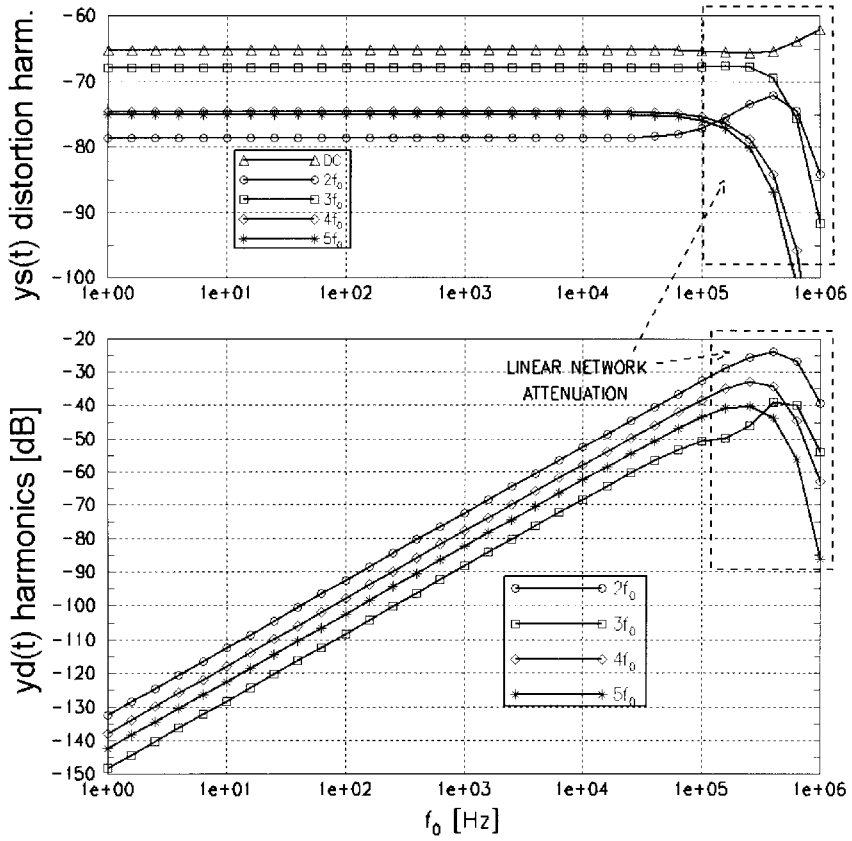

Fig. 9. Comparison between output superior-order harmonics (up to fifth-order) introduced respectively by static and purely dynamic nonlinear effects, as frequency f_0 increases at S/H-ADC input (ADS analysis).

(dashed line in the figure, ADS simulation). The response suffers from a time delay of approximately 0.8 μs, due to the presence of linear memory effects introduced by the input signal conditioning circuits and the sample-hold process. The linear network in the model functional description takes into account these phenomena. In the same figure, the purely dynamic, nonlinear contribution $y^{(D)}(t)$ is shown, which is not negligible at these values of frequency and input signal amplitude and would not be estimated by means of a conventional, static characteristic-based model. In Fig. 7, the spectral components of response $y(t)$ are shown. More complicated input signals can be considered in order to point out the

effects of nonlinear dynamics on the S/H-ADC response. In Fig. 8, the contribution $y^{(D)}(t)$ to the output of the modeled device is shown, obtained through a SPICE time analysis for a bipolar 4-V peak-to-peak square waveform at the input, with a transition time of 10 μs and a period of 300 μs. Relevant contributions to the response are present in correspondence of transitions of the sampled input, which are exclusively related to device nonlinear dynamics.

S/H-ADC nonlinear effects, due to respectively static and purely dynamic nonlinearities, are compared in Fig. 9. The spectral components of $y^{(S)}(t)$ and $y^{(D)}(t)$ that contribute to the overall output distortion are shown for a 4-V amplitude, zero-dc sinusoidal input whose frequency f_0 has been swept from 1 Hz up to 1 MHz. Purely dynamic nonlinear effects, negligible at low frequencies, become even more important than those introduced by the static characteristic, around the value $f_0 = 10\,\text{kHz}$.

VI. Conclusion

A previously proposed nonlinear dynamic model for the characterization of S/H-ADC devices was experimentally identified for a commercial digital acquisition board.

Details about procedures followed in order to measure model parameters were presented. Unlike other behavioral models, based on classical Volterra nonlinear system representation, the characterization of the proposed model does not introduce the need for the generation of complex input test signals or the use of high-order statistics. This is due to the convergence properties of the modified Volterra series from which the model derives. In fact, in the presence of nonlinear memory effects in the device, which are "short" with respect to the typical minimum period of the input signal, only the first-order kernel is needed in the modified series expansion even for large-amplitude input signals, with a strong simplification of techniques devoted to model parameter practical measurement.

Solutions for model implementation in the framework of commercial CAD tools for circuit analysis were shown, as well. Analysis results, performed both in the time and frequency domain by means of Agilent-ADS and Orcad-SPICE packages, were provided, which point out the model capabilities of predicting the effects of purely dynamic nonlinearities on the device response, which can become important already at moderate frequencies. This is an important feature of the proposed approach with respect to other static characteristic-based conventional models, which are not suitable for the characterization of this kind of ADC device nonidealities.

References

[1] S. Boyd, Y. S. Tang, and L. O. Chua, "Measuring Volterra kernels," *IEEE Trans. Circuits Syst.*, vol. 30, pp. 571–577, Aug. 1983.

[2] L. O. Chua and Y. Liao, "Measuring Volterra kernels (II)," *Int. J. Circuit Theory Applicat.*, vol. 17, pp. 151–190, 1989.

[3] P. Koukoulas and N. Kalouptsidis, "Nonlinear system identification using Gaussian inputs," *IEEE Trans. Signal Processing*, vol. 43, pp. 1831–1841, Aug. 1995.

[4] C. Evans, D. Rees, L. Jones, and M. Weiss, "Periodic signals for measuring nonlinear Volterra kernels," *IEEE Trans. Instrum. Meas.*, vol. 45, pp. 362–371, Apr. 1996.

[5] D. Mirri, G. Iuculano, F. Filicori, G. Vannini, G. Pasini, and G. Pellegrini, "A modified Volterra series approach for the characterization of nonlinear dynamic systems," in *IEEE IMT Conf.*, Brussels, Belgium, June 1996, pp. 710–715.

[6] D. Mirri, G. Pasini, F. Filicori, G. Iuculano, and G. Pellegrini, "Finite memory nonlinear model of a S/H-ADC device," in *IMEKO TC-4 Symp. Development Digital Meas. Instrum.*, Naples, Italy, Sept. 1998, pp. 873–878.

[7] D. Mirri, G. Pasini, P. A. Traverso, F. Filicori, and G. Iuculano, "A finite-memory discrete-time convolution approach for the nonlinear dynamic modeling of S/H-ADC devices," in *IMEKO TC-4 EuroWorkshop ADC Modeling and Testing*, Lisbon, Portugal, Sept. 2001, pp. 23–27.

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