A Note on Reliable Full-Duplex Transmission over Half-Duplex Links

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A simple procedure for achieving reliable full-duplex transmission over half-duplex links is proposed. The scheme is compared with another of the same type, which has recently been described in the literature. Finally, some comments are made on another group of related transmission procedures which have been shown to be unreliable under some circumstances.

KEY WORDS AND PHRASES: data transmission, error correction, full-duplex, half-duplex, transmission control, communications
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In a recent paper by W. C. Lynch [1] certain schemes are discussed for achieving full-duplex operation over half-duplex lines by alternating messages in either direction. Each message contains error-detecting information and also control information which is used to effect retransmission if an error occurs. It is assumed that all errors are detected. Lynch conjectures that for transmission schemes of this type, at least two control bits are necessary for infallible operation, as in the method he proposes, and cites a procedure using one control bit which can be shown to fail under some circumstances.

An extremely simple transmission scheme of the above type has been devised at the National Physical Laboratory for use in a general-purpose data communication network [2]. The method uses only one control bit, can be shown to be infallible (again assuming that all errors are detected), and is closely related to Lynch's reliable transmission scheme.

The procedure is represented by the two finite-state automata shown in Figure 1 for two communicating terminals labeled A and B. Each message transmitted by a terminal contains error detection information and a control bit termed the "alternation bit." The edges of the automata are labeled with the origin of the message currently being received or transmitted (label underlined) and the value of the alternation bit. The double arrows indicate that the current input has been accepted by the terminal and that a new message has been fetched for output.

The automata for the reliable simplex scheme described in [1] are shown in Figure 2. This procedure makes use of a "validation" bit, to indicate correct or incorrect receipt of a message, and an alternation bit. Instead of taking one fixed value of the validation bit to mean "acknowl-

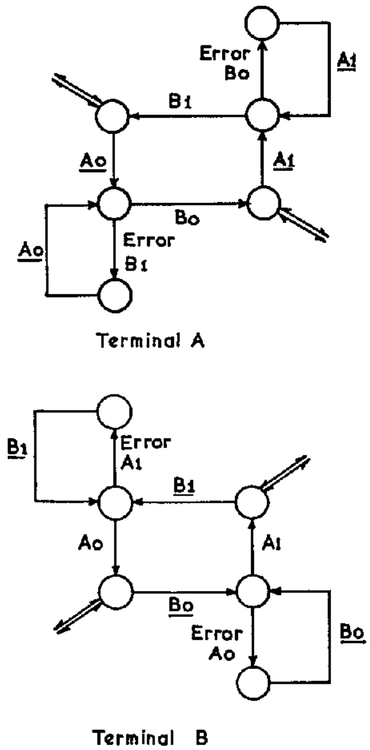

Fig. 1. Finite-state automata for the reliable half-duplex transmission scheme of National Physical Laboratory

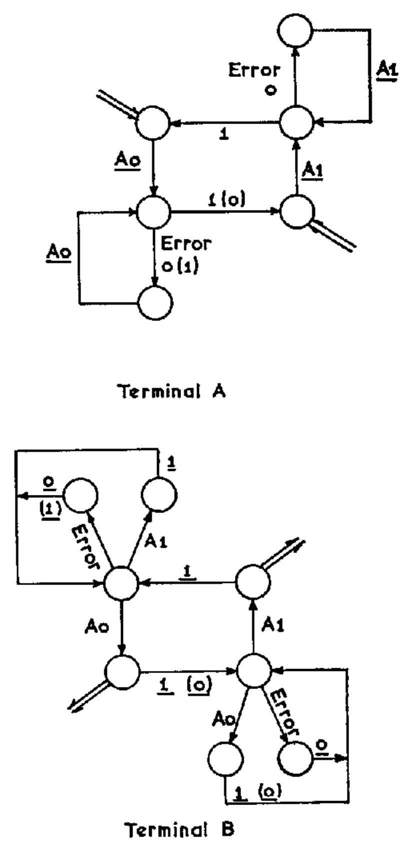

Fig. 2. Finite-state automata for the reliable simplex transmission scheme of Lynch

edge" and the other to mean "negative acknowledge," we can make the validation bit alternate so that a *change* in the value of this bit means "acknowledge." This alternation of the validation bit is shown by the parenthesized values in Figure 2. We thus have the key to the relationship between the two methods, the alternating validation bit becoming additionally the *alternation* bit for message transmission in one direction while the alternation bit for the reverse direction serves additionally as a *validation* bit.

The proof of the infallibility of the NPL scheme follows closely that given in [1] for the simplex scheme and need not be repeated here. The effect of message drops and the necessary recovery procedure are the same for both schemes. Undetected errors which change the alternation bit (a contingency which must arise in practice to an extent depending upon the degree of protection used) will at worst cause the loss of two messages in one direction and the triplication of a message in the other direction and at best have no adverse effect, depending on the part of the cycle in which the error occurred. The two terminals will always recover correct phase within one cycle.

One advantage of Lynch's duplex scheme results from the fact that it is constructed from two independent simplex procedures, while in the NPL scheme the transmissions are interdependent. Thus the former method would operate more efficiently for certain patterns of error incidence, since useful messages can flow in one direction while error recovery is taking place in the opposite direction. In general, however, the difference in efficiency is not expected to be great. In addition, the latter scheme is somewhat simpler to implement.

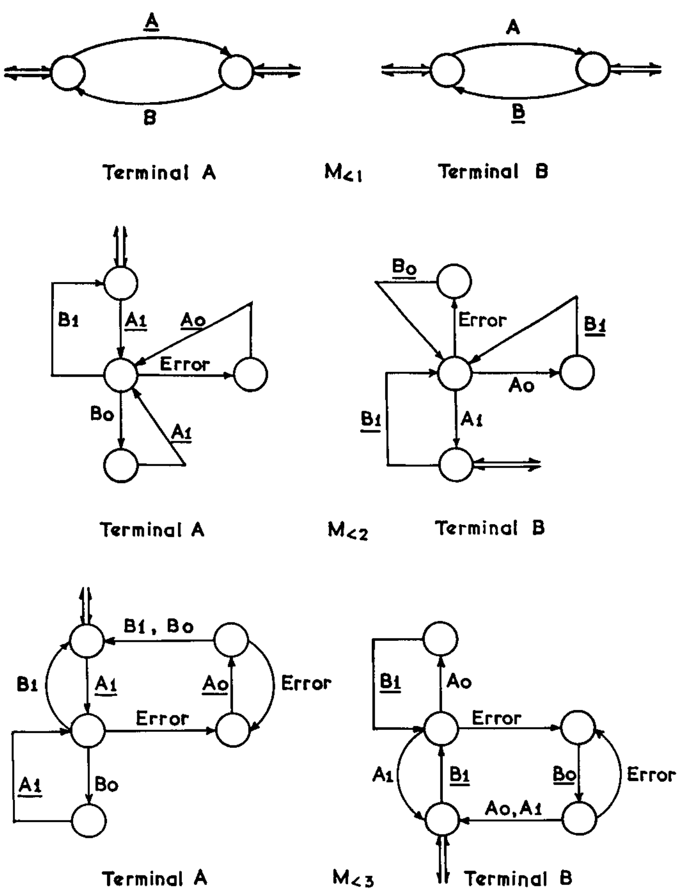

FIG. 3. Finite-state automata for three unreliable half-duplex transmission schemes

The inadequate scheme discussed by Lynch uses an "acknowledge" bit to request a repeat when the previously received message was in error. This procedure fails when two successive errors occur (in opposite directions). The procedure is shown in Figure 3 as the pair of finite-state automata labeled $M_{<2}$. Also shown in this diagram are two other pairs of automata, $M_{<1}$ and $M_{<3}$. $M_{<3}$ operates successfully provided that fewer than three successive errors occur. $M_{<1}$ is a trivial case, included for completeness. The existence of these three pairs of automata leads to an interesting conjecture, namely, for any positive integer, i, is it possible to construct a pair of automata, $M_{<i}$, which will operate successfully provided that fewer than i successive errors occur?

There is apparently a need for more research in the area of transmission control and error recovery techniques, for the classification and comparison of the various schemes, and for a formalization which hopefully would lead to a better understanding of the interrelationship between the methods now extant.

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Commentary on the Foregoing Note

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I heartily concur with all the comments made by Bartlett, Scantlebury, and Wilkinson concerning the transmission of information. The type on my paper was hardly set before I became aware of the fact that my conjecture at the end of the paper was incorrect. A student of mine, Mr. F. Grant Saviers, was in the process of writing a master's thesis concerned with the reliable transmission of teletype information. It was quite important for him to develop a one-bit correction scheme since the message in his case was a teletype character and an extra bit is a substantial amount of additional information. Mr. Saviers and Mr. Fred Camerer, of the Jennings Computer Center, devised a transmission scheme using one bit which is precisely the same one invented independently and described by Bartlett, Scantlebury, and Wilkinson. Mr. Saviers was later able to prove by means of automata and

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as required to reach vertical lines. In addition, the designer must be sure to allow adequate access to the component leads.

Conclusions

The power of this approach is its use of the context of all the interconnections in an area to make routing decisions. Due to the use of this context, the program has been very effective in maximizing the number of interconnections on the board.

The ratio between the vertical plus horizontal length of completed interconnections and the total available length is approximately 0.5. The program described here achieves high vertical line utilization. As a consequence, finding an open vertical line for rerouting an interconnection is difficult; the net result is fewer reroutings and, therefore, limited horizontal line utilization. The most effective way of obtaining higher horizontal line utilization appears to be more flexibility in "jinking" or moving lines aside, plus more flexibility in the detail routing. After interconnections have been deleted to eliminate the overloaded areas, some of the remaining wires have a very limited choice of routes that will not cause overloading.

The solution to the above problems appears to be:

1. Use "nearness to overload" information (computed from the context of all interconnections on the board) in defining approximate routes and via positions for all interconnections.

2. By using the approximate routes in (1) above, the routing problem is changed to two single-layer routing problems: one with vertical lines and one with horizontal lines (with the exception that via positions can be adjusted slightly to facilitate the routing).

3. Scan each side of the board with an aperture (orthogonal to the lines) to determine interconnection routing and helpful via position adjustments, incorporate the via position adjustments, and repeat the process until mutual agreement on via positions is obtained and all conflicts are resolved (by deleting the offending interconnections if necessary).

The end result of the program described here is shown in Figure 5, a composite photograph of the computer-generated artwork for the two sides of the circuit board.

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state diagrams that this scheme was reliable. His conjectures as to its efficiency of operation are precisely the same as those outlined in the Bartlett, Scantlebury, and Wilkinson note. As a matter of fact, in carrying out the research for his paper he discovered an article by Schwartz [1] in which the double-bit scheme which I described in my paper had been previously described. The paper must not have made a very deep impression since it proved to be extremely difficult to find in the literature and was stumbled upon only by accident.

I should like to make a few comments concerning the use of automata and state diagrams in regard to transmission schemes. This seems to be an extremely useful approach. First of all, I might comment that the Figure 2 in the Bartlett, Scantlebury, and Wilkinson note is a little bit misleading, since it presents only one half of the full duplex transmission. As a result it appears to be unsymmetric whereas the scheme itself is completely symmetric. The scheme proposed by Bartlett, Scantlebury and Wilkinson and also that used by Saviers is asymmetric in the following sense. The automata at each end of the line are identical but their initial states must differ from each other under the penalty of the automata getting into a loop in which no transmission occurs. This is not true in the scheme that I presented where not only the automata at each end of the line are exactly the same but their starting states are also identical. I not only believe in the correctness of the conjecture presented by Bartlett, Scantlebury, and Wilkinson at the end of their paper (concerning automata that would be arbitrarily error free), but I also believe that a general theory of transmission automata can be created to describe the features of various schemes, both reliable and unreliable.

I feel it should be possible to develop proof procedures for the reliability of automata and also to be able to determine performance characteristics. I am in particular agreement with their comment that there is a need for more research in this area.

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