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A Novel and High-Gain Switched-Capacitor and Switched-Inductor-Based DC/DC Boost Converter With Low Input Current Ripple and Mitigated Voltage Stresses

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ABSTRACT High voltage gain DC-DC boost converters are widely used in grid-connected applications through integration with the Renewable Energy Sources (RESs). Photovoltaic (PV) arrays or Fuel Cells (FCs) generate a limited value of the DC voltages and then for high power and high voltage applications, at the first stage, these voltages should be increased. This study presents a high gain, single-switched, and efficient DC-DC boost converter using the switched-capacitor and switched-inductor cells. These blocks easily can enhance the voltage and present an input current with the least values of the ripples. This will be done through replacing the location of the input inductors and by applying a switched-inductor block. Magnetizing in parallel and demagnetizing in series for the inductors present the smaller input current stresses. A single switch is used for the proposed boost converter that directly decreases the complexity of the control circuit for obtaining a fixed DC voltage at the output side for flexible input voltages or loads. More voltages will be presented by the used switched-capacitor cell simply by adding several diodes and capacitors. A deep and detailed mathematical analysis will be presented for continuous (CCM) and discontinuous conduction modes (DCM) and a 200 W laboratory-scaled prototype is presented. The results of the hardware tests confirm the correctness of the theoretical analysis and simulation results.

INDEX TERMS DC-DC boost converter, switched-capacitor, switched-inductor, continuous conduction mode (CCM), discontinuous conduction mode (DCM).

I. INTRODUCTION

High voltage gain DC-DC converters are widely used in industrial, grid-connection, and Renewable based applications [1]–[3]. Since some kinds of the RESs like the Photovoltaic (PV) arrays and Fuel Cells (FCs) can only generate limited values of the DC voltages, for any kind of grid or industrial applications, these voltages should be increased through a power converter circuit. For that, many types of step-up converters have been presented [4]–[6]. Conventional DC-DC boost converters include an inductor as the magnetic field storage, a capacitor as the electric field storage, and a power switch and diode as the semiconductor components. This structure can double the input voltage for 50 percent of the duty cycle of the power switch. Although, higher voltages can be obtained for longer duty ratios, for many of the applications, this voltage is not enough and leads to high power losses. For example, for a PV panel with 24 VDC, by a conventional DC-DC boost converter, a voltage close to 48 VDC can be obtained. Furthermore, the power values that can be transferred through a classic converter are less than the required values for high-power applications. For that,

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many different types of DC-DC boost converters have been presented. Isolated or non-isolated boost converters, unidirectional and bidirectional converters, voltage or current-fed structures, converters with hard or soft Pulse Width Modulation (PWM) switching techniques, and minimum and non-minimum-phase converters are among the presented topologies. All these converters have advantages and disadvantages. For example, non-isolated converters normally use a transformer to enhance voltage [8], [9]. For that, at the first stage, an inverter block is applied to convert the input DC voltage to an AC one, and at the second stage, this voltage is increased by the transformer. After that, a rectifier block is used to convert the generated high amplitude AC voltage to the desired DC voltage. As can be predicted, different inverter, transformer, and rectifier blocks should be used that directly enhance the number of the used components, cost, weight, and power losses. Unidirectional converters include both the power switches and diodes and can only convert the DC to the AC or AC to the DC voltages [10], [11]. As can be found, these types of converters are not suitable for many of the onboard applications such the vehicle-to-grid (V2G) or grid-to-vehicle (G2V) utilizations as a part of the electrical vehicles (EVs) applications [12]–[16].

Instead, in the unidirectional boost converters, diodes are replaced by the power switches and a control algorithm, and a circuit should be added to the converter to activate or deactivate the replaced switches when they should be in ON or OFF-states. These converters are suitable for many of the onboard applications like sensor applications or EVs, but a control prototype circuit should be designed and applied. Voltage and current-fed types of the converters normally can decrease and increase the input voltage at the output side respectively [17]–[19]. This means the voltage-fed converter acts as a Buck converter and includes an input capacitor whereas the current-fed converter includes an inductor at the input side and enhances the input voltage. These converters normally use a transformer between the input and output blocks which means they need the inverter and rectifier blocks that easily can present higher power losses and lower efficiency values. The main part of the power losses is the switching one. The dynamic losses can be presented and calculated through a current with a power of two through the internal resistance of the components. This type of power loss can be presented for all passive and active semiconductor devices like the capacitors, inductors, switches, and diodes. But in comparison to the switching losses, the dynamic losses are completely smaller. This comes back to cross points in the voltage and current curves of the semiconductors. It means that hard switching techniques, the power losses for the time intervals that a switch or diode is turning on or off completely have a high loss value. For ideal switching conditions, when a switch is activated, the current enhances, and voltage decreases through a step waveform. But in practice, it can be seen from the time intervals that both of the current and voltage waveforms exist. By increasing the switching frequency, the number of the intersection time intervals will be increased and gives more switching power losses. For that, different soft switching techniques like the zero voltage (ZVS) and zero current switching (ZCS), and zero voltage (ZVT) and zero current transition (ZCT) are presented [20]–[23]. Although these techniques help the switches and diodes to work under fewer power losses, normally the design of these snubber structures is difficult and the switching frequency of the converter is extremely high. Also, more components should be added to the converter.

Furthermore, voltage gain is an important issue that should be considered. Charge pump or switched capacitor (SC) circuits can simply be added to the converter to enhance the gain of the converter. In this technique, the energy transferring issue is done by the capacitor-diode (C-D) or capacitor-switch (C-S) blocks and no more inductors are added. The most important advantages of the SC blocks are the monolithic integration capability and enhancing the voltage through the simple (C-D) or (C-S) cells. In fact, the application of more SC blocks can present a higher DC voltage. To simplify the SC-cell configuration, one technique is using diodes instead of transistors. Although the dynamic loss of the diode normally is more than for a transistor, the control of the transistors can require a difficult algorithm and implementation. Also, by using the fast recovery silicon carbide (SiC) and Gallium Nitrite (GaN) types of the power diodes, this loss can be decreased to a large extent. Different studies are investigating SC configurations. Reference [24] presents a configuration with six power switches, three floated and one grounded capacitor, and four power diodes. The most advantage of this converter can be summarized as receiving the low–ripple input currents and variable voltage ratio based on the applications. Reference [25] presents an SC cell-based converter with totally two power switches, three floating and three grounded capacitors, and six power diodes. The soft switching capability of the proposed converter and less current stresses for the proposed SC block are among the most important features of the proposed configuration. The converter in [26] has a total of ten power switches, three floated, and one grounded capacitor without any power diodes. Bypassing the fault in onboard form, and the possibility to be connected to multiple loads are the important specifications of the converter. The converter in [27] presents a high voltage gain and lower power losses based on the small current stresses for the power components through the eight power switches, and four floated capacitors. The SC configuration will be activated through the two different switching approaches. Simple control schematics, including only two power switches and a variable and flexible voltage gain property, are among the most important advantages of the converter in [28]. This converter uses six grounded capacitors and six power diodes.

Another technique to enhance the voltage by a boost converter is using switched-inductor (SL) blocks. By this technique, normally a pair of the same inductors are used and magnetized in parallel and demagnetized in series. By this method, the specified capacitor will be charged and then a

higher output voltage is obtained at the next working steps. A single core can be used for both inductors to minimize the weight and cost of the converter. This is an appropriate aspect for the proposed configuration since weight and cost are among the serious problems with the inductors. Different SL-based circuits can be found in the literature. Elementary-lift cells, self-lift cells, and double lift-cells are among the most famous switched-inductor-based configurations. Basic SL cell includes three diodes and two inductors. For a conventional boost converter, the gain equation can be presented as $V_O = \frac{V_{in}}{1-D}$. In this equation, V_{in} and V_O are the input and output voltages and D is the duty ratio. The basic SL cell can increase the gain equation to the $\frac{V_{in}(1+D)}{1-D}$. The recent equation shows that the gain of the converter can enhance from two to three at $D = 0.5$ through the basic SC-cell. This rate can be enhanced by the elementary-lift cell converter to $\frac{V_{in}(2-D)}{1-D}$, self-lift cell to $\frac{2V_{in}}{1-D}$ and by double self-lift cell to $\frac{V_{in}(3-D)}{1-D}$ [29].

To take advantage of the *SC* and *SL*−based DC-DC power boost converter, this study presents an SC-S*L*-based power DC-DC boost converter with a high voltage gain including only on power switch. This converter can present a voltage at the load side equal to 7.5 t*imes* greater than the input voltage for c $D = 0.5$. More voltage gains can be obtained through longer duty ratios or more SC cells. For example, for $D = 0.8$, approximately, twenty times *of* the input voltage can be reached at the output, or for $D = 0.5$, by two cascaded SC-cells, more than twelve times *of* the input voltage can be reached. The enhancing of the voltage is done by a simple diode connection configuration that eliminates the need for the supernumerary power switches. A PI-based controller technique is presented to fix the DC voltage under the variable input voltages or variable loads working conditions. A comprehensive theoretical investigation, simulation, and hardware test results are presented and confirm the reliability of the proposed converter for different working situations.

II. PROPOSED CONVERTER

Figure 1(a) illustrates the fundamental configuration for the SL-cell. As can be seen, a pair of the inductors are in connection with three diodes to enhance the voltage. For that,normally a pair of the same inductors are magnetized in parallel and demagnetized in series connections. This means that the diodes D1 and D2 are activating simultaneously and for the time intervals that the diode D3 is deactivated. The state of the diodes for parallel and serial charging and discharging operational modes are seen in figures 1(b) and 1(c), respectively. For minimizing the volume of the inductors, since the same inductors are used normally, a common core is applied. This can decrease the weight and cost of the configuration. Application of a pair of the inductors can decease the current ripples for the input source, which is an important feature in DC-DC converters.

Figure 2(a) presents a conventional SC-cell. As can be seen, when the switch S1 is activated the voltage across the

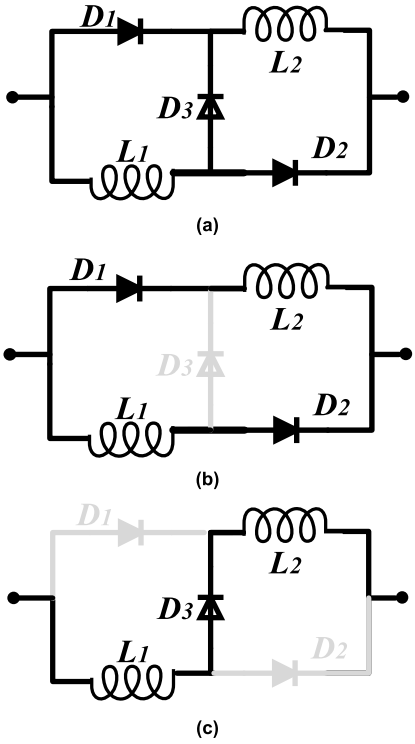


FIGURE 1. (a) The conventional SL-cell, and the configuration when inductors are (b) magnetized and (c) demagnetized.

capacitor C1 is equal to the input voltage V_{in}. At the next step, this voltage is transferred across the capacitor C2 by activating the switch S2. After several time intervals, this voltage can be completely transferred across the load. Also, there are different serial SC blocks that can be used in multi-phase approaches to enhance the input voltage. Figure 2(b) presents a multi-phase SC-cell. For this figure, when the switches S1 and S2 are in phase 1, the input voltage is transferred across the capacitor C1, and then by changing the location of the phases for the switches, a voltage equal to twice the input voltage is transferred across the second capacitor for the load.

The higher DC voltages can be obtained through a cascaded SC-cell configuration. This state can be seen in figure 1(c). This figure shows that when the switches are in mode I, the voltage across the capacitor C1 is equal to V_{in}. For the next working phase and by changing the states of the switches to phase II, capacitor C1 is connected in series with the input voltage V_{in}. Therefore, a double voltage of the V_{in} is transferred to the capacitor C2. This state will be continued for the next time intervals and finally a voltage with a fourth times greater than the input voltage appears across the capacitor Co. For the proposed converter in this study, a novel SC-cell is presented that can double the input voltage.

A. PROPOSED SL AND SC-CELL-BASED BOOST CONVERTER

Firstly, in figure 3, a flowchart is presented to show the different steps of this study. As can be seen, after presenting

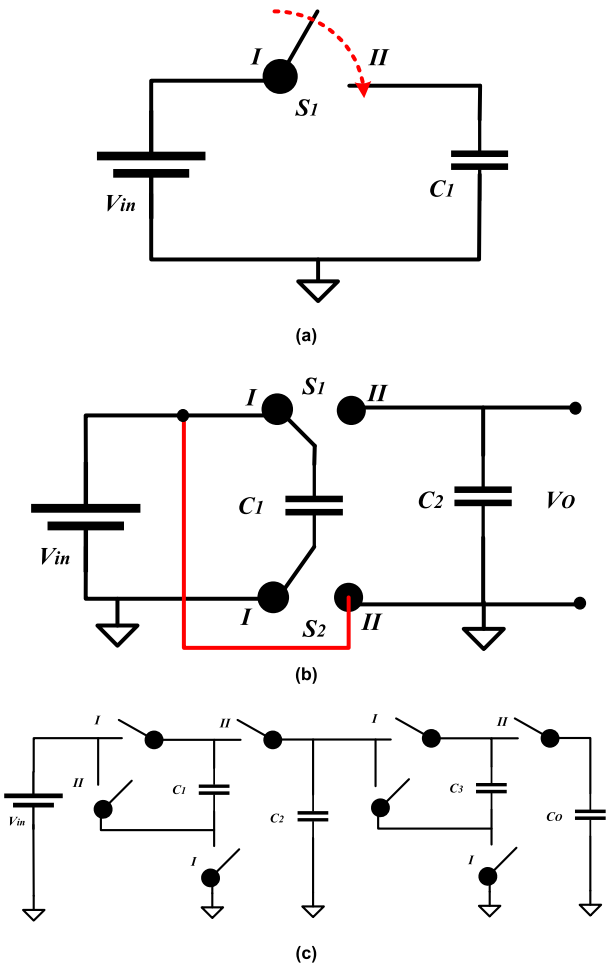


FIGURE 2. (a) A basic SC-cell, (b) a multi-phase SC-cell, and (c) a high-gain multi-phase SC-cell configuration.

the proposed topology, the theoretical analysis is done for both CCM and DCM working modes, and then the simulation and hardware test results are compared with these results. Figure 4(a) shows the proposed converter. The proposed DC-DC boost converter, as can be seen, is formed by using a power switch (S1), five power diodes (D1, D2, D3, D4 and D7), two inductors (L1 and L2) and two capacitors (C1 and Co). For this side, the location of the switch, inductors, and diode D_1 is changed. Also, a switched-inductor block has been added to enhance the gain of the boost converter. The SC-cell is formed from two capacitors (C2 and C3) and two diodes (D5 and D6). This part is enhancing the voltage through the power diodes instead of the switches that can decrease the complexity of the control circuit and is among the most important specifications of the proposed SC-cell. The reaction of this part of the proposed converter is analyzed in this section through two different operating modes of the power switch. This can be followed through figures 4(b) and (c). Figures 4(b) and (c) show the state of the converter when the switch is activated and deactivated respectively.

B. GAIN CALCULATION FOR THE CONVERTER

For the time interval that the switch is activated, both inductors L_1 and L_2 start to be magnetized through the switch, and diodes D_2 and D_3. For this time capacitor C_1 is discharged since the current is established and passes from the negative pole of this capacitor and capacitor C_2 is charged through the power diode D_5 to be ready for discharging across the load for the next time interval. Also, the diode D_4 is deactivated because the anode of this diode receives a voltage near to zero volt, then cannot conduct the current. The voltage across the inductors L_1 and L_2 can be shown by:

$$V_{L1\,and\,L2} = V_{in} = L\frac{di_L(t)}{dt} \tag{1}$$

Since the same inductor values are used, therefore, in all equation's inductors L1 and L2 can be shown with L. in (1), $V_{L1\,and\,L2}$ presents the voltage across the inductors and V_{in} shows the input voltage. Diode D7 is in forward-biased working state and the capacitor Co is charged.

For the time interval that the power switch is deactivated, the diode D1 works in ON-mode and charges the capacitor C1. Also, both inductors begin to discharge since a serial connection will be inevitable in this operational mode and the voltage across per inductor will be negative since a high value of the voltage drops across the capacitor C1 to charge it. In this working mode, both diodes D2 and D3 are deactivated. Also, diode D6 since receives a negative voltage at the cathode in comparison with the anode voltage that is connected to the positive pole of the capacitor C3 is activated and for the same reason, diode D5 is deactivated. Diode D7 is in Off-mode since the cathode of this diode is connected to an output voltage that is always greater than the input voltage. For this mode, since a serial connection forms between the inductors, the KVL through the input voltage and capacitor C1 can be presented by:

$$V_{in} = 2V_L + V_{C1} \tag{2}$$

Therefore, the voltage across the inductors can be calculated by (3):

$$V_{in} = 2L\frac{di_L(t)}{dt} + V_{C1} \rightarrow V_L = L\frac{di_L(t)}{dt} = \frac{V_{in} - V_{C1}}{2} \tag{3}$$

Since the total value of the voltage drops across an inductor in a switching circuit is zero based on periodic operation, one can write:

$$V_{L,ON} + V_{L,OFF} = 0 \rightarrow V_{in}D + \left(\frac{V_{in} - V_{C1}}{2}\right)(1-D) = 0 \tag{4}$$

Therefore, the voltage across the capacitor C1 can be written:

$$V_{C1} = V_{in}\left(\frac{1+D}{1-D}\right) \tag{5}$$

This equation shows that the proposed converter can increase the input voltage $(1+D)$ times more than a conventional boost converter by adding a SL-cell. Furthermore, this configuration needs to have currents with smaller ripple magnitudes in

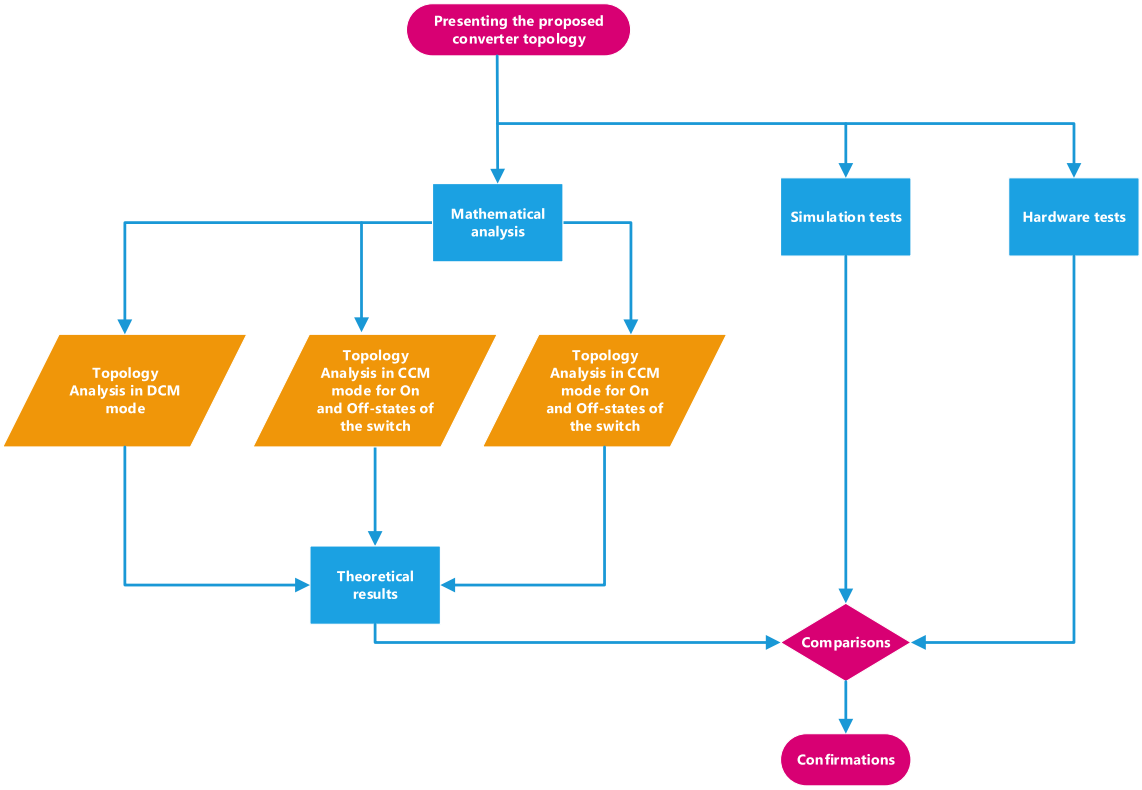


FIGURE 3. A flowchart to present the steps of the study.

comparison with the current of the input inductors in classical boost converter. This subject will be analyzed in detail in the next subsection.

For obtaining the voltage across the capacitors C2 and C3, one can write:

$$V_{C2} = \int_0^{DT} (V_{C1} + V_{L1})\, dt + \int_{DT}^{T} (V_{C1} + V_{L1} + V_{L2} - V_{C3})\, dt = 0 \quad (6)$$

And:

$$V_{CO} = \int_0^{DT} (V_{C2} - V_{C3})\, dt \quad (7)$$

Then, the voltages for the capacitors C2 and C3 can be obtained:

$$V_{C2} = \frac{V_{in}(2-D)}{(1-D)},\ and\ V_{C3} = \frac{V_{in}}{(1-D)} \quad (8)$$

Therefore, the gain of the converter M_{CCM} can be obtained:

$$M_{CCM} = \frac{V_0}{V_i} = \frac{(3+D)}{(1-D)} \quad (9)$$

This equation shows that the proposed converter can enhance the input voltage to 7.5 times for the duty ratio $D = 0.5$ and closed to 20 times for the $D = 0.8$. The greater voltages can be obtained by more cascaded SC-cells. A simple comparison easily can show that the gain of the proposed converter by considering the number of the used component numbers is acceptable and comparable with many of the recently designed boost converters in literature.

C. CURRENT RIPPLES FOR THE INDUCTORS

One of the most important features of the converter is achieving limited ripples for the input current. It is essential for the long-life calculations and reliability of the connected RES source especially if it is a PV module. Therefore, the calculation for this parameter should be presented. When the power switch is activated, the current of the inductors can be presented by (10 and 11):

$$V_{L1,\,and\,L2} = V_{in} = L\frac{di_L(t)}{dt} \rightarrow \frac{di_L(t)}{dt} = \frac{\Delta i_L}{DT} = \frac{V_{in}}{L} \quad (10)$$

$$(\Delta i_L)_{closed} = \frac{V_{in}}{L} DT \quad (11)$$

In (11), $(\Delta i_L)_{closed}$ is the ripple of the inductors when the switch is in On-sate. Also, for the time intervals that switch is deactivated, the current ripple of the inductors can be found by (12 and 13):

$$V_L = L\frac{di_L(t)}{dt} = \frac{V_{in} - V_{C1}}{2} \rightarrow \frac{di_L(t)}{dt} = \frac{\Delta i_L}{(1-D)T} = \frac{V_{in} - V_{C1}}{2L} \quad (12)$$

$$(\Delta i_L)_{open} = \frac{V_{in} - V_{C1}}{2L}(1-D)T \quad (13)$$

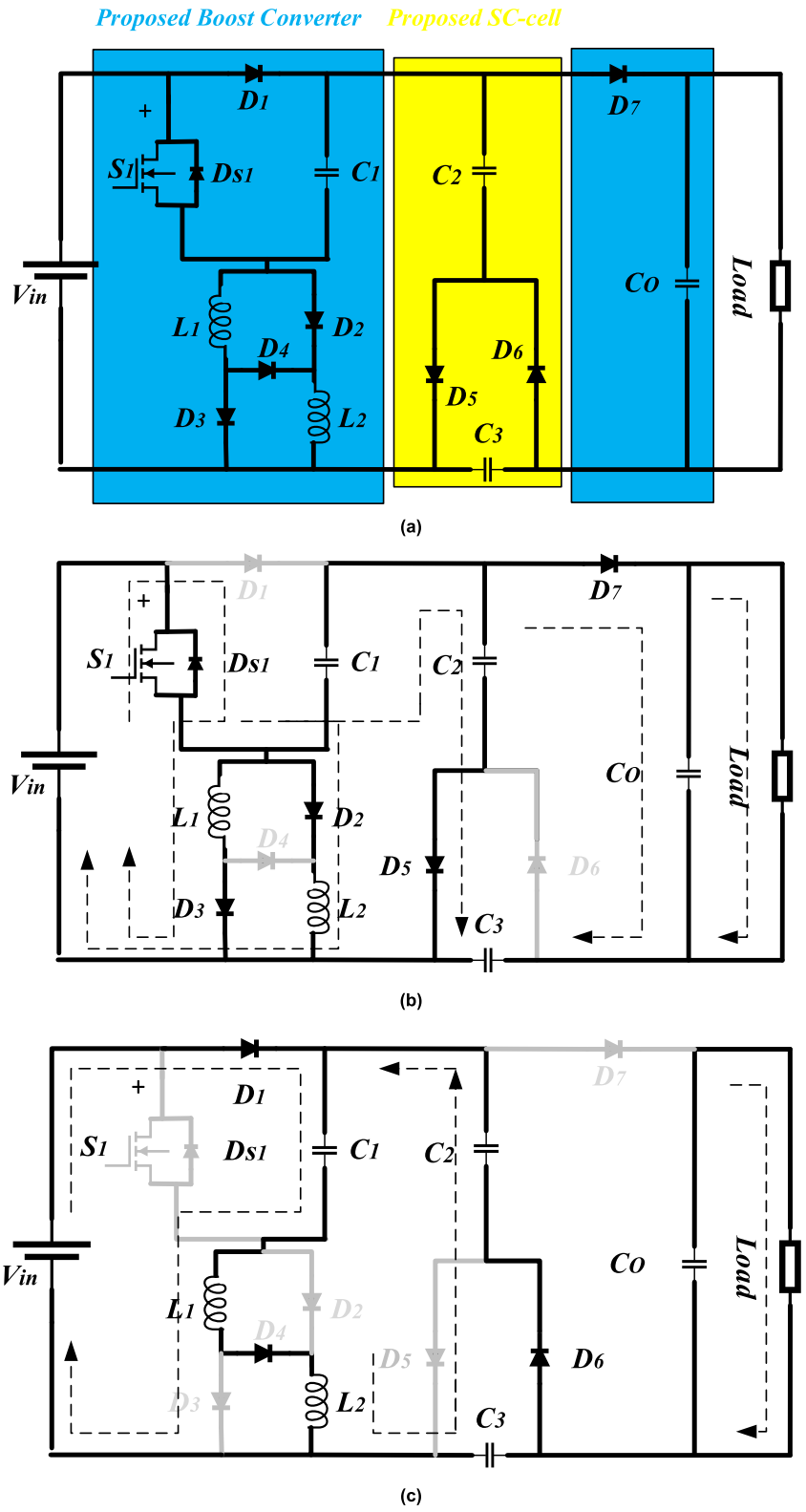


FIGURE 4. (a) The proposed SL-SC boost converter, the state of the proposed DC-DC boost converter when the power switch is (b) activated and (c) deactivated.

$(\Delta i_L)_{open}$ presents the ripple of the current for the inductors when the switch is deactivated. Also T is a period of the switching signal. Since the voltage across the capacitor C1 is approximately equal to the output voltage of the converter without considering the SC-cell, therefore one can change V_{C1} to V_{O1}. V_{O1} is the voltage at the input side of the

SC-cell. Since for the steady-state operation, the change of the current should be zero for the inductor, from (11) and (13) one can write:

$$(\Delta i_L)_{closed} + (\Delta i_L)_{open} = 0 \rightarrow \frac{V_{in}}{L} DT + \frac{V_{in} - V_{O1}}{2L} (1 - D)\, T = 0 \quad (14)$$

For ideal working conditions, the average power absorbed by the load is the same as the generated power by the source. If a load like R_O is considered as the load, the output power P_{out}, equal to the input power P_{in} can be calculated simply by (15):

$$P_{out} = \frac{V_O^2}{R_O} = V_O I_O, P_{in} = V_{in} I_{in} = V_{in} I_L\, (1 - D)\, T \quad (15)$$

This equation can be written by considering that the current of the inductors is the same as the current of the input source for the time interval that the switch is in ON-state. Therefore:

$$V_{in} I_L\, (1-D)\, T = \frac{V_{O1}^2}{R_O} = \frac{(V_{in} \left(\frac{1+D}{1-D}\right))^2}{R_O} = \frac{(V_{in}\, (1+D))^2}{(1-D)^2 R_O} \quad (16)$$

The average amount of the inductor current can be calculated by (17):

$$I_L = \frac{V_{in}\, (1 + D)}{(1 - D)^2} \quad (17)$$

The maximum and minimum values of the inductor current can be found by (18) and (19) by considering the (11) and (17):

$$I_{L,max} = I_L + \frac{\Delta i_L}{2} = \frac{V_{in}\, (1 + D)}{(1 - D)^2 R_O} + \frac{V_{in}}{2L} DT \quad (18)$$

$$I_{L,min} = I_L - \frac{\Delta i_L}{2} = \frac{V_{in}\, (1 + D)}{(1 - D)^2\, R_O} - \frac{V_{in}}{2L} DT \quad (19)$$

These recent equations show that the minimum and maximum amplitude of the ripples for this converter is at least equal to half of the ripple's amplitude for the conventional boost converter. For Continuous Conduction operational Mode (CCM), $I_{L,min}$ needs to be greater than zero. Therefore, for obtaining the boundary between CCM and Discontinuous Conduction Mode (DCM), inductor current can be determined from (20):

$$I_{Lmin} = \frac{V_{in}\, (1+D)}{(1-D)^2\, R_O} - \frac{V_{in}}{2L} DT = 0 \rightarrow \frac{V_{in}\, (1+D)}{(1-D)^2\, R_O} = \frac{V_{in}}{2Lf} D \quad (20)$$

In this equation f is the switching frequency. The minimum value of the inductors and switching frequency of the proposed boost converter for operating in CCM is therefore:

$$(Lf)_{min} = \frac{D\, (1 - D)^2 R_O}{2\, (1 + D)}, \quad L_{min} = \frac{D\, (1 - D)^2 R_O}{2\, (1 + D) f} \quad (21)$$

This equation easily shows that the selected inductor values are dependent on the duty ratio, the load value, and the switching frequency.

D. VOLTAGE RIPPLE FOR OUTPUT CAPACITOR

A Fixed voltage with a minimum value of the ripple should be presented at the output sides of the converter. This will prepare an appropriate working condition for the load block. The output capacitor value and the voltage ripple across this capacitor will be investigated in this sub-section. It is possible to find the voltage variation across a capacitor by considering the currents of the capacitor. The capacitor electrical charge Q, can be calculated as (22) for the time interval that the C_2 is charged:

$$|\Delta Q| = \left(\frac{V_O}{R_O}\right) DT = C_2 \Delta V_O \quad (22)$$

This equation has been written based on the fact that the current of the output capacitor for the ON-state time interval of the switch is equal to the $\frac{V_O}{R_O}$.

Therefore, the voltage ripple for this capacitor can be found as presented in (23):

$$\Delta V_O = \left(\frac{V_O}{R_O C_O}\right) DT = \frac{V_O D}{R_O C_O f} \quad (23)$$

$$\frac{\Delta V_O}{V_O} = \frac{D}{R_O C_O f} \quad (24)$$

(24) shows that it is possible to calculate the value of the capacitor C_O in terms of the output voltage ripple:

$$C_O = \frac{D}{R_O(\Delta V_O / V_O) f} \quad (25)$$

The state of the current and voltage for the components of the boost converter is shown in figure 5.

E. CONTROLLER DESIGN

By considering a load like R, at the output points of the converter, for the time intervals that the power switch is activated, DT, the equation (26) can be written:

$$C_O \frac{dV_O}{dt} + \frac{1}{R_O} V_O = d(i_{in} - 2i_L - 2i_{C2}) = u \quad (26)$$

With a simple placement in (26), one can write:

$$C_O S V_O + \frac{1}{R_O} V_O = V_O \left(C_O S + \frac{1}{R_O}\right) = d(i_{in} - 2i_L - 2i_{C2}) = u \quad (27)$$

In these equations, R_O is the output resistance of the boost converter. Also, i_{in}, and u are the input current and output signals of a classic PI controller. Equation (27) indicates that the control signal of the controller has a direct relation with the value of the capacitor C_O and the values of the currents of the input source, inductors, and the capacitor C_2. By a simpler method, duty ratio that will be implemented to the power switch of the converter can be presented by (28):

$$d = \frac{u}{(i_{in} - 2i_L - 2i_{C2})} \quad (28)$$

Figure 6 presents the controller scheme of the proposed converter and is obtained according to (28).

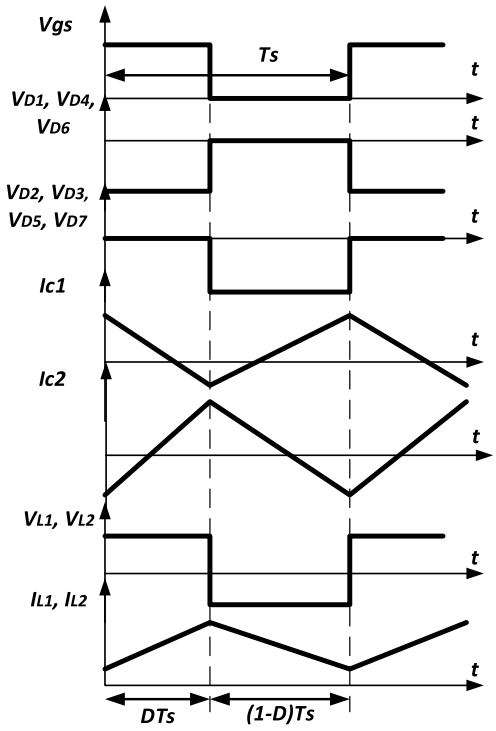


FIGURE 5. Voltage and current waveforms of the different components in proposed DC-DC boost converter.

The transform function of a PI controller $G(s)$, can be written by (29):

$$G(s) = k_p + \frac{k_i}{s} = \frac{k_p s + k_i}{s} \tag{29}$$

The closed-loop G_{C-L} function of the controller then can be written by:

$$G_{C-L} = \frac{G_o}{1+G_o} = \frac{\frac{1}{C_O}(k_p + k_i)}{s^2 + (\frac{1+Rk_p}{RC_O}) + \frac{k_i}{C_O}} \Rightarrow G_{C-L} = \frac{\frac{1}{C_O}(k_p s + k_i)}{s^2 + 2\xi\omega_0 s + \omega_o^2} \tag{30}$$

k_p and k_i are the proportional and integral coefficients of the PI controller and can be obtained as:

$$\begin{cases} \frac{1+Rk_p}{RC_2} = 2\xi\omega_0 \\ \frac{k_i}{C_2} = \omega_0^2 \end{cases} \Rightarrow \begin{cases} k_p = 2\xi\omega_0 C_2 - \frac{1}{R} \\ k_i = \omega_0^2 C_2 \end{cases} \tag{31}$$

In recent equation, ξ and ω_0 are the damping factor and frequency.

F. DCM ANALYSIS

To analyze the DCM working mode, all of the semiconductor devices should be considered in OFF-state. The reason is that, in DCM working mode, the currents of the inductors reach to zero and a voltage equal to zero can be measured across them. This state can occur after the second state in CCM. In this working mode that is not normally desired, the voltage

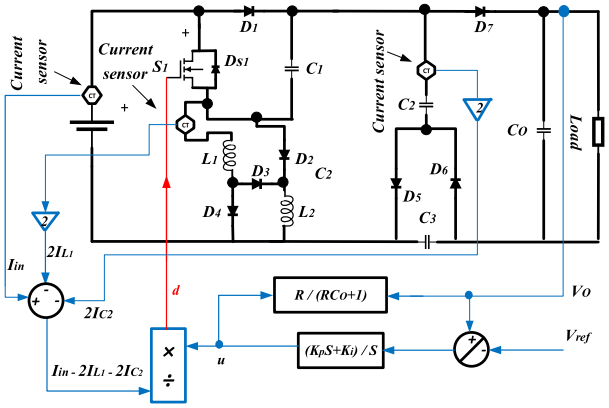


FIGURE 6. Controller design for the proposed boost converter.

for the capacitors is fixed. The currents of the inductors are important because for a boost converter, the load current is supplied by the inductors. Receiving the zero current in the inductors ($I_{L_{1,DCM}} = I_{L_{2,DCM}} = 0$) means the inability to supply the load and deliver the current and power to the load. Figure 7a presents the voltage and current waveforms for the inductors within a period in DCM, and figure 7(b) shows the state of the proposed converter for this operational mode.

Since the currents for the inductors reach zero, the diodes D_1 and D_4 go to off-state and no current can be established from the DC input source since the switch is in off-state. The current equations for the power diodes and the switch can be presented by the below equation:

$$I_{D_1} = I_{L_{1,DCM}} = 0 \tag{32}$$

The current of the inductor in this mode is shown by $I_{L_{1,DCM}}$. The currents of the diodes D_2 and D_3 are zero since these diodes are activated in CCM and when the switch is activated. Therefore, one can write:

$$I_{D_2} = 0 \tag{33}$$
$$I_{D_3} = 0 \tag{34}$$

The current for the diode D_4 is zero since this device is passing the current of the inductors:

$$I_{D_4} = I_{L_{1,DCM}} = I_{L_{2,DCM}} = 0 \tag{35}$$

By disconnecting the loop current from the input side and by having a zero current for the output diode D_7, the currents for the capacitors in the switched-capacitor block reach to zero. Therefor:

$$I_{D_5} = 0 \tag{36}$$
$$I_{D_6} = 0 \tag{37}$$
$$I_{D_7} = 0 \tag{38}$$
$$I_O = \frac{V_O}{R} \tag{39}$$

As mentioned, this state occurs after the second working station in CCM and in this mode the switch is deactivated.

The reflection of the diodes and the switch can easily show that the connection with the input source and the load will be disconnected and only the output capacitor exists to supply the load.

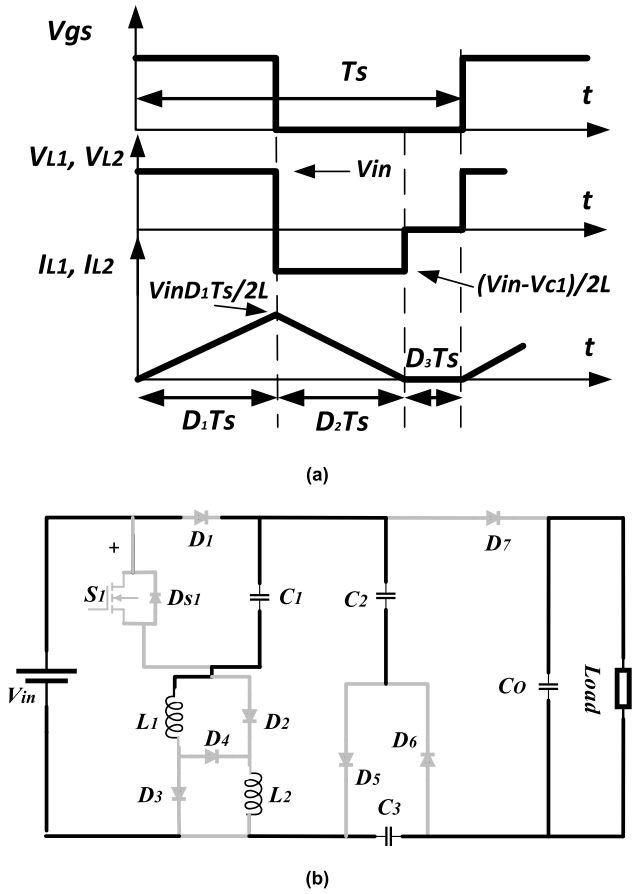


FIGURE 7. (a) Voltage and currents of the inductors in DCM working mode and (b) state of the proposed converter for DCM mode.

III. CALCULATION FOR COMPONENTS AND LOSSES, COMPARISON, AND DISCUSION

The components value in the circuit should be designed based on the working power value, and desired output voltage. Since the gain of the converter shows that it can present a voltage close to the 360 VDC at the output nodes by a 48 VDC input source, and in order to set up the circuit in the lab, a prototype with about 200 W, as the output power is analyzed. A simple calculation shows that a resistive load close to the 650 Ω should be considered and a current near to the 550 mA is expected. The components values are presented through the equations below.

A. INDUCTORS VALUES AND INPUT CURRENT CALCULATIONS

As mentioned, both inductors have the same value. For an acceptable current ripple for an inductor, a maximum variation of current ripples close to 40 percent is considered. Duty cycle $D = 0.5$, and switching frequency f = 50 kHz. Since the ripple is the same for both inductors, through the (9), and (11):

$$M_{CCM} = \frac{V_0}{V_i} = \frac{(3+D)}{(1-D)} \rightarrow \frac{I_0}{I_i} = \frac{(1-D)}{(3+D)} \quad (40)$$

$$\Delta i_{L1} = \Delta i_{L2} = \frac{1}{2}\Delta i_{in} \quad (41)$$

$$\Delta i_{L1} = \Delta i_{L2} = (0.3)\frac{(3+D)}{(1-D)} I_o = 1.115A \quad (42)$$

$$(\Delta i_L)_{closed} = \frac{V_{in}}{L} DT \rightarrow L = \frac{V_{in}}{\Delta i_L f} D = \frac{48}{1.115 \times 50000} \times 0.5 = 680\mu H \quad (43)$$

The inductor values can be shown by (43). (43) shows that for a larger switching frequency a smaller inductor can be used. On the other hand, for a limited ripple for the current, a larger inductor can be selected. Since this study plans to present the experimental test results, therefore, 50 kHz as a reliable frequency is chosen and the obtained inductor value is proper.

The configuration of the proposed converter shows that the input current is the same with the total currents of the inductors L_1, L_2 when the switch is activated and is equal with the currents of these inductors for time intervals that the switch is deactivated. (17) presents the average current of the inductors. For times the switch is in ON-state, by using the (11), the inductors are magnetized, and the input current is obtained as:

$$I_{in} = I_L + (\Delta i_L)_{closed} = \frac{V_{in}(1+D)}{(1-D)^2} + \frac{V_{in}}{L} DT \quad (44)$$

The input current for the time duration that the switch is deactivated by using the (13) is calculated as:

$$I_{in} = I_L + (\Delta i_L)_{open} = \frac{V_{in}(1+D)}{(1-D)^2} + \frac{V_{in} - V_{C1}}{2L}(1-D)T \quad (45)$$

Recent equations and the configuration of the inductors in the proposed converter show that the input current is the same as the inductors current and that the average current of the input source and each inductor is equal.

The minimum and maximum input currents can be presented through the (46) and (47):

$$I_{in,min} = I_L - \frac{\Delta i_L}{2} = \frac{V_{in}(1+D)}{(1-D)^2 R_O} - \frac{V_{in}}{2L} DT \quad (46)$$

$$I_{in,max} = I_L + \frac{\Delta i_L}{2} = \frac{V_{in}(1+D)}{(1-D)^2 R_O} + \frac{V_{in}}{2L} DT \quad (47)$$

By replacing the equations (40) into (46) and (47), the current stress for the input source can be found as:

$$\Delta i_{in} = \frac{V_{in}(1+D)}{V_O(1-D)^2} \quad (48)$$

A comparison between the input current stresses for the proposed converter and some of the presented similar converters by the research in recent years is presented in Table 2.

B. CAPACITORS VALUES

Equation (23) presents the relation between the output capacitor value and the voltage ripple. For a good converter, with a fixed output voltage, normally a ripple close to 1 percent is considered. Therefore, the output capacitor can be selected as:

$$\Delta V_O = \left(\frac{V_O}{R_O C_O}\right) DT = \frac{V_O}{R_O C_{Of}} \rightarrow C_O = \frac{V_O D}{R_O \Delta V_{Of}} = \frac{360 \times 0.5}{650 \times 3.6 \times 50K} = 1.53\mu F \quad (49)$$

This value shows that for a larger capacitor the output voltage will be more fixed. In practice, since many of the parasitic components are included in the account that normally in theoretical investigations are ignored, a larger ripple value is expected. For that, instead of the calculated capacitor value in (49), a larger one should be considered. For simulation and implementations, 220 μF is selected.

The values for the capacitors in SC-cell, the equation (50) can be presented:

$$C_2 = C_3 = \frac{I_o}{f_s \Delta_{V_o}} = \frac{0.55}{50k \times 3.6} = 3.5\mu F \quad (50)$$

In practice, 4.7 μF capacitors are selected since these are the standard values for the capacitors. For heavier loads, greater capacitor values should be considered. The capacitor C_1 acts as the output capacitor of the boost converter. Therefore, a same equation as is presented in the literature can be selected. A same equation has been presented in (51):

$$C_1 = \frac{D}{R_O(\Delta V_O/V_O)f} = \frac{0.5}{650 \times (0.01) \times 50k} = 1.53\mu F \quad (51)$$

As the same facts are mentioned for other devices, a larger capacitor should be considered. A Larger capacitor will fix the voltage for the SC-cell; therefore $C_1 = 10\mu F$ is selected. Table 1 presents all values for the elements.

TABLE 1. Components values.

Parameters	Values
Input voltage V_{in}	48 V
Output voltage V_o	360 V
Inductors L_1, L_2	680 μH
Capacitor C_o	220 μF
Capacitor C_1	10 μF
Capacitor C_2, C_3	4.7 μF
Switching frequency f_s	50 kHz

C. POWER LOSSES CALCULATIONS

The efficiency of the converter is obtained by dividing the output power over the input power. The power losses in a converter structure can be divided into dynamic and switching losses. Dynamic losses can be calculated for all semiconductor devices and passive elements since they can transfer the current in the circuit while switching losses occur only for power semiconductor devices including the switch and diodes. To find the dynamic losses, the root-mean-square (RMS) value of the currents for each element should be calculated.

1) POWER LOSSES CALCULATIONS FOR THE SWITCH

The relation between the input and output currents can be presented by through equation (40):

$$P_0 = P_{in} \rightarrow V_0 I_0 = V_{in} I_{in} \rightarrow I_{in} = \frac{(3+D)}{(1-D)} I_0 \quad (52)$$

The current of the switch is the same as the input source current:

$$I_S = I_{in} \, for \; 0 < t < DT \quad (53)$$

The RMS current for the switch can be presented by:

$$I_{S,rms} = \sqrt{\frac{1}{T}\int_0^{DT} (I_{in})^2 dt} = \sqrt{\frac{1}{T}\int_0^{DT} \left(\frac{(3+D)}{(1-D)} I_0\right)^2 dt} \quad (54)$$

Therefore, the dynamic power loss value for this element can be calculated through:

$$P_{S,dynamic} = r_{DS} {I_{S,rms}}^2 = r_{DS}\sqrt{D}\frac{(3+D)}{(1-D)} I_0 \quad (55)$$

In this equation, $P_{S,dynamic}$ and r_{DS} are the dynamic loss of the switch and the internal resistance between the drain and source pins of the switch, respectively.

The switching loss of switch can be presented by:

$$P_{S,switching} = f_s C_s V_s^2 = f_s C_s \left(\frac{Vo - Vin}{2}\right)^2 \quad (56)$$

In equation (56), $P_{S,switching}$, f_s, C_s, and V_s indicate the switching loss value, switching frequency, internal capacitor between drain-source pins and voltage stress across the switch. Therefore, the total power losses of the switch P_S, can be shown through:

$$P_S = P_{S,dynamic} + P_{S,switching} = r_{DS}\sqrt{D}\frac{(3+D)}{(1-D)} I_0 + f_s C_s \left(\frac{Vo - Vin}{2}\right)^2 \quad (57)$$

2) POWER LOSSES CALCULATIONS FOR THE DIODES

The real and RMS current for the diode D_1 are:

$$I_{D1} = I_{in} \, for \; DT < t < T \quad (58)$$

$$I_{D1,rms} = \sqrt{\frac{1}{T}\int_{DT}^{T} (I_{in})^2 dt} = \sqrt{\frac{1}{T}\int_{DT}^{T} \left(\frac{(3+D)}{(1-D)} I_0\right)^2 dt} \quad (59)$$

Therefore, the dynamic power loss can be calculated:

$$P_{D1,dynamic} = r_{DS} {I_{D1,rms}}^2 = r_{DS}\sqrt{1-D}\frac{(3+D)}{(1-D)} I_0 \quad (60)$$

The switching losses $P_{D1,switching}$ for this diode can be calculated as below:

$$P_{D1,switching} = V_{F_{D1}} Q_{rr_{D1}} f_s \quad (61)$$

$V_{F_{D1}}$, $Q_{rr_{D1}}$, and $V_{F_{D1}}$ are the dropped voltage across this diode in forward-biasing working situation, electrical charge

of the internal capacitor between anode-cathode pins and the switching frequency respectively.

The RMS and average current for the diodes D_2 to D_4 can be presented through below equations:

$$I_{D2,rms} = \sqrt{\frac{1}{T}\int_0^{DT} (I_{L_1})^2\, dt} = \sqrt{(I_{L_1})^2 D} = I_{L_1}\sqrt{D} \quad (62)$$

$$I_{D3,rms} = I_{D2,rms} \quad (63)$$

$$I_{D4,rms} = \sqrt{\frac{1}{T}\int_{DT}^{T} (I_{L_1})^2\, dt} = \sqrt{(I_{L_1})^2 (1-D)} = I_{L_1}\sqrt{1-D} \quad (64)$$

$$I_{D2,ave} = \frac{1}{T}\int_0^{DT} I_{L_1} dt = I_{L_1} D \quad (65)$$

$$I_{D3,ave} = I_{D2,ave} \quad (66)$$

$$I_{D4,ave} = \frac{1}{T}\int_0^{DT} I_{L_1} dt = I_{L_1}(1-D) \quad (67)$$

The power losses can be calculated for these diodes as below:

$$P_{D2,dynamic} = R_{F_{D2}} {I_{D2,rms}}^2 = R_{F_{D2}} (I_{L_1})^2 D \quad (68)$$

$$P_{D2,switching} = V_{F_{D2}} Q_{rr_{D2}} f_s \quad (69)$$

$$P_{D3,dynamic} = R_{F_{D3}} {I_{D3,rms}}^2 = R_{F_{D3}} (I_{L_1})^2 D \quad (70)$$

$$P_{D3,switching} = V_{F_{D3}} Q_{rr_{D3}} f_s \quad (71)$$

$$P_{D4,dynamic} = R_{F_{D4}} {I_{D4,rms}}^2 = R_{F_{D4}} (I_{L_1})^2 (1-D) \quad (72)$$

$$P_{D4,switching} = V_{F_{D4}} Q_{rr_{D4}} f_s \quad (73)$$

The RMS and average currents and power losses for the diodes D_5 and D_6 are as below:

$$I_{D5,rms} = \sqrt{\frac{1}{T}\int_0^{DT} (I_{C_2})^2\, dt} = \sqrt{(I_{C_2})^2 D} = I_{C_2}\sqrt{D} \quad (74)$$

$$I_{D6,rms} = \sqrt{\frac{1}{T}\int_{DT}^{T} (I_{C_2})^2\, dt} = \sqrt{(I_{C_2})^2 (1-D)} = I_{C_2}\sqrt{1-D} \quad (75)$$

$$I_{D5,ave} = \frac{1}{T}\int_0^{DT} I_{C_2} dt = I_{C_2} = I_{C_2} D \quad (76)$$

$$I_{D6,ave} = \frac{1}{T}\int_{DT}^{T} I_{C_2} dt = I_{C_2} = I_{C_2}(1-D) \quad (77)$$

$$P_{D5,dynamic} = R_{F_{D3}} {I_{D5,rms}}^2 = R_{F_{D3}} (I_{C_2})^2 D \quad (78)$$

$$P_{D6,dynamic} = R_{F_{D3}} {I_{D6,rms}}^2 = R_{F_{D3}} (I_{C_2})^2 (1-D) \quad (79)$$

$$P_{D5,switching} = V_{F_{D5}} Q_{rr_{D5}} f_s \quad (80)$$

$$P_{D6,switching} = V_{F_{D5}} Q_{rr_{D5}} f_s \quad (81)$$

The voltage across the anode-cathode pins of the diode V_{D7} and current of this diode are equal to:

$$V_{F_{D7}} = \frac{Vo}{(\frac{3+D}{1-D})} = \frac{1-D}{3+D} Vo \quad (82)$$

$$I_{D7} = I_O \; for \; 0 < t < T \quad (83)$$

The RMS and average currents for this diode can be obtained through equations (84) and (85):

$$I_{D7,rms} = \sqrt{\frac{1}{T}\int_0^{DT} (I_O)^2\, dt} = \sqrt{(I_O)^2 D} = I_O\sqrt{D} \quad (84)$$

$$I_{D7,ave} = \frac{1}{T}\int_0^{DT} I_O dt = I_O D \quad (85)$$

Therefore, the losses for this diode can be presented by:

$$P_{D7,dynamic} = R_{F_{D7}} {I_{D7,rms}}^2 = R_{F_{D7}} (I_O)^2 D \quad (86)$$

$$P_{D7,switching} = V_{F_{D7}} Q_{rr_{D7}} f_s \quad (87)$$

3) POWER LOSSES CALCULATIONS FOR THE INDUCTORS AND CAPACITORS

To find dynamic power losses for passive elements, the internal resistance of these components should be multiplied by the square of the RMS current of the components:

$$i_{L1,\,and\,L2} = \frac{I_{in}}{2} \; for \; 0 < t < DT \quad (88)$$

$$i_{rms,L1,\,and\,L2} = \frac{(3+D)}{(1-D)} I_0 \quad (89)$$

$$P_{L1,L2,dynamic} = R_{L_{1,2}} {I_{rms,L1,\,and\,L2}}^2 = R_{L_{1,2}} (\frac{(3+D)}{(1-D)} I_0)^2 \quad (90)$$

In recent equations, $P_{L1,L2,dynamic}$, $R_{L_{1,2}}$, and $i_{rms,L1,\,and\,L2}$ are the dynamic losses of the inductors L_1 and L_2, internal resistance and RMS current of these inductors respectively.

The losses for capacitors generally can be calculated through equation (91):

$$P_{Cx,dynamic} = R_{C_x} {I_{rms,Cx}}^2 \quad (91)$$

In (91), R_{C_x} and ${I_{rms,Cx}}^2$ show the internal resistance of any of the capacitors and RMS value of the currents for these capacitors, respectively.

Total power losses can be presented by:

$$\begin{aligned} P_{Loss} = {} & P_S + P_{D_1-D_7} + P_{L_1,L_2} + P_{C_1-C_O} = P_{S,dynamic} \\ & + P_{S,switching} + \sum_{a=1}^{7} P_{Da,dynamic} \\ & + \sum_{b=1}^{7} P_{Db,switching} + P_{L1,L2,dynamic} \\ & + \sum_{x=1}^{4} P_{Cx,dynamic} \end{aligned} \quad (92)$$

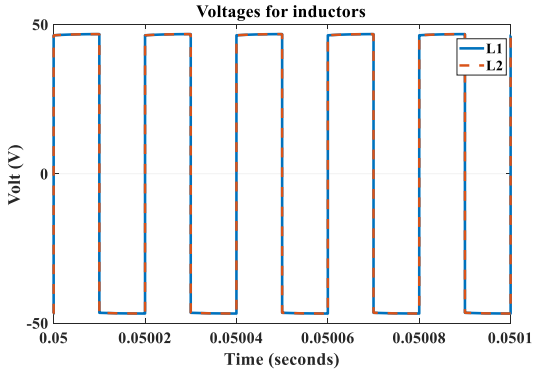
The efficiency equation can be shown through:

$$\eta = \frac{P_o}{P_{in}} = \frac{P_o}{P_o - P_{Loss}} \quad (93)$$

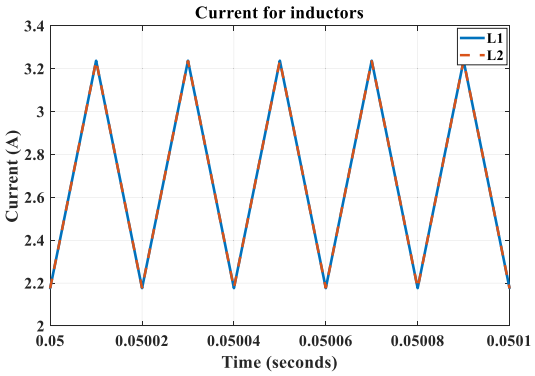
D. SIMULATION RESULTS

A group of the simulations have been done for the proposed converter. Figures 8 to 11 show the results. In figure 8, the reaction of the inductors in SL-cell is investigated. The voltage across the inductors is reported in figure 8a and the currents of the inductors can be seen in figure 8b. These figures have been obtained for the elements in Table 1.

To verify the performance of the proposed converter, the circuit is tested under different working conditions.



(a)



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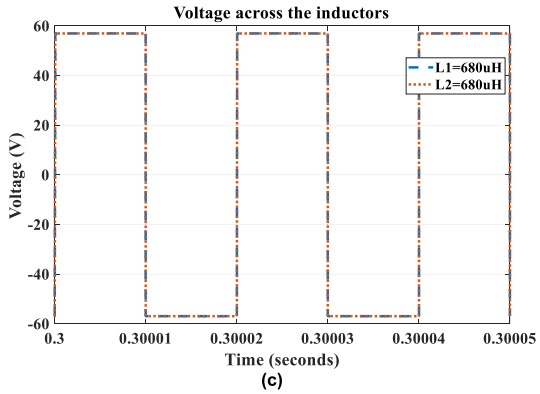
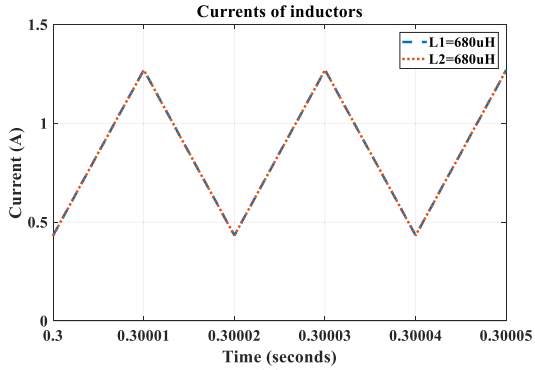


(c)



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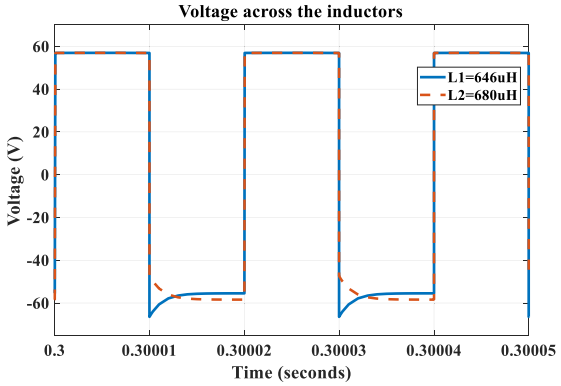

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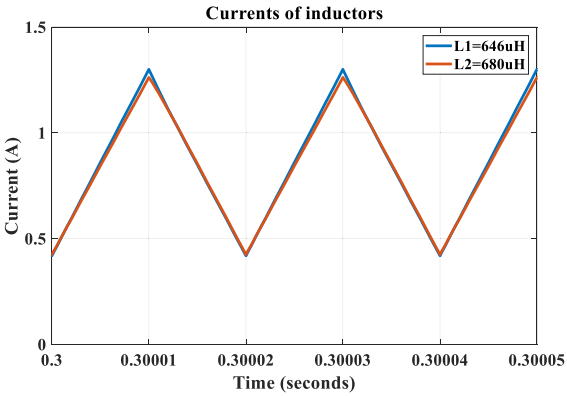
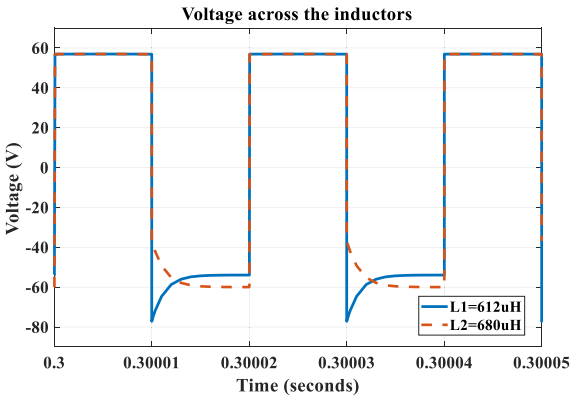
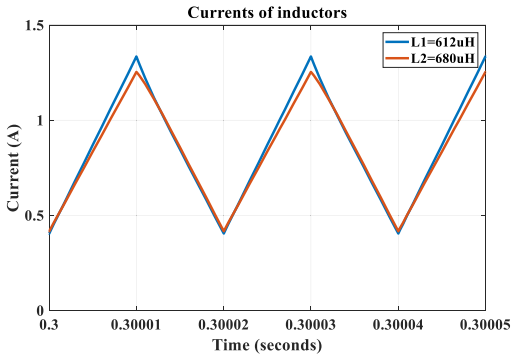


(f)



(g)



(h)

FIGURE 8. (a) The voltage and (b) the currents of the inductors in SL-cell. The state of the inductors voltages and currents when the inductors are (c) and (d) $L_1 = L_2 = 680\mu H$, (e) and (f) $L_1 = 646\mu H$, $L_2 = 680\mu H$, and (g) and (h) $L_1 = 612\mu H$, $L_2 = 680\mu H$.

For example, the voltage and currents of the inductors are obtained with different values of the inductors. The values of the inductors are considered to be the same. In practice, it is hard to prepare similar inductors, and tolerances of about a maximum of 5 percent can be accepted. Figures 8(c), (d), (e), (f), (g) and (h) present the voltage and current for the inductors with the same values, 5 percent differences, and 10 percent differences in values, respectively. As can be seen, an ignorable difference for the current and almost the same voltage waveforms can be obtained, and it does not degrade the performance of the circuit much.

Since the same values of the inductors are used, and both inductors are magnetized and demagnetized simultaneously, the voltage and current of the inductors are the same. For a 200 W prototype circuit, with 48 VDC and 360 VDC as the input and output voltages, a positive and negative voltage with 50 V magnitude and a ripple in current equal to 1 A are reported. A resistive load closed to 650 Ω is considered for the simulations and this means that a current equal to 0.55 A is expected at the output load. Figures 9(a) and (b) show the input and output voltages and currents, respectively. Results show that all desired voltage and current values for the output side are obtained.

Figure 9b shows that an average current close to 4.25 A is presented by the source. Also, the reaction of the converter under variable loads should be considered. For that, figure 9(c) is presented to show the performance of the converter in generating the different load currents for different load values. For example, for a load equal to 580 Ω, with about 360 VDC, a current close to 615 mA is obtained. At times $t = 0.1$, and $t = 0.2$, the second and third loads are involved at the output side. These loads are the same as the first load; therefore, an enhancement for the output current is expected at these times. Figure 9(c) shows that the load current increases to 1.230 A and 1.84 A, respectively at times $t = 0.1$, and $t = 0.2$.

In figure 10a, the currents of the power switch and the diode D1 are presented. An average current equal to 3.5 A and 0.75 A pass through the switch and diode D1 respectively. A total of both these currents follows from the input source and can be seen in figure 9(b). The voltage across the drain-source pins of the switch is seen in figure 10b. This figure reports a maximum voltage stress close to 140 V for this switch at the 360 VDC of the output voltage. Figure 11 presents the voltage across the diodes. This figure shows that when the switch is activated, diodes D2, D3, D5, and D7 are in ON-state, and for the time intervals that the switch is deactivated, diodes D1, and D6 are in ON-state respectively. The correctness of figure 5 can be proved through this figure. The voltage states of the diodes D1, D2, and D3 are shown in figure 11(a) and the voltage waveforms for the diodes D5, D6 and D7 can be seen in figure 11(b).

E. COMPARISON

To evaluate the performance of the proposed converter, a group of the SC and SL-based boost converters were

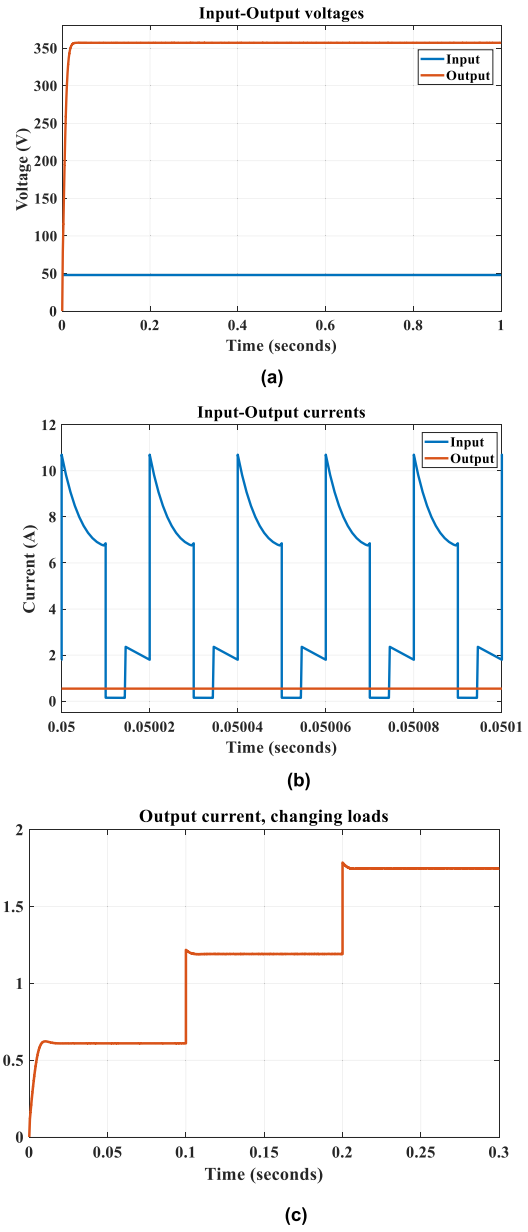


FIGURE 9. The input-output (a) voltages, and (b) currents. (c) State of the output current for variable loads.

considered, and the results of the comparison are presented in Table 2. For the comparison, the number of the inductors, capacitors, diodes and switches and the voltage stress across the main switch and the gain of the proposed converters are examined. Based on the results, the converter in [31] has the most number of the inductors, and converters in [33], [36], and [37] include the most number of the capacitors. The proposed converter with the circuits in [33], [35], and [39] include only one power switch that is a proper feature for having a simpler controller circuit. However, the proposed converter and converter in [37] include the most number of the power diodes.

Figure 12 illustrates the voltage gain curves for the converters in Table 2. This figure shows that the gain of the

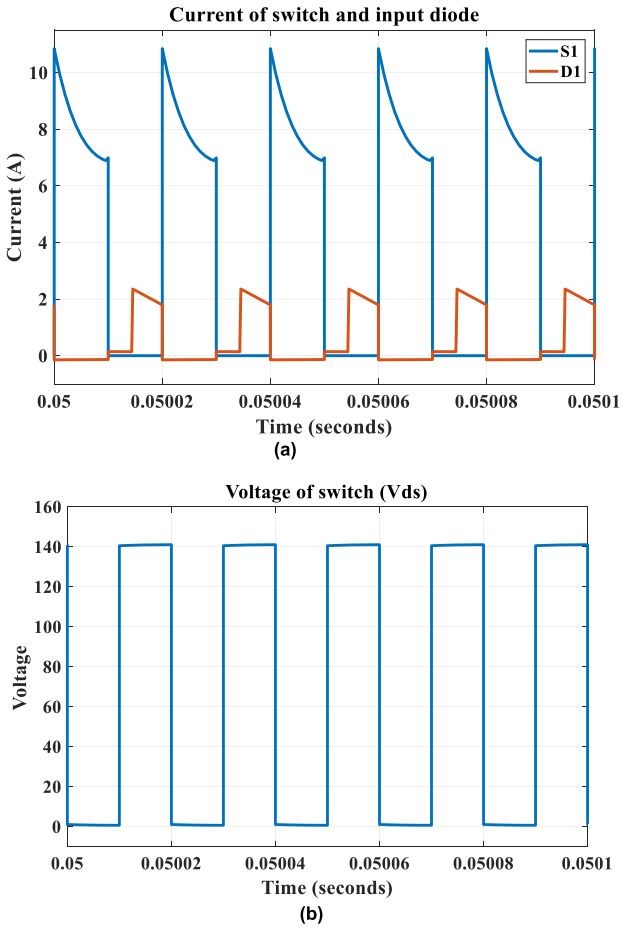


FIGURE 10. (a) The currents of the switch and input diode, D1, and (b) the voltage across the drain-source pins of the switch.

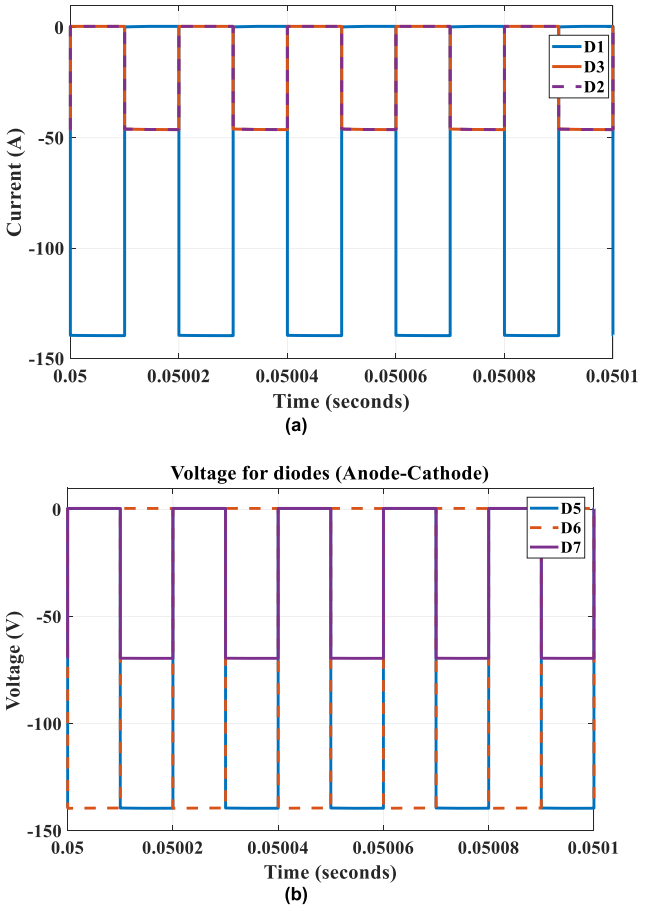


FIGURE 11. The voltages across the power diodes (a) D1, D2, and D3, and (b) D5, D6, D7.

proposed converter in all duty ratios, is greater than converters in [30]–[33] and [35]. The converter in [34] has the most values of the voltage gain and is closed to the gain of the proposed converter in this study. Converters in [36] and [37] act as the voltage multiplier circuits and enhance the input voltage through a fixed switching frequency and duty ratio. Therefore, in figure 12, the gain of these converters is drawn fixed for all duty ratios. Circuit in [36] increases the input voltage by 6 times and converter in [37] enhances the source voltage by 4 times, respectively. Also, the voltage stress curves for the converters in Table 2 are presented in figure 13. Where the converter in [35] presents a stress closed to the output voltage, other converters present smaller voltages and the best results can be obtained for the converters in [34], [33] and proposed converters respectively. The numbers in the vertical axis should be multiplied to the output voltage at the same duty ratio to find the expected voltage magnitude.

Figure 14 shows the voltage stress across the output power diode. Results show that the maximum voltage stresses are reported for converters in [30]–[32], the middle stresses are belonging to the converters in [33] and [34] and the least stress is seen for the proposed converter.

Figure 15 presents the input current stress for the proposed converter in comparison with some of the configurations in Table 2. Although in this table, the current stress equations are presented for the majority of the proposed topologies, since some of these equations are related to parameters such the switching times or current ripples in inductors that can be shown difficultly, the current of the topologies in [30] and [38] are shown. This figure shows the current ripple for duty ratios between 0.5 to 0.6, and as can be seen, the current stress is obtained between the ripples for converters in [30] and [38]. This shows that the proposed converter can guarantee a reliable range for the current fluctuations at the input source side.

IV. EXPERIMENTAL RESULTS

This section presents some of the results for hardware tests. For that, a 200 W converter circuit was established in the laboratory according to the elements value of the theoretical investigations and the simulation. A resistive load equal to 650 Ω is considered, and an output voltage close to 360 VDC is considered to be obtained for this load. The switching frequency is adjusted at the 50 kHz and the FQP34N20 type of the MOSFET is selected for the switch. This transistor has

TABLE 2. Comparison for the proposed and similar SC and SL-based boost converters.

Converter	Gain	No. of inductors	No. of capacitors	No. of diodes	No. of switches	Voltage stress for output diode	Voltage stress for main switch	Input current stresses	Efficiency in 200 W
[30]	$\frac{3D+1}{1-D}$	3	1	4	2	GVi	$\frac{2G+1}{3}$	$I_{in,max} = 2\frac{V_{in}}{L}DT$ $I_{in,min} = \frac{V_O - V_{in}}{4L}(1 - D)T$	95.5
[31]	$\frac{1}{1-D}$	4	3	4	4	GVi	Vo	$I_{in,max} - I_{in,min} = \frac{V_{in}(t_{10}-t_4)}{L_{1a}}$	92
[32]	$\frac{2}{1-D}$	2	3	4	2	GVi	$\frac{Vo}{2}$	$I_{in,ave} = \frac{VinD}{2\Delta i_L f}$	95
[33]	$\frac{2+D}{1-D}$	2	5	4	1	---	$\frac{Vo}{2+D}$	-----	95
[34]	$\frac{2(n+1)}{1-D}$	2	3	2	4	$\frac{2n+1}{2(n+1)}Vo$	$\frac{Vo}{2(n+1)}$	-----	96,2
[35]	$\frac{1+D}{1-D}$	2	1	4	1	----	Vo	-----	---
[36]	$Vomax = 6Vin$	3	5	5	5	----	Vin	-----	92
[37]	$Vomax = 4Vin$	3	5	6	6	$Vo - Vin$	$n \times Vin$	-----	94,8
[38]	$\frac{1+D}{1-D}$	2	1	3	2	Vo	$\frac{Vo}{2G}$	$\Delta i_{in} = 2\frac{VinD}{Lf} - \frac{V_O - V_{in}}{2L}(1 - D)T$	96
[39] – Type 2	$\frac{2-D}{1-2D}$	2	4	3	1	Vo	----	$\Delta i_{in} = \frac{Vin(1-D)D}{Lf(1-2D)}$	< 90
Proposed	$\frac{3+D}{1-D}$	2	4	7	1	$\frac{Vo}{G}$	$\frac{Vo - Vin}{2}$	$\frac{V_{in}(1+D)}{(1-D)^2}$	96

35 mΩ between drain and source pins for the short-circuit working condition. Also, the FRD type with IN5402 number is chosen for all power diodes. The dynamic resistance for this type of the power diode is equal to 12 mΩ. The forward voltage for this diode based on the datasheet is equal to 1.2 V.

Figure 16a presents the implemented prototype circuit for the proposed converter. Figure 16b shows the input and output currents of the converter. By the measured results, the output current is a DC current with 550 mA magnitude. Input side current is divided between the switch and D1, and as mentioned in sections 2 and 3, around 4 A for the average current for the source side is expected. In test results, at the duty cycle, close to 50 percent at the Fs = 50 kHz, the expected current is obtained. Figure 16(c) shows the state of

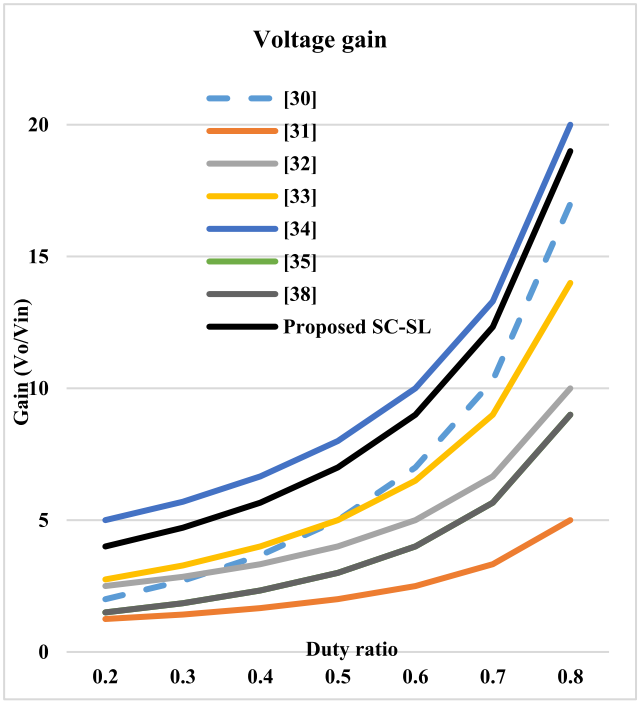


FIGURE 12. The voltages gain curves for the proposed and other converters.

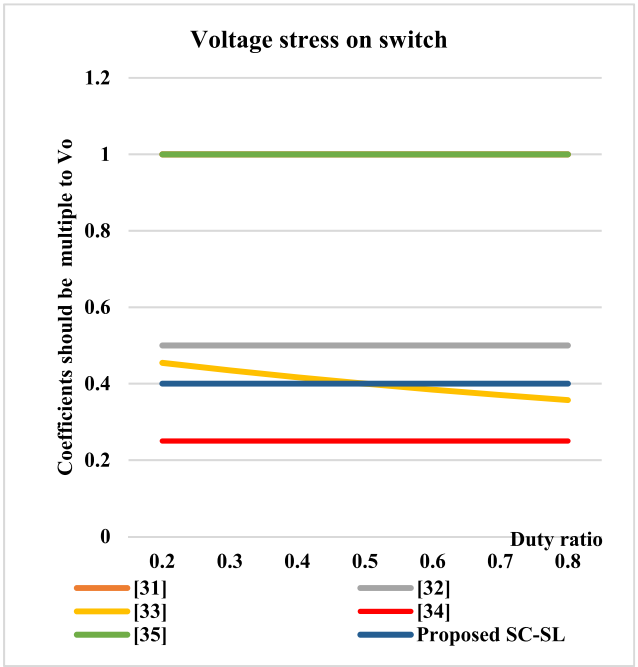


FIGURE 13. The voltages stress curves on main power switches for the proposed and other converters.

the power switch and illustrates that a voltage near to 140 V drops across the drain-source pins with a current ripple from zero to 8A. An average current close to 4A is obtained. The frequency and duty ratio of these waveforms, as can be seen, are the same as the desired values.

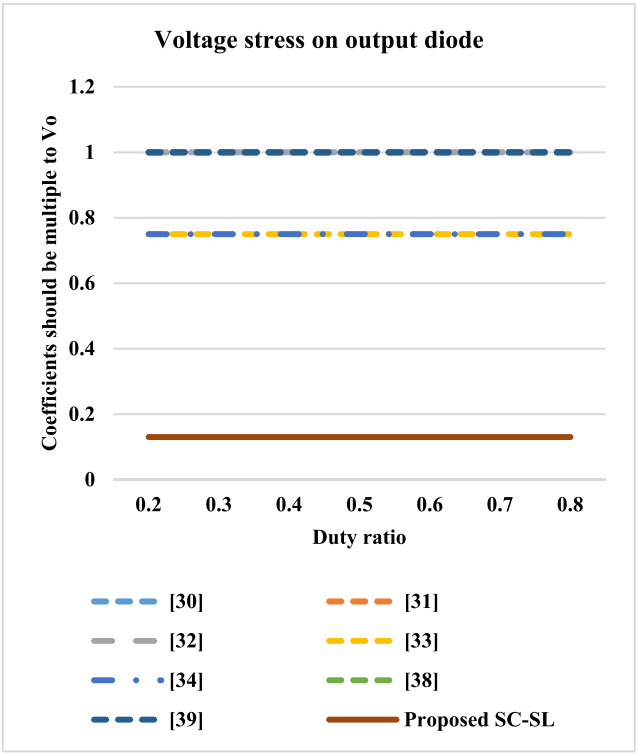


FIGURE 14. The voltages stress curves on output diode for the proposed and other converters.

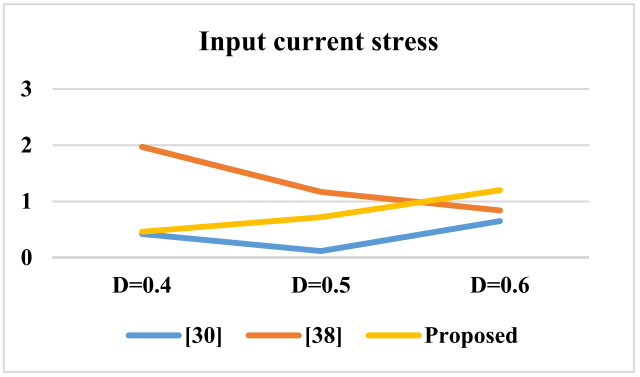
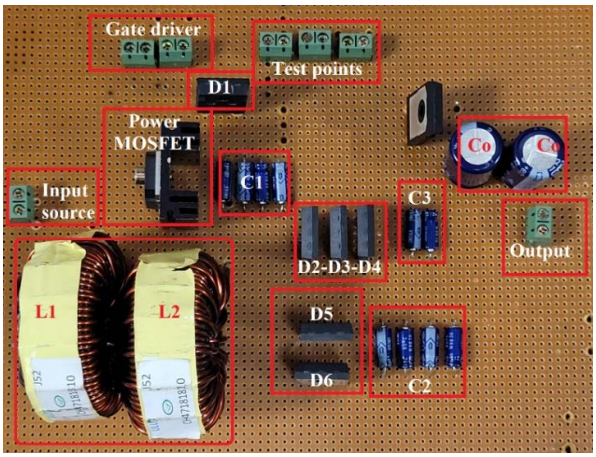
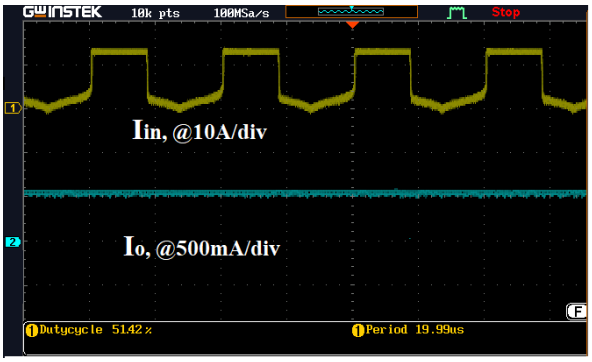


FIGURE 15. The voltages stress curves on output diode for the proposed and other converters.

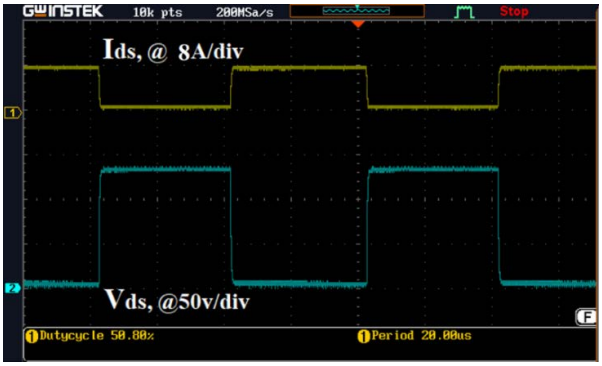
The current waveforms and voltage drop across the inductors are similar and can be seen in figure 16(d). A voltage with peak to peak 120 V is obtained and a current with maximum 3.2 A and minimum around 2 A is reported. These results have a proper overlap with the simulation results since approximately the same current is obtained and about 20 V more than the simulation results for the inductors voltages are reported. This can be because of the internal resistance of the inductors that was not considered for the theoretical analysis and also for the simulation tests. Figure 16(e) presents the voltage across the diodes D2 and D3. These two diodes are in series with the inductors and are activated and deactivated simultaneously.



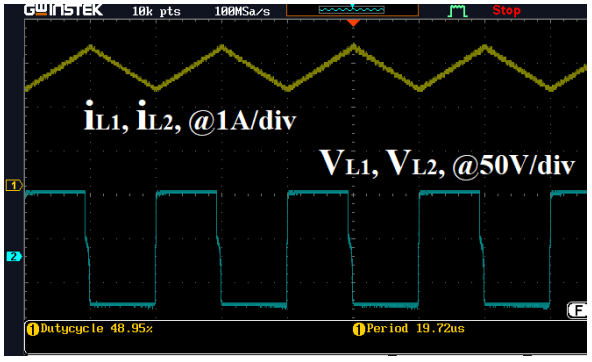
(a)



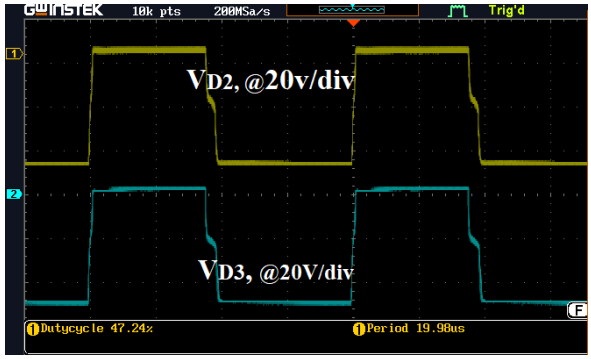
(b)



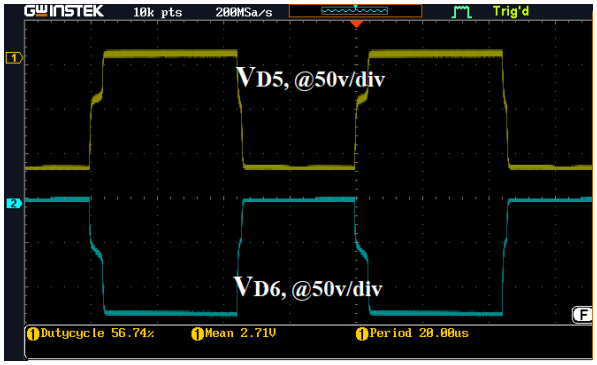
(c)



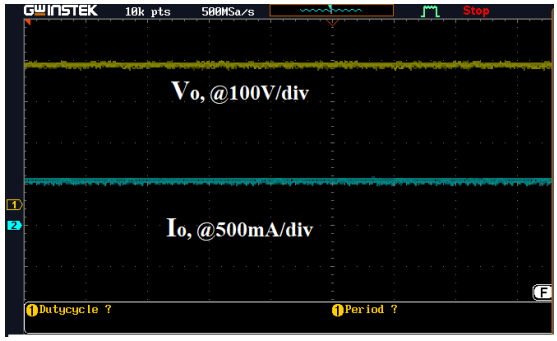
(d)



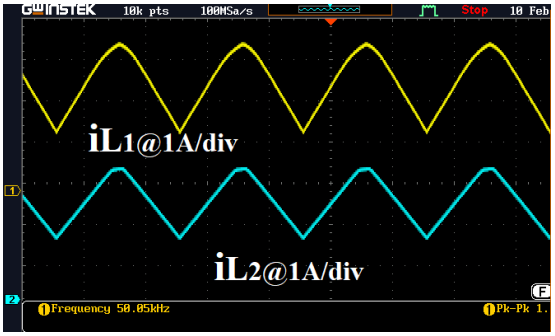
(e)



(f)

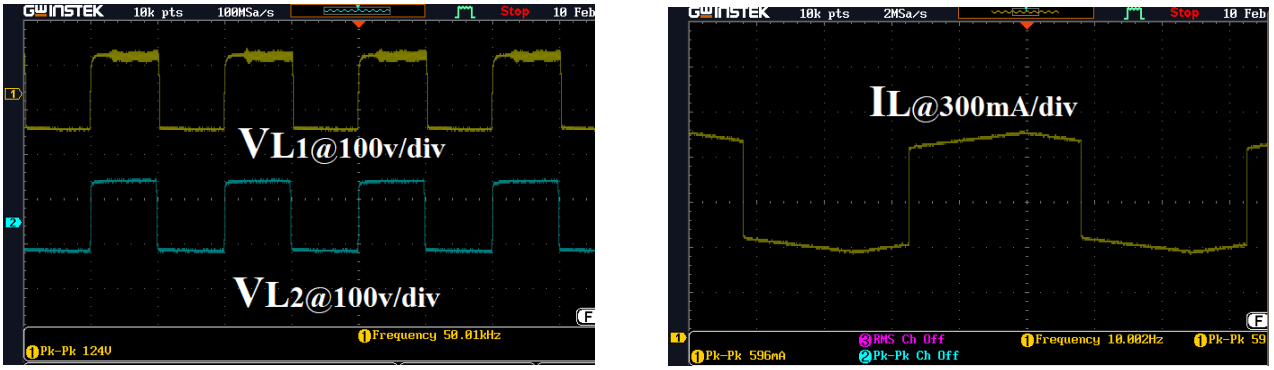


(g)



(h)

FIGURE 16. (a) The implemented prototype converter, (b) Input and output currents, (c) Voltage and currents for the switch, (d) Voltage and currents of the inductors L_1 and L_2 (the same voltage and currents), (e) Voltages for diodes D2 and D3, (f) Voltages for diodes D5 and D6, (g) Output voltage and current, (h) inductors currents for heavier loads (500Ω).



(i) (j)

FIGURE 16. *(Continued.)* **(i) inductors voltages for heavier loads (500Ω), and (j) output current (I_L) for different load values.**

To show the reaction of the diodes in SC-cells figure 16(f) is presented. According to the simulation results, these diodes are in ON and OFF-states asynchronously and for any time interval only one of these diodes is activated. Results show that a voltage with a maximum 50 V peak to peak is obtained. By considering that the diodes and capacitors in the SC-cell are the same, the voltages across these devices also should be the same. Figure 16(f) shows that the diodes work alternatively and voltages across the anode-cathode pins are the same. Figure 16(g) is one of the most important figures and shows the output voltage and current. Where theoretically a voltage with 360 VDC amplitude and a current equal to 550 mA are expected, 350 VDC as the voltage and 500 mA as the current are obtained. This overlap for the voltage and current can be categorized the converter between the proper topologies as there are expected results.

Figures 16(h) and 16(i) present the currents and voltages for the inductors under a heavier load. The currents for these inductors and the voltage across them are important, since in practice, generating similar inductors is not easy. But they can be made by acceptable tolerance values. As can be seen, by these figures, similar currents and voltages can be obtained. The switched-inductor part of the circuit is working synchronously since, by inductors with close values, similar results are predicted. Figure 16(j) illustrates the capability of the converter on the output side when the loads are changing. Two similar 580 Ω resistive loads through a breaker are connected at the output side and the ability of the converter for presenting the necessary currents for these loads is investigated. This figure shows that the output current approximately doubles when the second load is applied. The current in this figure is shown with I_L and means the current of the load. This is different from inductors currents that are indicated by I_{L1} or I_{L2}.

Figure 17 presents the efficiency diagram for the converters in Table 2. For that, the efficiency of the converters for power values from zero to 200 W is read. Also, the efficiency curve for the proposed converter is added. According to the results of this figure, the converters in [30], [34], and [35] present the maximum efficiencies for powers less than 125 W. After this power value, the proposed converter with converters in [30] and [34] present the highest efficiencies. The converters in [35] and [38] are suitable for low-power applications and the efficiency of the converter in [36] for higher power values is grater and makes the converter proper for high-power applications. For drawing the figure, the authors tried to present curves with the closest input voltages and working conditions for all of the converters for a fair comparison. The efficiency of the proposed converters is more than 90 percent for all output power values and can present higher efficiencies for higher power values. For powers below 150 W, this converter can present higher efficiencies in comparison with a large part of these converters, and for powers more than 150 W, it can present the highest efficiency. This property is important since it can prepare the converter for high-power applications.

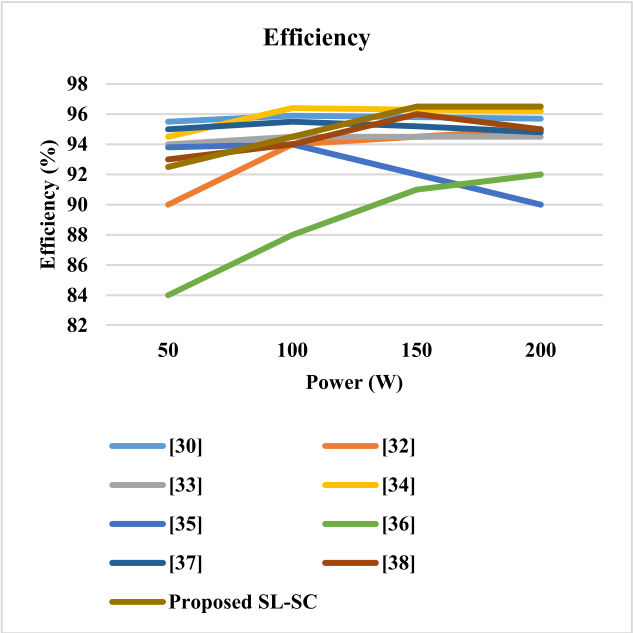


FIGURE 17. **Efficiency of the converters in Table 2 and proposed converter.**

Figure 18 presents the efficiency diagram for the proposed converter with different input voltages and 360 VDC as the fixed output voltage for output power of 200 W. As was

predictable, with an enhancement in input voltage, the converter acts more efficient, and this is because of fewer differences between the input and output voltages. For fewer input voltages, longer duty cycles are needed to be applied to the switch and diodes, and since the semiconductors have most of the losses, efficiency is less.

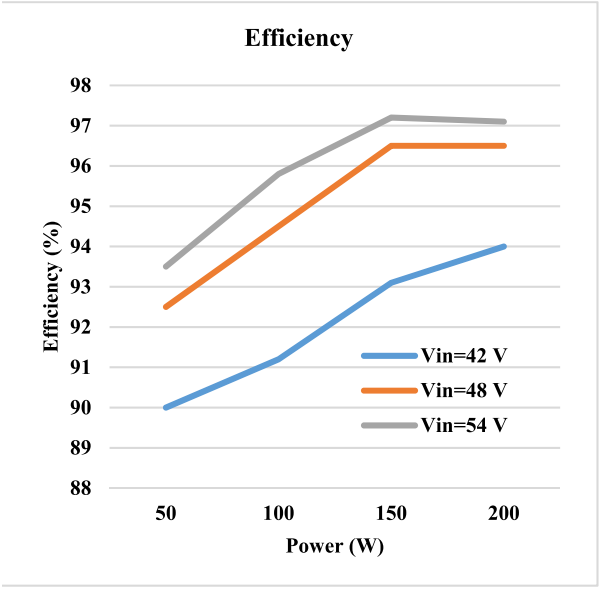


FIGURE 18. The efficiency of the converter for different input voltages for P = 200 W.

V. CONCLUSION

A boost converter with a switched-inductor and a switched-capacitor topology is presented in this study. By adding an inductor to the conventional boost converter and replacing the locations of the inductors, transistor and diode, a new configuration for the proposed boost converter is presented. The most important feature of this configuration is enhancing the input voltage with more gain ($(1 + D)$ times greater) and decreasing the input current ripple in comparison with the classic boost converters. All these specifications will be gained only by an extra inductor and three power diodes for the SL configuration. Since diodes are used instead of the transistors on the SL-side, there is no need for the control circuit. For the next step, the proposed SC-cell is introduced with a simple configuration including two capacitors and two diodes. This block enhances the voltage at the output of the converter, since for the duty ratio closed to 0.5, a voltage equal to 7.5 times greater than the input voltage is obtained. Also, with the proposed SC-cell for the duty ratio closed to 0.8, approximately 19 times greater than the input voltage is obtained. Since working under the greater duty ratios can lose more power because of the longer time to pass current for obtaining more gains, by considering that the SC-cell has only four devices, a cascaded configuration can be considered for receiving high efficiencies. This configuration is suitable for grid integration Photovoltaic (PV) applications since the generated voltages of the PV arrays are limited and need to be enhanced. A large part of the voltages and currents of the converter components are reported theoretically, in simulation and practically. A laboratory-scaled 200 W prototype is presented and confirms the theoretical results.

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