IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received December 15, 2020, accepted January 7, 2021, date of publication January 12, 2021, date of current version January 22, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3051039

A Novel Asymmetrical 21-Level Inverter for Solar PV Energy System With Reduced Switch Count

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This work was supported by the Danida Mobility Grant, under Project 19-MG06AAU responsible for the Ministry of Foreign Affairs of Denmark (MFA), Act 7 on Denmark's International Development Cooperation.

ABSTRACT This article presents a novel asymmetrical 21-level multilevel inverter topology for solar PV application. The proposed topology achieves 21-level output voltage without H-bridge using asymmetric DC sources. This reduces the devices, cost and size. The PV standalone system needs a constant DC voltage magnitude from the solar panels, maximum power point tracking (MPPT) technique used for getting a stable output by using perturb and observe (P&O) algorithm. The PV voltage is boosted over the DC link voltage using a three-level DC-DC boost converter interfaced in between the solar panels and the inverter. The inverter is tested experimentally with various combinational loads and under dynamic load variations with sudden load disturbances. Total standing voltage with a cost function for the proposed MLI is calculated and compared with multiple topologies published recently and found to be cost-effective. A detailed comparison is made in terms of switches count, and sources count, gate driver boards, the number of diodes and capacitor count and component count level factor with the same and other levels of multilevel inverter and found to be the proposed topology is helpful in terms of its less TSV value, devices count, efficient and cost-effective. In both simulation and experimental results, total harmonic distortion (THD) is observed to be the same and is lower than 5% which is under IEEE standards. A hardware prototype is implemented in the laboratory and verified experimentally under dynamic load variations, whereas the simulations are done in MATLAB/Simulink.

INDEX TERMS Multilevel inverter, photovoltaic (PV) system, maximum power point tracking (MPPT), cost function (CF), TSV calculation, total harmonic distortion (THD).

NOMENCLATURE

V_0	Output voltage
I_0	Output Current
I_{PV}	Photovoltaic module current
V_{PV}	Photovoltaic module voltage
P_{PV}	Photovoltaic module power
D	Duty cycle
$MPPT$	Maximum power point tracking
$P\&O$	Perturb and observe
THD	Total harmonic distortion
TSV	Total standing voltage
CF	Cost function
CF/l	Cost function per level count
TSV_{pu}	Total standing voltage per unit
C_1, C_2	DC capacitors
P_{sw}	Switching losses
P_{cl}	Conduction losses
P_{out}	Output power
P_{in}	Input power
V_{OC}	Open-circuit voltage
I_{SC}	Short-circuit current
I_D	Diode saturation current
V_{MPP}	Voltage at maximum power point

The associate editor coordinating the review of this manuscript and approving it for publication was Eklas Hossain.

I_{MPP}	Current at maximum power point
V_{OK-STM}	Open-circuited voltage at the standard testing case
I_{SK-STM}	Short-circuited current at the standard testing case
V_{Suni}	Voltage stress on unidirectional switch
V_{Sbi}	Voltage stress on bidirectional switch
α	Weight coefficient
E_{on}, E_{off}	Energy utilization of switches
STM	Standard testing measurement
R_S, R_{SH}	Series and shunt resistances
K	Boltzman constant
T	Temperature

I. INTRODUCTION

The attempt to use renewable energy sources motivates the rapid increase of greenhouse emissions and fuel costs [1], which causes air pollution and climate change in the long term [2]. Amid various sustainable energy sources, solar energy is elegant with zero emissions, with which the electricity conversion is made easy with the photovoltaic (PV) system [3]. It became a common source of electricity for both domestic and industrial consumers [4]. This includes various applications in solar electric vehicles, vehicle charging stations, a good deal of water pumping systems, and standalone systems for the areas where there is a lack of reliable grid access [5]–[7].

The photovoltaic power generation comprises solar PV panels, where the output of a solar panel is fed to DC link through a DC-DC converter. The voltage from a DC link is provided to the DC-AC inverter and to load [8]. The output of solar PV is not constant, and it changes according to the solar irradiation and temperature [9]. Therefore, for an efficient operation of PV panel even under various climatic changes in an annual calculation, it is essential to extract maximum power from the PV module, admitted to being Maximum power point tracking (MPPT) [10]. Whenever the MPPT exists in a system, the DC-DC converter plays a significant role in handling maximum power as it works with the duty cycle change [11]. Using MPPT in PV system increases the efficiency and life-span of a solar module [12].

Based on the essential requirement of DC-AC inverter in a solar PV system, rather than the conventional inverters like voltage source inverter, multilevel inverter (MLI) has opted in the present scenario where it is efficient in capable of obtaining the quality of power with significantly less error [13]. The current multilevel inverter topologies comprise a smaller number of components used in the circuit compared with the conventional inverters such as flying capacitor type (FC) [14], cascaded H-bridge type (CHB) [15] and the neutral point clamped type (NPC) [16]. The number of components in the circuit is directly proportional to the number of levels in MLI, which increases cost and complex structure [17]. In both the FC MLI and NPC MLI, the capacitor voltage balancing is a challenging task with which these are limited to five-level and unable to cascade. This lowers the output voltage to half of the input voltage, providing high switching frequency with more losses [19]. A wide range of research is reducing the components of MLI, and several topologies are proposed based on the various levels which are having their challenges [20], [21].

Multilevel inverters are divided into isolated and non-isolated. Isolated inverters are designed with external DC sources, whereas non-isolated inverters are designed with a single source [17]. Further, Isolated inverters are divided into symmetrical and asymmetrical configurations. Each DC source has an equal value known to be a symmetrical configuration, while different values of DC sources make up the asymmetrical design of MLI with trinary or binary techniques [18]. There are many such topologies which work for both configurations proposed in [23]. Specifically, for a photovoltaic power generation under low and medium rated applications, the asymmetrical configuration is preferred, where the optimization of PV modules can be done quickly. In opting for the suitability among isolated and non-isolated structures, isolated MLI is optimal towards PV integration. In contrast, the non-isolated MLI like FC and NPC, the balancing of voltage is a challenging task [24].

For a PV fed inverter, in producing a stable DC voltage, there is a need for a control technique. A typical PI controller realized in the standalone PV system to select a proper duty cycle of the DC-DC converter by comparing the converter output with reference [25]. It is not desirable to have control over the DC-DC converter with the MPPT technique and hence various topologies are proposed to solve this issue for the standalone solar system. In the recent past, several advanced techniques like artificial intelligence (AI), practical swarm optimization (PSO), fuzzy and genetic algorithm (GA) to have an auto-control regarding the training data to regulate voltage [26]. The selection of the MPPT technique for a suitable application is an astonishing task where every method is having its own merits and demerits [27]. For example, hill climbing (HC), perturb, and observing (P&O) and are widely used MPPT methods because of its simple implementation. Under partial shading conditions, the conventional methods like fuzzy, P&O, INC algorithms cannot extract global MPP (GMPP) [28]. Many works of literature have been implemented MLI with DC link with MPPT, where the control of outputs can be done by the load [29] or under steady solar irradiance [30]. MPPT consistently changes the energy of the solar panel to operate at the maximum point of the power which depends on temperature, load, and solar irradiance. Both solar irradiance and temperature change during day time for climatic conditions and depending on the season. So, it is very important to track all these parameters and get maximum power point.

In this article, a standalone PV system is implemented using a 21-level multilevel inverter integrated with a three-level DC-DC boost converter is presented. P&O powered MPPT technique is implemented in the proposed system to

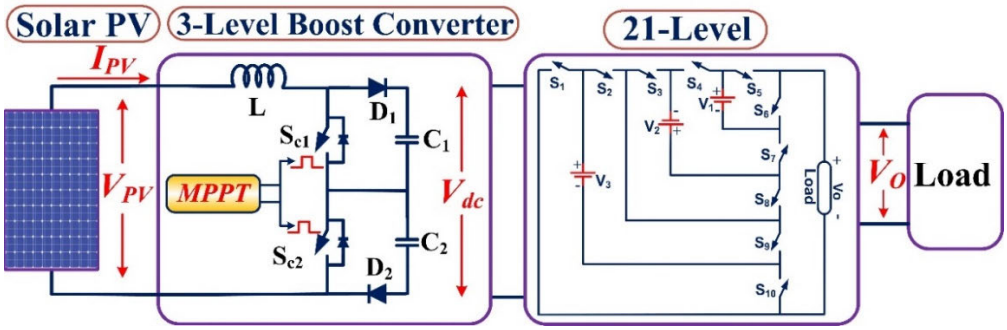

FIGURE 1. Solar PV boost converter for the proposed 21-Level MLI.

extract peak energy from the solar panels. Got DC voltage from the solar panels fed to the three-level boost converter where the voltage gets boosted to the desired level and is fed to the 21-level inverter. Performance of the MLI is based on many such parameters like power losses, efficiency, THD, cost factor, total standing voltage (TSV) are calculated. These parameters are compared with various MLI topologies and are presented in detail. The implemented system is tested in MATLAB/Simulink, whereas it is tested experimentally with a hardware setup.

The organization of the article is: Modeling of PV and three-level DC-DC boost converter is represented in section-II, the proposed 21-level MLI modeling with total standing voltage (TSV), cost function (CF) and power loss calculations in detail are presented in section III. Several comparisons are made with respect to the same and distinct levels of MLI topologies are presented in section-IV. The simulation and experimental results are explained in section V. Finally, conclusions followed with future scope are made in section VI.

II. MODELING OF PV AND DC-DC BOOST CONVERTER

A. MODELING OF SOLAR PV

The modeling of a solar cell is an important segment of analyzing a solar PV system. The overall proposed circuit comprises solar panels, three-level DC-DC boost converter fed to 21-level MLI shown in FIGURE 1. The solar PV can be modelled with three categories such as an equivalent circuit with current-voltage (I-V) and power-voltage (P-V) characteristics, the effect of solar irradiation and temperature and the partial shading condition is taken into consideration.

PV resembles two words photo and voltaic: photo represents the photonic energy, and voltaic represents the electrical energy, which implies that the energy conversion from photonic energy into electrical energy [31]. The combination of a solar array is of various types of modules, where each module comprises solar cells. This comprises p-n semiconductor diodes [32]. the designed solar PV has a behavior of changing its output with the variation of temperature and climatic conditions [33]. Therefore, the factors in modeling a solar PV are represented below:

1) SOLAR CELL: EQUIVALENT CIRCUIT AND I–V CHARACTERISTICS

The solar cell comprises internal resistance R_{SE} and R_{SH} connected to the diode in series and parallel combination, known to be an equivalent circuit shown in FIGURE 2.

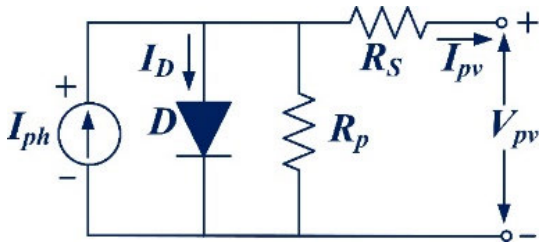

FIGURE 2. Equivalent circuit of solar PV.

V_{PV} and I_{PV} are the output voltage and current of a solar cell, respectively. These are got from the series and parallel connection of several PV modules shown in equation (1),

$$I_{PV} = \left\{ I_{Ph} - I_0 \left[exp\left(\frac{q(V_{PV} + R_S I_{PV})}{N_{SE} AKT} \right) - 1 \right] - \frac{(V_{PV} + R_S I_{PV})}{N_{SE} R_{SH}} \right\} \quad (1)$$

where N_{SE} and N_{SH} are the number of PV cells in series and parallel connection. R_S is the series resistance, and R_{SH} is the parallel resistance. A is the ideality factor of a semiconductor device. K is Boltzmann's constant ($1.3806503 \times 10^{-23}$ J/K), T is the temperature. I_p is the current produced and is depends on the irradiation and temperature shown in equation (2)

$$I_P = [I_{SK-STM} + K_i (T - T_{STM})] - \left(\frac{G}{G_{STM}} \right) \quad (2)$$

where $I_{SK\text{-}STM}$ is a short-circuited current at standard testing cases (STM), Ki is the SCC coefficient, G (W/m^2) is the irradiance on the surface of the cell, GSTM ($1000W/m^2$) is the irradiance at STM, and the cell temperature is T_{STM} [34].

$$I_D = \left\{ \frac{I_{SK-STM} + K_i (T - T_{STM})}{exp\left[(V_{OK-STM} + K_{OV} (T - T_{SKC}) / AV_{Sth} \right]} \right\} \quad (3)$$

where V_{OK-STM} is an open-circuited voltage at the standard testing case, K_{OV} represents the open-circuit voltage

coefficient, V_{Sth} is solar cell thermal voltage.

$$P_{PV}=V_{PV}\times N_{SH}\left(I_{Ph}-I_O exp\left(\frac{qV_{PV}}{N_{SE}AKT}\right)-\left(\frac{V_{PV}}{N_{SE}}\right)\right) \quad (4)$$

I-V/P-V curves represent the characteristics of a solar cell is shown in FIGURE 3 [4]. It is clear from the curve there is instability for the operating point of a PV; it varies continuously from null to open-circuit voltage. In this process, there is a single point that provides peak power for the design of solar PV at various irradiance. Here, the respective voltage and currents are V_{MPP}, I_{MPP} shown in FIGURE 3. The values of current and voltage got from the solar PV depend on irradiance, temperature, number of series and parallel connected strings. So, it is required to choose the solar panel wisely. In this article, 1Soltech 1STH-215-P panel is selected from the list of given solar modules data in MATLAB with 2 series and parallel connected modules per string. The specifications of the selected solar panel are described in table 1, and the readings in the table are given for 1 parallel string and 1 series-connected module with a solar irradiance of 1000 W/m^2 and 250°C temperature.

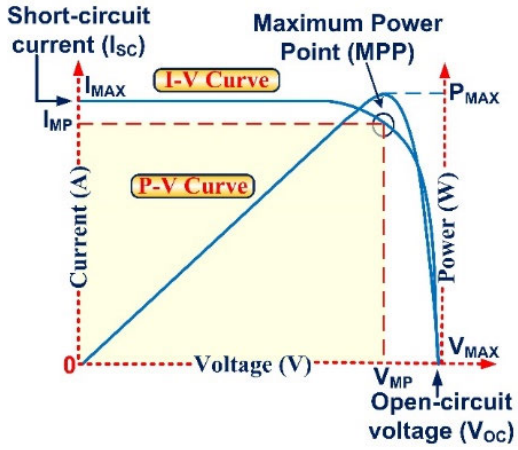

FIGURE 3. I-V and P-V characteristics of solar cell.

2) IRRADIANCE AND TEMPERATURE EFFECT

The solar PV output continuously varies with variation in climatic changes [35]. As the solar irradiance confides on the incidence angle of sun rays, this effect forces the I-V/P-V characteristics to change. The output current I_{PV} varies with the variation of sunray incidence, making V_{PV} constant and V_{PV} also shifts its magnitude, making I_{PV} constant [35]. Three factors are influencing the variation in temperature of a solar PV: The heat dissipated on its own during the functioning of PV, for the infrared wavelength started, which is a worn on the cell and the gradual increase in the sunbeam intensity [27]. The V_{OC} and I_{SC} are measured based on the equations (5) and (6) at variable irradiance.

$$V_{OC}=V'_{OC}+a_2\left(T-T'\right)-(I_{SC}-I'_{SC})R_{SE} \quad (5)$$

$$I_{SC}=I'_{SC}\left(\frac{G}{G'}\right)+a_1\left(T-T'\right) \quad (6)$$

From the above equations, the temperature coefficients are a_1 and a_2 of the PV cell, respectively [36]. V'_{OC} and I'_{SC} are the reference parameters at solar intensity G' and temperature T'. As the variations of climatic conditions are specific, it affects the output voltage and currents. At any point during the operation of solar PV, the maximum extraction of power can be done. This can be possible with an efficient MPPT technique which tracks the irradiation and temperature and provides a constant voltage at the output.

3) PARTIAL SHADING EFFECT

Apart from the temperature and irradiance conditions, a partial shading case is also a challenging task for the MPPT technique in achieving maximum power. This partial shade occurs with mists, consecutive structures, trees, etc. [37]. According to equation (2), the photocurrent I_{ph} gets reduced with low insolation. With series-connected PV modules, the current is the same in all cells. But in this case, the shaded cell goes to a breakdown, and instead of providing the energy, this acts as a load because of the weakening of photocurrent.

B. MPPT CONTROLLER

The operating of solar PV is to extract the maximum power from the PV module is an MPPT controller. During all the disturbances mentioned above, if the controller can able to operate efficiently in tracking and to provide peak power from the solar panels, the efficiency and life span of the solar PV gets increased. This can be achieved by sinking the solar source to the load for various climate conditions to produce maximum power. There are two ways to extracting the maximum power from a solar panel. They are Mechanical and electrical tracking. With mechanical tracking, the solar panels change their direction depends on the climatic variation patterns. This includes seasonal climate changes for several months. With electrical tracking, the I-V curve is forced to locate the point of maximum power in the operation of the PV array [38]. The MPPT controller is an internal part of the system which feeds the maximum power to load (batteries/motors).

For tracking maximum power during the operation of the PV module, a suitable algorithm is to be used. This can be seen in the P-V graph of a solar cell. There are many such methods to track the maximum power such as incremental conductance, perturb and observe, genetic algorithm, fractional open-circuit voltage, etc. In this article, the perturb and observe algorithm has many advantages. It is easy to implement using various controllers such as Arduino, microcontroller, etc. The maximum power point determination speed can be controlled by varying the perturbation value. The P&O algorithm is shown in FIGURE 4.

The algorithm for Perturb and Observe Technique is:

a) I_{pv} and V_{pv} values are gathered from PV module.
b) P_{pv} is calculated from I_{pv} and V_{pv}.

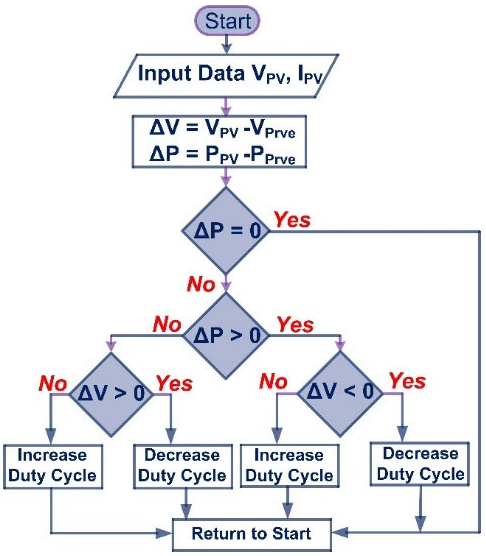

FIGURE 4. Representation of P&O algorithm.

c) Voltage and power values are stored.
d) The values are recorded for the next consecutive $(k+1)^{th}$ instant and repeat step 'a'.
e) The values got at $(k+1)^{th}$ instant are subtracted from the values got at kth instant.
f) In the PV curve of a solar panel, in the right side, the slope is negative i.e., $(\frac{dP}{dV} < 0)$ whereas on the left side, the slope is positive $(\frac{dP}{dV} > 0)$. Therefore, the lesser duty cycle occurs at the right side of the curve, and high-duty appears at the left side of the curve.
g) Based on the polarity of the slope after subtraction, the algorithm decides the change in the duty cycle.

The solar panel design is presented in section II, under I-V characteristics of solar PV section with a power of 215W, the respective parameters and their specifications are shown in TABLE 1.

TABLE 1. Specifications of a 215W PV System.

Maximum power	213.15W
The voltage at maximum power point (V_{MPP})	29V
Open circuit voltage (V_{oc})	36.3V
Current at maximum power point (I_{MPP})	7.35A
Short circuit current (I_{sc})	7.84A
Diode ideality factor	0.98117
Diode saturation current (I_D)	2.9259×10^{-10}A

C. DC-DC BOOST CONVERTER

A three-level DC-DC boost converter interfaced in between the solar panels and the proposed inverter is shown in FIGURE 5 [22]. This converter comprises a boost inductor L, two dc-link capacitors C1 and C2, and two switches S1 and S2, depending on switching states, the three-level boost converter has four modes of operation they are when the switches S1 or S2 are turned ON, Mode 2 and Mode 3 occur.

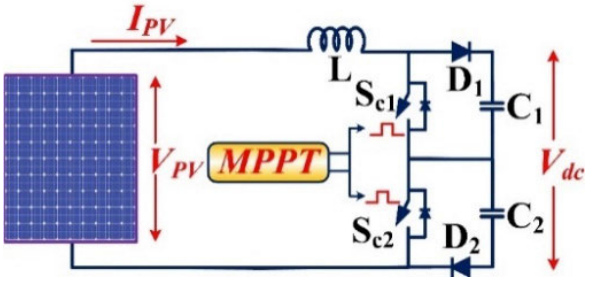

FIGURE 5. 3-level boost converter for solar PV.

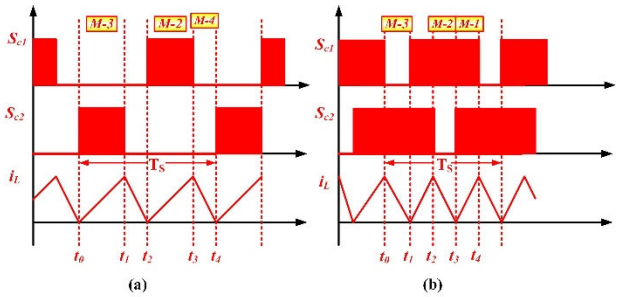

FIGURE 6. Gate pulses and inductor current of three-level boost converter (a) Region-1 (b) Region-2.

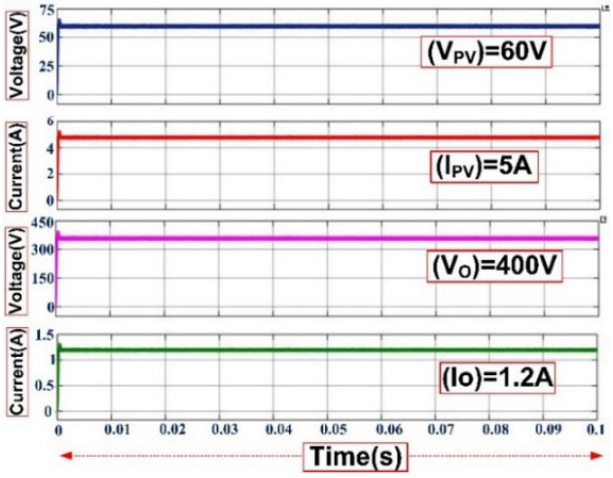

FIGURE 7. Simulation results of voltage and current for solar PV and boost converter.

During the operation of the switches S1 and S2, there is two modes of operation which are Mode 1 and Mode 4. Based on the range of duty cycle D at $(0 < D < 0.869)$ and $(0.869 < D < 1)$, there is two more operating regions. For the first range of D, the converter operates in Mode-2, Mode-3, and Mode-4, for the second range of duty cycle, the converter operates in Mode-1, Mode-2 and Mode-3, respectively. Depending on switching states, the three-level boost converter modes of operation is shown in FIGURE 6.

The specifications of the boost converter are tabulated in TABLE-2. 1Soltech 1STH-215-P solar PV panel generates 60V DC voltage with 5A current, and it will boost up to 400V DC with 1.2A by using the DC-DC boost converter. The simulation and experimental results are shown in FIGURE 7 and FIGURE 8, respectively.

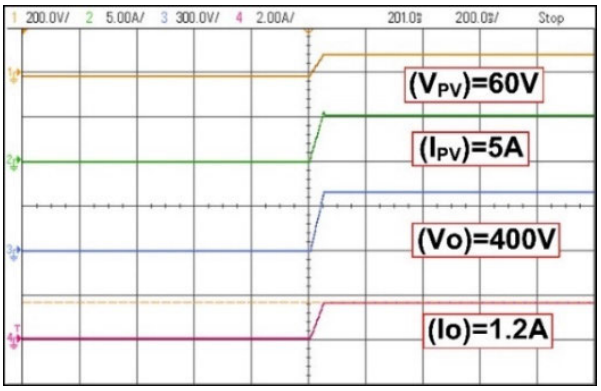

FIGURE 8. Experimental results of voltage and current for solar PV and boost converter.

TABLE 2. Specifications of the Boost Converter.

Parameters	Value
Inductance L	15.38 mH
Capacitance C1 & C2	282μF
Input DC voltage	~60V
Resistance(R2)	10 Ohms
Duty Cycle	0.869

The output voltage of the converter can be calculated from the following relation.

$$V_0 = \frac{D}{1-D} V_{dc} \tag{7}$$

The inductor of the boost converter is designed from

$$L = \frac{V_{in}}{f_s I_L} \tag{8}$$

where f_s is the switching frequency, ΔI_L is the inductor current is given as $0.3I_0$ and V_{in} is the input voltage.

The capacitor of the boost converter is designed from

$$C = \frac{I_0}{(f_s * \Delta V_0)D} \tag{9}$$

where ΔV_0 is the voltage ripple, 5% of output voltage.

III. PROPOSED ASYMMETRICAL 21-LEVEL MLI

A novel asymmetrical 21-level MLI is proposed with a smaller number of components is shown in FIGURE 9. The proposed MLI topology comprises 10 controlled switches with three asymmetric DC sources with the absence of inductors, capacitors and diodes. The three DC sources are of unequal voltage levels formed to be an asymmetrical configuration. Several power quality issues like total standing voltage (TSV), cost factor and cost per unit with various values of the weight factor, THD, switch count, component count level, voltage stress are minimized with this MLI topology. This topology achieves less TSV and is compared with various topologies. The path of the load current through the switches are represented in TABLE 3. The various switching states are represented in TABLE-4. Few modes of operation, along

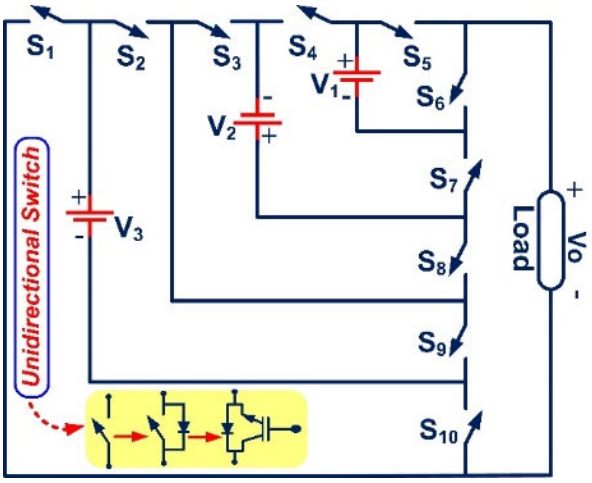

FIGURE 9. Proposed 21-level MLI.

with the switching pulses and the expected output waveform is illustrated in FIGURE 10.

The proposed 21-level MLI can be viewed through the switching pulses shown in FIGURE 10, according to the function of switches. If the switch is turned on, then the state of the switch is '1' otherwise state becomes '0'. The switches operate for several modes and produce an output voltage of 400V. The MLI is designed with three unequal magnitudes of voltages: V_1, V_2, V_3. These voltages are selected based on the 1:2:7 ratio. Hence, the values of voltages are 40V, 80V, 280V respectively. Therefore, 400V output voltage is obtained with a current of 4A and resistor of 100Ω.

The simulations of the proposed MLI are done in MATLAB/Simulink, and the respective results got are tested experimentally with a hardware setup. The MLI is tested under various dynamic load variations such as R-load, Motor (L)-load, RL-load, LR-load with sudden load disturbances. In all conditions, the results got in experimental testing are like that of the simulation results and the proposed MLI hold best in its performance in terms of cost, power losses, number of device count, efficiency, etc. The few modes of operation for the proposed 21-level MLI are shown in FIGURE 10.

The proposed 21-level MLI is operated in various modes of operation shown in TABLE 3. In mode-1 operation of the circuit, the switches S_{10}, S_3, S_7, S_5, S_2 turn on forming a load current path of V_B-S_{10}-V_3- S_2- S_3- V_2- S_7- V_1- S_5- V_A, where V_1, V_2 and V_3s ources act in the circuit and produce a voltage of 40V, 80V and 280V respectively and get a maximum voltage of 400V. The respective switching pulses, switching states and current paths are represented in Table 3 and Table 4, respectively. In mode-2 operation, the switches S_{10}, S_2, S_3, S_7 turn on forming a load current path of V_B-S_{10}-V_3- S_2- S_3- V_2- S_7-D_6-V_A, where V_2 and V_3 sources act in the circuit and produce a voltage of 80V and 280V respectively and get a voltage of $9V_{dc}$ which is equal to 360V. In mode-3 operation, the switches S_{10}, S_2, S_7, S_5 turn on forming a load current path of V_B-S_{10}-V_3- S_2- D_8- S_7- V_1-S_5-V_A, where V_3 and V_1 sources act in the circuit and produce

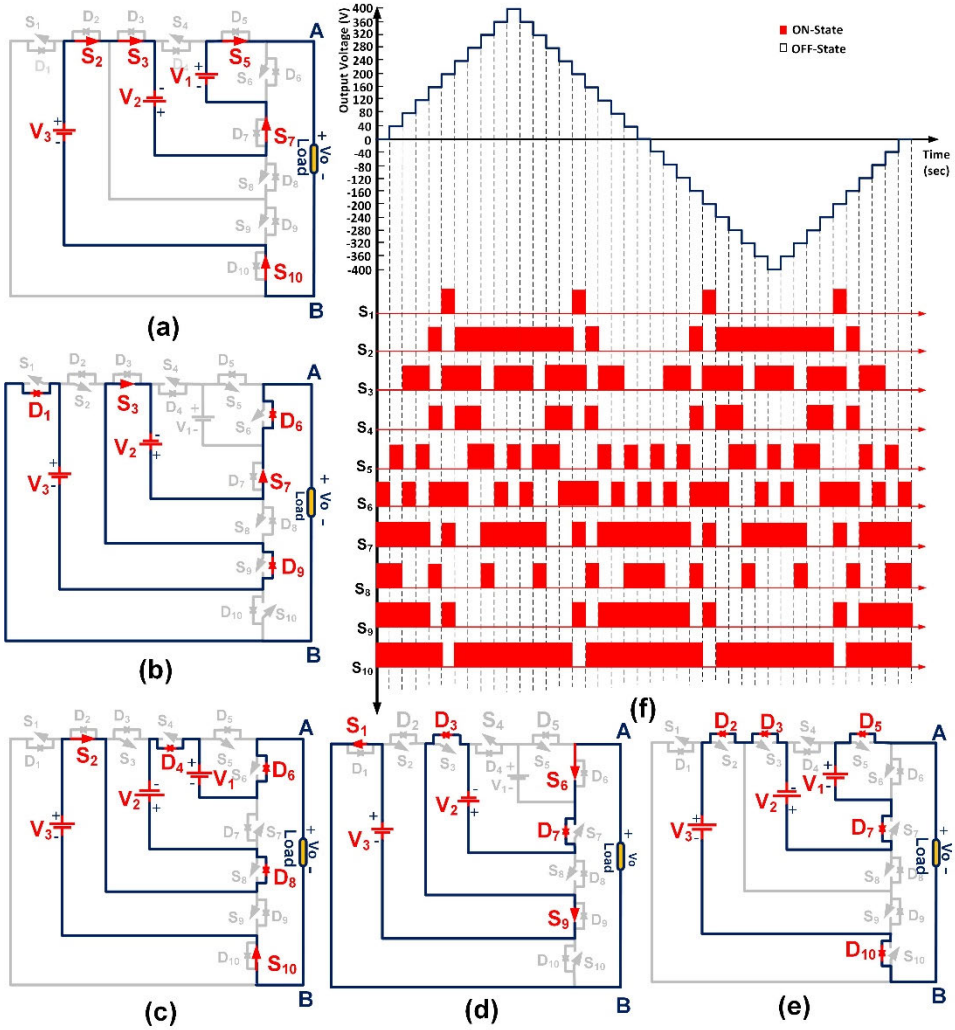

FIGURE 10. Operating modes of the proposed 21-Level MLI topology. (a): Mode-1, (b) Mode-6, (c) Mode-7, (d) Mode-16, (e) Mode-21, (f) 21-Level expected output voltage waveform with switching pulses.

a voltage of 280V and 40V respectively and get a voltage of $8V_{dc}$ equal to 320V. In mode-4 operation, the switches S_{10}, S_2, S_3, S_4, S_5 turn on with the voltages V_3 source acts in the circuit and produces a voltage of 280V respectively and get a voltage of $7V_{dc}$ which is equal to 280V. In mode-5 operation, the switches S_{10}, S_2, S_4 S_7, S_5, S_6 turn on with the voltages V_3 and V_1 sources acts in the circuit and produces a voltage of 280V and 40V respectively and get a voltage of $6V_{dc}$ equal to 240V. In mode-6 operation, the switches S_{10}, S_2, S_8, S_4, S_5, turn on with the voltages V_3 and V_2 sources act in the circuit and produce a voltage of 280V and 80V respectively and get a voltage of $5V_{dc}$ which is equal to 200V. In mode-7 operation, the switches S_{10}, S_2, S_8, S_4, S_6, turn on with the voltages V_3, V_2 and V_1 sources acts in the circuit and produces a voltage of 280V, 80V and 40V respectively and get a voltage of $4V_{dc}$ which is equal to 160V. In mode-8 operation, the switches S_{10}, S_9, S_7, S_5, turn on with the voltages $V_2$and V_1 sources act in the circuit and produces a voltage of 80V and 40V respectively and get a voltage of $3V_{dc}$, which is equal to 120V. In mode-9 operation, the switches S_{10}, S_9, S_3, S_7, S_6, turn on with the voltages V_2 source acts in the circuit and produces a voltage of 80V respectively and gets a voltage of $2V_{dc}$ equal to 80V. In mode-10 operation, the switches S_{10}, S_9, S_8, S_7, S_5, turn on with the voltages V_1 source acts in the circuit and produces a voltage of 40V respectively and gets a voltage of V_{dc} which is equal to 40V. Hence the positive cycle is made. The negative cycle is implemented with the negative modes of operation shown in Table 3, according to the switching states in Table 4. Therefore, the 21-level MLI output waveform is achieved with a simulation THD of 3.49% shown in FIGURE 16. The experimental THD is shown in FIGURE 22 is of 3.49%, which is like that of simulation THD. The output waveform for output voltage and currents are shown in FIGURE 14 and FIGURE 15. The experimental output voltage and output current are represented in FIGURE 17. The MLI is tested with R-load, and the result is shown in FIGURE 18. For L-load, the experimental result shown in FIGURE 19. For RL-load,

TABLE 3. Load Current Path for the Proposed 21-level MLI.

Mode	*Load current path*	*Output Voltage (V)*		
Mode-1	$V_B - S_{10} - V_3 - S_2 - S_3 - V_2 - S_7 - V_1 - S_5 - V_A$	$10V_{dc}$	$V_3+V_2+V_1$	+400
Mode-2	$V_B - S_{10} - V_3 - S_2 - S_3 - V_2 - S_7 - D_6 - V_A$	$9V_{dc}$	V_3+V_2	+360
Mode-3	$V_B - S_{10} - V_3 - S_2 - D_8 - S_7 - V_1 - S_5 - V_A$	$8V_{dc}$	V_3+V_1	+320
Mode-4	$V_B - S_{10} - V_3 - S_2 - S_3 - D_4 - S_5 - V_A$	$7V_{dc}$	V_3	+280
Mode-5	$V_B - S_{10} - V_3 - S_2 - S_3 - D_4 - V_1 - D_6 - V_A$	$6V_{dc}$	V_3-V_1	+240
Mode-6	$V_B - D_1 - V_3 - D_9 - S_3 - V_2 - S_7 - D_6 - V_A$	$5V_{dc}$	V_3-V_2	+200
Mode-7	$V_B - S_{10} - V_3 - S_2 - D_8 - V_2 - D_4 - V_1 - D_6 - V_A$	$4V_{dc}$	$V_3-V_2-V_1$	+160
Mode-8	$V_B - S_{10} - D_9 - S_3 - V_2 - S_7 - V_1 - S_5 - V_A$	$3V_{dc}$	V_1+V_2	+120
Mode-9	$V_B - S_{10} - D_9 - S_3 - V_2 - S_7 - D_6 - V_A$	$2V_{dc}$	V_2	+80
Mode-10	$V_B - S_{10} - D_9 - D_8 - S_7 - V_1 - S_5 - V_A$	V_{dc}	V_1	+40
Mode-11	$V_B - S_{10} - D_9 - D_8 - S_7 - D_6 - V_A$	0	0	0
Mode-12	$V_A - D_5 - V_1 - D_7 - S_8 - S_9 - D_{10} - V_B$	$-V_{dc}$	$-V_1$	-40
Mode-13	$V_A - S_6 - D_7 - V_2 - D_3 - S_9 - D_{10} - V_B$	$-2V_{dc}$	$-V_2$	-80
Mode-14	$V_A - D_5 - V_1 - D_7 - V_2 - D_3 - S_9 - D_{10} - V_B$	$-3V_{dc}$	$-(V_1+V_2)$	-120
Mode-15	$V_A - S_6 - V_1 - S_4 - V_2 - S_8 - D_2 - V_3 - D_{10} - V_B$	$-4V_{dc}$	$-(V_3-V_2-V_1)$	-160
Mode-16	$V_A - S_6 - D_7 - V_2 - D_3 - S_9 - V_3 - S_1 - V_B$	$-5V_{dc}$	$-(V_3-V_2)$	-200
Mode-17	$V_A - S_6 - V_1 - S_4 - D_3 - D_2 - V_3 - D_{10} - V_B$	$-6V_{dc}$	$-(V_3-V_1)$	-240
Mode-18	$V_A - D_5 - S_4 - D_3 - D_2 - V_3 - D_{10} - V_B$	$-7V_{dc}$	$-V_3$	-280
Mode-19	$V_A - D_5 - V_1 - D_7 - S_8 - D_2 - V_3 - D_{10} - V_B$	$-8V_{dc}$	$-(V_3+V_1)$	-320
Mode-20	$V_A - S_6 - D_7 - V_2 - D_3 - D_2 - V_3 - D_{10} - V_B$	-9Vdc	$-(V_3+V_2)$	-360
Mode-21	$V_A - D_5 - V_1 - D_7 - V_2 - D_3 - D_2 - V_3 - D_{10} - V_B$	-10Vdc	$-(V_3+V_2+V_1)$	-400

TABLE 4. Switching Operations for the Proposed 21-level MLI.

Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
Level-1	0	1	1	0	1	0	1	0	0	1
Level-2	0	1	1	0	0	1	1	0	0	1
Level-3	0	1	0	0	1	0	1	1	0	1
Level-4	0	1	1	1	1	0	0	0	0	1
Level-5	0	1	1	1	0	1	0	0	0	1
Level-6	1	0	1	0	0	1	1	0	1	0
Level-7	0	1	0	1	0	1	0	1	0	1
Level-8	0	0	1	0	1	0	1	0	1	1
Level-9	0	0	1	0	0	1	1	0	1	1
Level-10	0	0	0	0	1	0	1	1	1	1
Level-11	0	0	0	0	0	1	1	1	1	1
Level-12	0	0	0	0	1	0	1	1	1	1
Level-13	0	0	1	0	0	1	1	0	1	1
Level-14	0	0	1	0	1	0	1	0	1	1
Level-15	0	1	0	1	0	1	0	1	0	1
Level-16	1	0	1	0	0	1	1	0	1	0
Level-17	0	1	1	1	0	1	0	0	0	1
Level-18	0	1	1	1	1	0	0	0	0	1
Level-19	0	1	0	0	1	0	1	1	0	1
Level-20	0	1	1	0	0	1	1	0	0	1
Level-21	0	1	1	0	1	0	1	0	0	1

the result shown in FIGURE 20. For LR-load, the practical result is shown in FIGURE 21. The complete experimental setup is shown in FIGURE 13. The empirical specifications used in implementing 21-level MLI are shown in Table 5.

A. TOTAL STANDING VOLTAGE (TSV)

The total standing voltage (TSV) plays a significant role in the selection of switches in the circuit. It is the sum of all blocking voltages for the total number of semiconductor devices in the topology. The voltage stresses on the bi-directional and uni-directional switches are given as $V_{Sbi} = V_i$ and $V_{Suni} = 2V_i$

TABLE 5. Specifications of 21-level MLI.

Output Voltage V_o	400V
Output current I_o	4A
dSPACE controller	RTI1104
Resistive load (Lamp)	100Ω
Inductive load	98mH
IGBT	IGBT CM75DU-12, 600V, 75A
Motor load	Single-phase, 230V, 0.5HP

respectively, where i = 1, 2.....n and n are complimentary switches count. The maximum output voltage (V_0) for the proposed topology is $V_{0,max} = 400V$. In the proposed MLI, the voltages are equal for complimentary switches, and all switches are unidirectional. Hence TSV is calculated using the following relation:

$$\begin{aligned} TSV &= 2(V_{S1} + V_{S3} + V_{S5} + V_{S7} + V_{S9}) \\ &= 2(7V_{dc} + 2V_{dc} + V_{dc} + 3V_{dc} + 7V_{dc}) \\ &= 40V_{dc} \end{aligned}$$

The maximum blocking voltage of the voltage is less results in the low rating devices and as a result the cost of the developed system gets decreased. Further, the component count level factor is realized for finding the components count. The component count level factor represents the total number of semiconductor devices used in a circuit. The lesser the value, fewer components are used, which provides fewer losses and more efficiency. The component count per level factor F_{ccl} is calculated using the following relation:

$$F_{ccl} = \frac{N_s + N_d + N_{cap} + N_{dk} + n}{N_{Lev}} \tag{10}$$

B. COST FUNCTION

The cost function plays a major role in selecting the respective MLI having less cost. The design of MLI based on cost

TABLE 6. The Variance of Various 21-Level MLI Topologies.

Topology			CHB	NPC	FC	[40]	[41]	[39]	Proposed
No. of Switches (N_S)			40	40	40	16	10	12	10
Driver board circuits (N_{dk})			40	40	40	16	10	10	10
DC sources (n)			10	1	1	7	6	3	3
Number of diodes (N_d)			12	20	10	-	10	-	-
Number of capacitors (N_c)			3	20	20	-	3	-	-
Components count per level (F_{ccl})			5	5.76	5.28	1.86	1.86	1.2	1.1
Total Standing Voltage (TSV_{pu})			4.0	4.0	4.0	6.7	4.0	4.4	4.0
Cost Function/Levels (CF/L)	α	0.5	46.19	5.81	5.33	11.78	10.0	3.45	3.14
		1.5	48.09	6.0	5.52	14.01	11.14	4.08	3.71

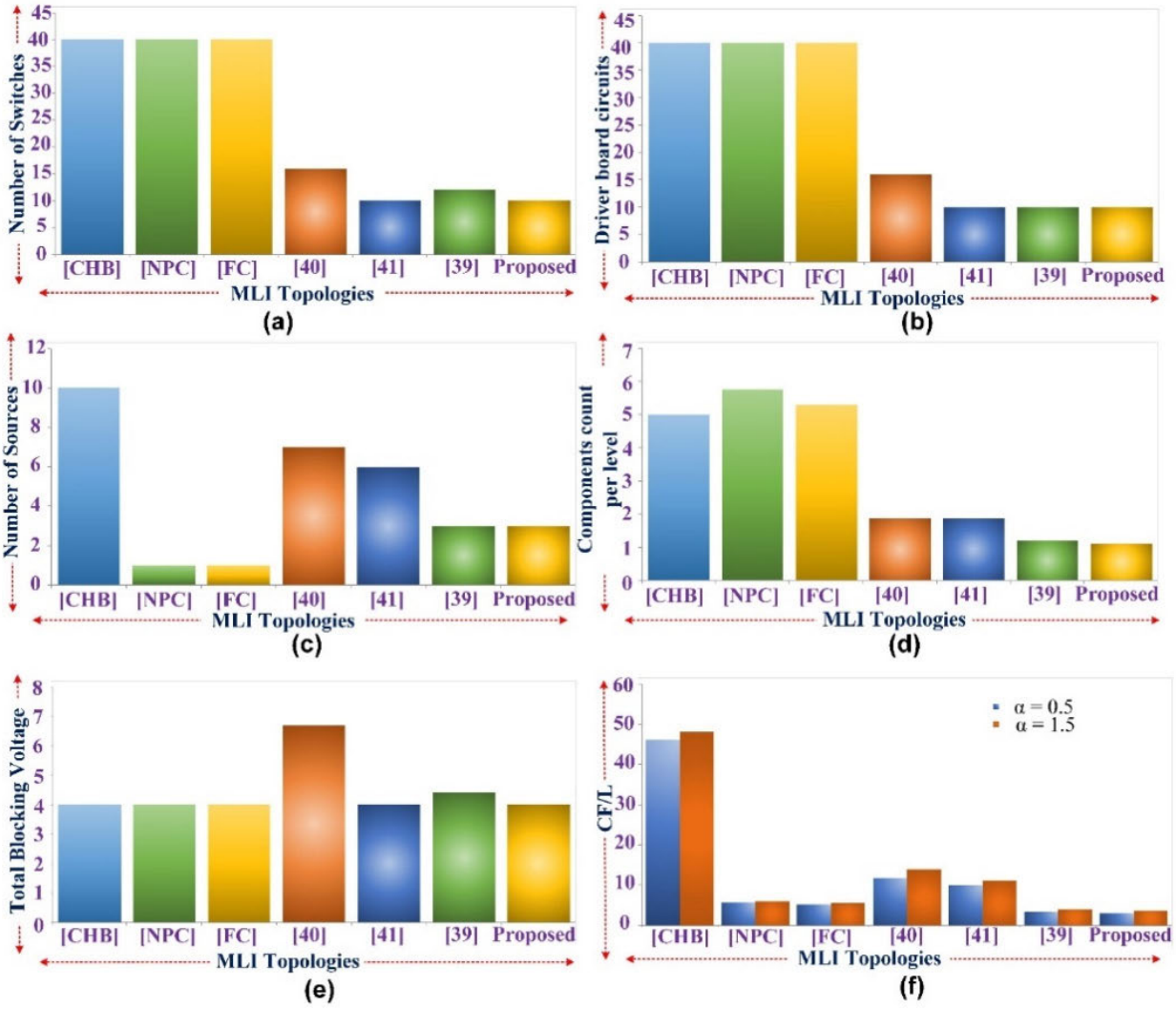

FIGURE 11. Comparison of various 21-Level MLI topologies. (a) Switches count (b) Gate driver circuits count (c) DC sources count (d) Components count per level (e) TSV (f) Cost function/Level count.

function makes the MLI cost-effective. The cost factor for the proposed 21-level MLI can be calculated using the parameters like several switch counts, source count, total standing voltage, driver circuits count and using the formula shown in equation (11) [39].

$$CF = (N_S + N_{dk} + N_d + N_c + \alpha TSV_{pu}) \times n \quad (11)$$

where CF is the cost factor, N_S is the number of switches, N_{dk} is the gate driver circuit count, N_d is the diodes count, N_c is the number of capacitors. TSV is the maximum standing voltage for the switches in conduction. TSV_{pu} is the total standing voltage per unit, which is given by

$$TSV_{pu} = V_{TSV}/V_{0max} \quad (12)$$

TABLE 7. Cost Comparison of Various Multilevel Inverters With Proposed 21-Level MLI.

Topology			[42]	[43]	[44]	[45]	[46]	[47]	Proposed
Number of Levels			25	25	31	33	23	31	21
No. of Switches (N_S)			24	20	14	24	18	16	10
Driver board circuits (N_{dk})			24	16	10	18	12	12	10
DC sources (n)			8	8	6	8	6	6	3
Total Standing Voltage (TSV_{pu})			4.0	3.33	5.33	5.0	11.45	6.33	4.0
Cost Function/Levels (CF/L)	α	0.5	16	12.05	11.78	10.78	9.31	6.03	3.14
		1.5	17.28	13.11	14.01	12	12.30	7.25	3.71

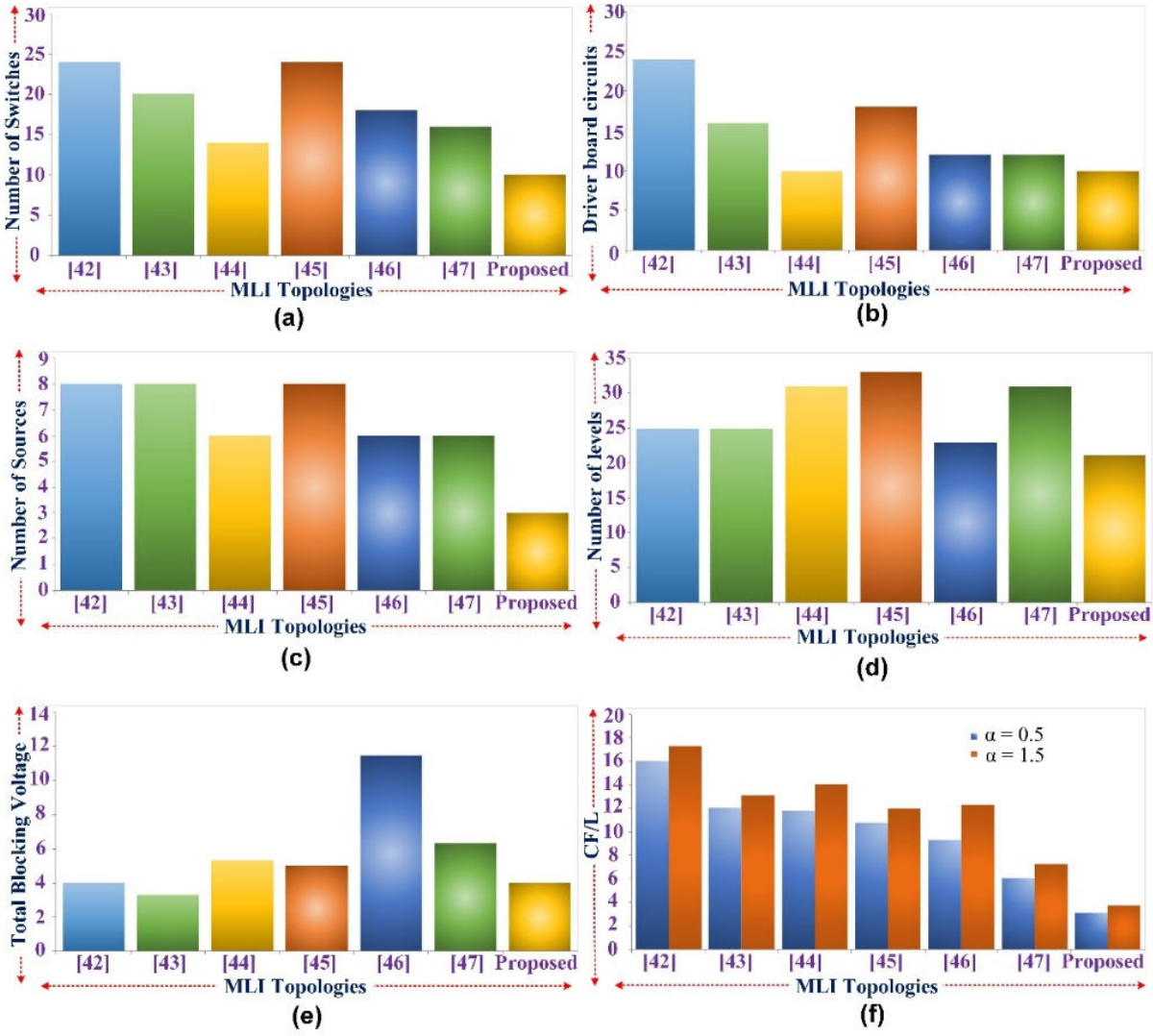

FIGURE 12. Comparison of various topologies of MLI with different levels with proposed 21-Level MLI. (a) Number of switches (b) Driver circuit count (c) DC sources count (d) Number of levels (e) TSV (f) Cost function/Level count.

where n is the DC sources count in the circuit. α is the weight coefficient which is multiplied with TSVpu. For the proposed asymmetrical 21-level topology, as the diodes and capacitors are not used; hence these can be neglected, and the cost function is calculated using the relation.

$$CF = (S + N_{dk} + \alpha TSV_{pu}) \times n \tag{13}$$

The value of α is to be considered in such a way that one value is greater than one, and the other is less than one. In this article, the value of α is realized as 0.5 (<1), and the other value is 1.5 (>1) for the evaluation of the cost function. The cost-effectiveness of any MLI is calculated with level count (CF/L). This value is to be calculated for both values of α shown in TABLE 6.

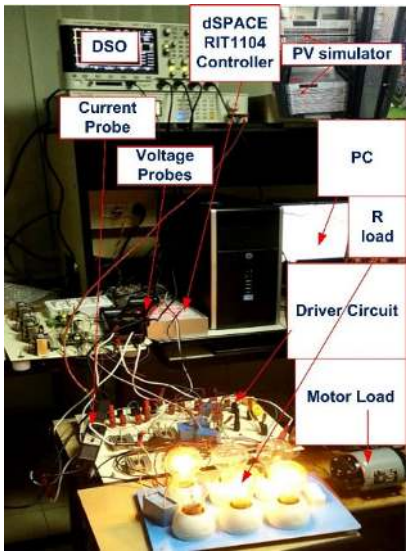

FIGURE 13. Experimental setup.

C. POWER LOSS AND EFFICIENCY

The total losses are divided into conduction and switching losses related to switches. The conduction losses for the switches can be calculated using equation (14).

$$P_{Cl} = \left[V_S + R_S i^{\beta}(t)\right] i(t) \tag{14}$$

where V_S is the voltage drop of the IGBT switch and V_d is the voltage drop of diodes. R_S is the equivalent resistance of the switch, R_d is the diodes equivalent resistance. The generalized relation for finding conduction power losses (P_{cl}) considering the N_{IGBT} switches and N_d diodes at t instant of time is given in equation (15).

$$P_{Cl} = \frac{1}{2\pi}\int_0^{2\pi}\left[N_{IGBT}(t)\, P_{cl,IGBT}(t)\, dt\right] \tag{15}$$

The switching losses can be calculated from the equation (16)

$$P_{Sl} = f\sum_{K=1}^{N_{switch}}\left[\sum_{j=1}^{N_{on,k}} En_{on,kj} + \sum_{j=1}^{N_{off,k}} En_{off,kj}\right] \tag{16}$$

where E_{on} and E_{off} are the energy used by the switches.

The total power losses $(P_{total\ loss})$ is calculated:

$$P_{total\ loss} = P_{cl} + P_{sl} \tag{17}$$

The efficiency (η) is calculated using the following relation

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \tag{18}$$

where P_{out} and P_{in} are the output and input powers.

The output power can be estimated:

$$P_{out} = V_{rms} * I_{rms} \tag{19}$$

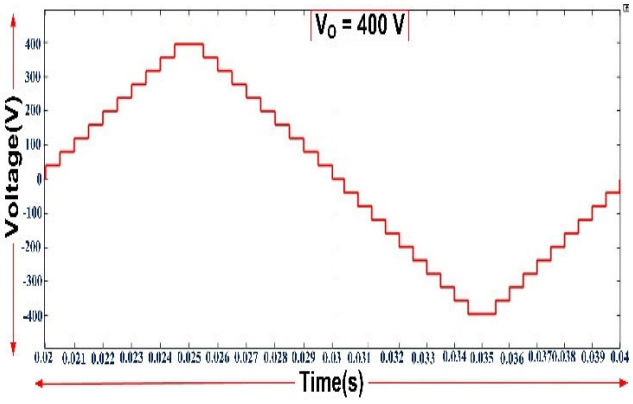

FIGURE 14. Simulation output voltage waveform of the 21-Level MLI.

IV. COMPARISON STUDIES

In the proposed 21-level MLI topology, it is noticed that it is cost-effective as compared with the various recent topologies for both values of α. The proposed MLI is compared with multiple current topologies considering important parameters like several switches, DC source count, gate driver circuits, Capacitor count, total standing voltage, component count per level in Table 6 and graphically represented in FIGURE 11. FIGURE 11 (e) represents the comparison of total standing voltage and is less than the other topologies. FIGURE 11 (f) shows the comparison of the cost function for various topologies and found cost-effective.

The proposed 21-level MLI is compared with various topologies are of different levels, and it is noticed that this topology is cost-effective as compared with the various recent topologies for both values of α. The proposed MLI is compared with multiple current topologies considering important parameters like several switches, DC source count, gate driver circuits, Capacitor count and total standing voltage in TABLE 7 and graphically represented in FIGURE 12. FIGURE 12 (e) represents the comparison of total standing voltage and is less than the other topologies. FIGURE 12 (f) shows the comparison of the cost function for various topologies and found cost-effective. The proposed MLI got better results in all parameters of comparison.

V. RESULTS AND DISCUSSION

The proposed topology comprises three power sources and ten unidirectional power semiconductor power switches (N_s). The inverter parameters such as the number of power sources (n), semiconductor switches (N_s), output voltage levels (N_l) and peak output voltage (V_0) are estimated as follows.

The number of switches (N_s) is calculated from $N_s = 2^n + 2$. Let $n = 3$, then the $N_s = 10$. The number of levels for the proposed inverter can be estimated as $N_l = 7 \times n$. Therefore the output levels obtained are $N_l = 21$. The inverter peak output voltage is obtained from $V_0 = [2^n + 2] * V_{dc}$ Where $V_{dc} = V_1 = 40V$, hence $V_0 = 400V$.

The simulation results are obtained using MATLAB/SIMULINK, where the voltage and number of

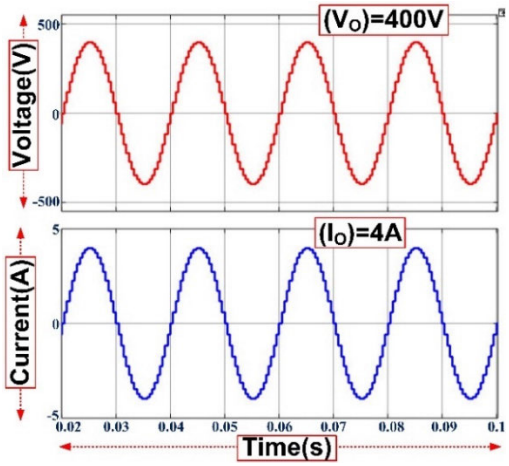

FIGURE 15. Simulation output voltage and current waveforms of the 21-Level MLI.

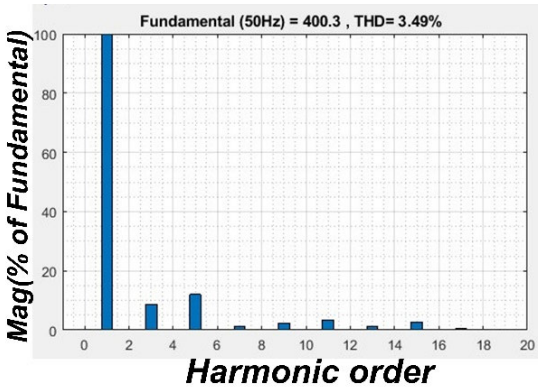

FIGURE 16. Simulation THD of proposed 21-level MLI.

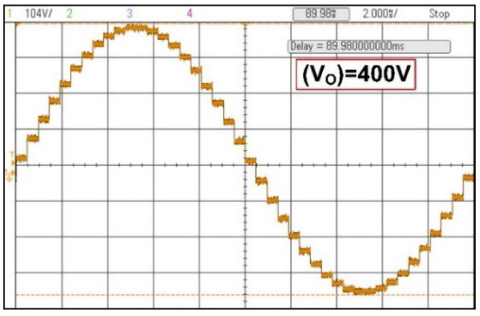

FIGURE 17. Experimental output voltage waveform (V_0).

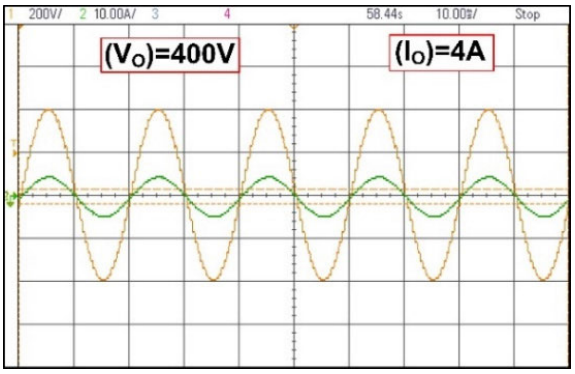

FIGURE 18. Experimental output voltage and current waveforms for R-load.

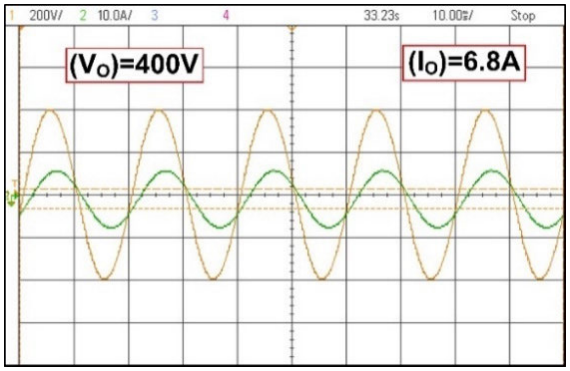

FIGURE 19. Experimental output voltage and current waveforms for L-load.

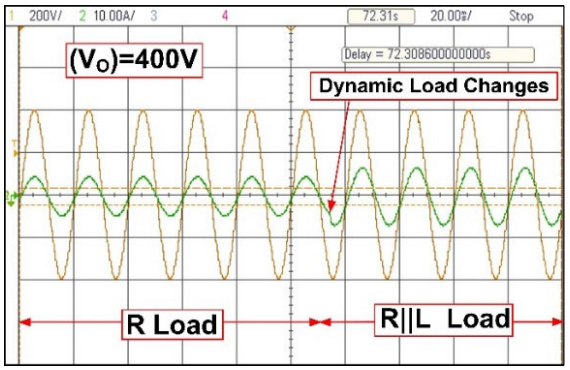

FIGURE 20. Experimental output voltage and current waveforms under dynamic load changes of R || L-load.

levels obtained for the proposed 21-level MLI are shown in FIGURE 14. The output voltage and currents obtained are $V_0 = 400V$, and $I_0 = 4A$, respectively, are shown in FIGURE 15. In FFT analysis, the THD got is 3.49% and is shown in FIGURE 16. The simulations results are tested experimentally and verified in the laboratory by implementing a 21-level inverter setup shown in FIGURE 13. The set up comprises CM75DU-12, 600V, 75A IGBT's with three input DC sources V_1, V_2 and V_3 provide 21-levels and produce an output voltage of 400V and 50Hz frequency. For operate IGBTs, the pulses are generated based on the switching angles using a controller board on the dSPACE RTI1104 processor. The experimental results containing the output voltage $V_0 = 400V$ is shown in FIGURE 17, and the experimental results of voltage $V_0 = 400V$ and current $I_0 = 4A$ for lamp load with a resistance of 100Ω are shown in FIGURE 18. Experimentally THD obtained is 3.49% and is shown in FIGURE 22, which is similar to the simulation THD. For motor load, L = 98mH, the voltage and current waveforms are shown in FIGURE 19 with an output current of 6.8A. The proposed MLI is tested for dynamic load variations for R||L load, the respective results shown in FIGURE 20. For L||R load

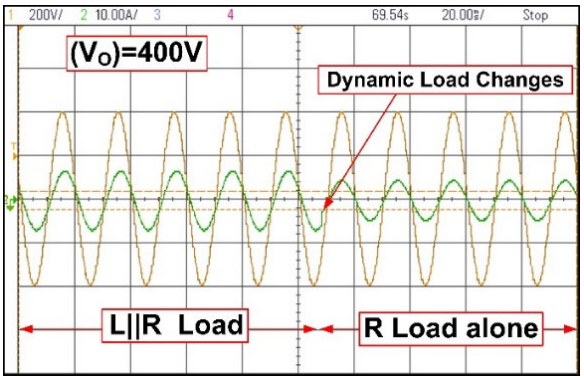

FIGURE 21. Experimental output voltage and current waveforms under dynamic load changes of L || R-load.

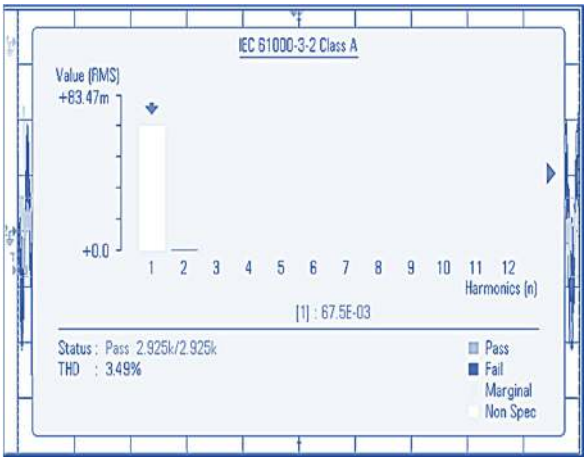

FIGURE 22. Experimental THD of proposed 21-level MLI.

under the load disturbance conditions, results are represented in FIGURE 21.

VI. CONCLUSION AND FUTURE SCOPE

A novel asymmetrical 21-level MLI topology is designed and implemented for the solar PV energy system with lesser semiconductor devices to reduce the cost and size of the inverter improves efficiency and reliability. P&O algorithm based MPPT technique is implemented to extract the maximum power from the PV panel; the stable output is achieved irrespective of partially shaded conditions. The proposed MLI requires fewer components to generate desired output voltage levels with a low THD. TSV and cost function is calculated, and all parameters are compared with various topologies with the same and different levels of MLI. Comparative analysis shows that the proposed MLI is helpful in less TSV value, more efficient and cost-effective. The proposed MLI is tested under various dynamic load variations, and it is noticed that both simulation and experimental THD are 3.49%. TSV_{pu} is 4; efficiency is 94.21%, CF/L value for both values of α are 3.14and 3.71, which shows the cost of the inverter is very less compared with various topologies.

As the topology can able to deliver power with less harmonic content, which is permissible as per IEEE standards, this can be efficiently applied for the grid-connected systems and dynamic voltage restorer (DVR) based applications and well-suited for the renewable energy sources. Besides that, it is favorable for single-phase applications, where the multiple isolated DC sources are available. The proposed MLI applied to the real applications is the future work and is suitable for a battery storage system for standalone and emergency services like residential and hospitality industries.

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