A novel CMOS low-noise amplifier design for 3.1-to 10.6-GHz ultra-wide-band wireless receivers

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A Novel CMOS Low-Noise Amplifier Design for 3.1- to 10.6-GHz Ultra-Wide-Band Wireless Receivers

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Abstract—An ultra-wideband (UWB) 3.1- to 10.6-GHz low-noise amplifier (LNA) employing a common-gate stage for wideband input matching is presented in this paper. Designed in a commercial 0.18-μm 1.8-V standard RFCMOS technology, the proposed UWB LNA achieves fully on-chip circuit implementation, contributing to the realization of a single-chip CMOS UWB receiver. The proposed UWB LNA achieves 16.7 ± 0.8 dB power gain with a good input match (S11 < -9 dB) over the 7500-MHz bandwidth (from 3.1 GHz to 10.6 GHz), and an average noise figure of 4.0 dB, while drawing 18.4-mA dc biasing current from the 1.8-V power supply. A gain control mechanism is also introduced for the first time in the proposed design by varying the biasing current of the gain stage without influencing the other figures of merit of the circuit so as to accommodate the UWB LNA in various UWB wireless transmission systems with different link budgets.

Index Terms—Common gate, low-noise amplifier (LNA), RFCMOS, ultra-wideband (UWB), variable gain.

I. INTRODUCTION

IN 2002, the Federal Communications Commission (FCC) approved the operation of certain types of wireless devices incorporating the ultra-wideband (UWB) technology, which transmits information using very low power, short impulses thinly spreading over a wide bandwidth [1]. Benefiting from the extremely wide transmission bandwidth, the UWB radio exhibits desirable features such as large transmission channel capacity, fine time and range resolution, less multipath fading effect and easier material penetration. Possible applications are high-data-rate wireless connection, high-accuracy positioning/locating, penetration imaging, etc. [2]–[4]. Table I presents the categories of the UWB applications approved by the FCC with their respective spectrums and restrictions [1].

Of all the spectrums approved by the FCC for UWB applications, the 3.1- to 10.6-GHz band is of the greatest interest for both academia and industry due to its versatility in almost all of the approved UWB applications. Due to the FCC's loose definition of UWB [1], various methods can be employed to utilize this vast spectrum. Meanwhile, different wideband pulse shapes and pulse modulation schemes have been proposed for the future UWB transmission systems [5]–[9]. Two proposals have been refined for the final decision:

1) Direct-sequence UWB (DS-UWB) proposal [10];

TABLE I
FCC-APPROVED UWB APPLICATIONS [1]

Application (Systems)	Spectrum Allocated For Application	Limited Operation
Ground Penetrating Radar and Wall Imaging	< 960 MHz or 3.1 - 10.6 GHz	Yes*
Through-Wall Imaging	< 960 MHz or 3.1 - 10.6 GHz	Yes**
Medical Imaging	3.1 - 10.6 GHz	Yes***
Surveillance	1.99 - 10.6 GHz	Yes****
Vehicular Radar	24 - 29 GHz	No
Communications and Measurement	3.1 - 10.6 GHz (subject to FCC's emission power limitations)	No

*: Restricted to law enforcement, fire and rescue organizations, scientific research institutions, commercial mining companies, construction companies.

**: Restricted to law enforcement, fire and rescue organizations.

***: Restricted to licensed health care practitioners.

****: Restricted to law enforcement, fire and rescue organizations, public utilities, and industrial entities.
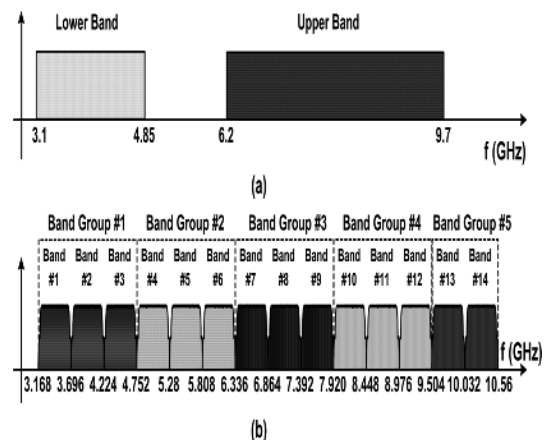
Fig. 1. Spectrum division of the two UWB proposals. (a) DS-UWB. (b) MB-OFDM.

2) Multiband orthogonal frequency division multiplexing UWB (MB-OFDM UWB) proposal [11]. The DS-UWB proposal divides the 3.1- to 10.6-GHz band into two discontinuous bands while the MB-OFDM UWB proposal divides the whole band into 14 *528-MHz sub-bands* that are grouped into five main bands as shown in Fig. 1.

Despite all the favorable features of the UWB systems, serious challenges still exist for the realization of UWB receiver front-end circuits, especially for the low-noise amplifier

(LNA). Due to FCC's stringent power-emission limitation at the transmitter and the additional transmission path loss, the received UWB signal exhibits very low power-spectral density (PSD) at the receiver antenna, resulting in a received signal power that is typically three orders of magnitude smaller than that of the narrow-band transmission systems [12]. Therefore, a UWB LNA is required to provide sufficient gain over the entire 7500-MHz bandwidth, a wide-band 50-Ω input matching and, more importantly, a low noise figure to enhance the sensitivity of the UWB receiver. Low power consumption is also desired for the LNA. The linearity of an amplifier is traditionally described in terms of 1-dB compression point (P1 dB) and third-order intercept point (IP3). While the UWB signal seldom suffers from gain compression in the LNA due to the low power of the received signal, the IP3 could be an important figure-of-merit of the proposed LNA due to the existence of strong narrow-band interferers such as the 802.11a WLAN signals in the 5- to 6-GHz band. However, the IP3 of the proposed LNA is not of great concern of this work due to the two reasons: Firstly, the UWB signals are intrinsically wide-band signals rather than single tones in narrow-band systems, which bring about the difficulty in defining the IP3 for the LNA. Secondly and even more importantly, thanks to today's mature antenna design techniques [13], [14], the interferers within the 5- to 6-GHz frequency band could be readily rejected by notch UWB antennas, relaxing the requirement for the linearity of the proposed UWB LNA.

This paper focuses on the design and implementation of an LNA for UWB applications based on the conventional RFCMOS technology. Section II discusses the design challenges in the implementation of a CMOS UWB LNA, while Section III gives the detailed circuit analysis and describes the optimizing techniques. Section IV presents the final schematic of the proposed design with a comparison of the pre-layout simulation and post-layout simulation results. Section V summarizes the figures of merit of the CMOS UWB LNA and compares its application in both DS-UWB proposal and MB-OFDM proposal. Finally, Section VI draws the conclusion.

II. DESIGN CHALLENGES

Although the employment of the wide-band impulse as the transmitting signal has greatly simplified the receiver front-end architecture, most of the design challenges of a UWB LNA remain due to the enormous bandwidth. While various LNAs in CMOS technology have been studied for a long period [15]–[17], traditionally, wide-band RF amplifiers are realized in compound semiconductor technologies (e.g., SiGe and GaAs), taking advantage of their superior intrinsic frequency response and noise performance [18], [19]. With its higher parasitics, the lossy silicon substrate of the CMOS technology substantially degrades the gain and the noise performance of the amplifier as frequency increases, which further jeopardizes the maximum achievable bandwidth [20], [21].

The distributed amplifier (DA), in which the parasitic capacitances of the active devices are absorbed by the transmission lines, has been proposed to be a good candidate for wide-band amplification. Recent research shows that relatively flat gain can be achieved over the 3.1- to 10.6-GHz UWB band using
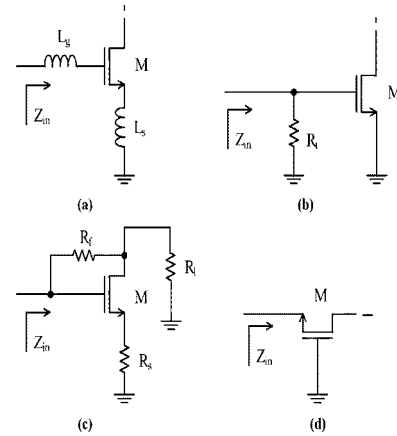

Fig. 2.　Basic input matching techniques. (a) Inductive source degeneration. (b) Direct resistor termination. (c) Shunt-series feedback. (d) Common-gate $1/g_m$ termination.

CMOS distributed amplifiers [22]–[24]. However, due to the *additive* nature of each transistor's gain, the distributed amplifiers cannot achieve high gain. The average gain of the reported DAs is around 8 dB, which is insufficient to amplify the received UWB signal. On the other hand, the power consumption of a typical DA is more than 60 mW, too high for the battery-powered portable UWB devices. Furthermore, although the distributed amplifier can provide wide-band amplification, it has not been optimized for noise performance. Considering these drawbacks associated with the DAs, traditional multistage transistor amplifier technique is opted for our design.

The noise performance of an LNA is directly dependent on its input matching. The wide-band input matching is intrinsically noisier than the narrow-band counterparts as the noise performance can not be optimized for a specific frequency. Thus, the stringent tradeoff between the wide-band input matching and the noise figure of the UWB LNA should be carefully studied and decided. Fig. 2 shows the four basic 50-Ω input matching techniques that have been explored in the traditional transistor-amplifier domain [16], [17], [20], [25], [26]. The common-gate architecture (or *the $1/g_m$ termination*) that is illustrated in Fig. 2(d) has the highest potential to achieve the wide-band input matching. However, little work has been reported on the design of a common-gate LNA [16]. This may be due to the fact that the wide-band input matching is not needed in traditional narrow-band receivers, and a common-gate amplifier exhibits relatively lower gain and higher noise figure than a common-source amplifier.

Assuming the input impedance of a common-gate amplifier remains largely resistive and the perfect matching is achieved by setting the transconductance of the active device to 20 mS, the noise factor (F) can be obtained as

$$F = 1 + \frac{\gamma}{\alpha R_s g_m} = 1 + \frac{\gamma}{\alpha} \qquad (1)$$

where γ is the MOS transistor's coefficient of channel thermal noise and α is defined as the ratio of the transconductance g_m and the zero-bias drain conductance g_{d0}, respectively [17]. Given that γ is process dependent and difficult to control, the noise performance can be optimized by increasing the
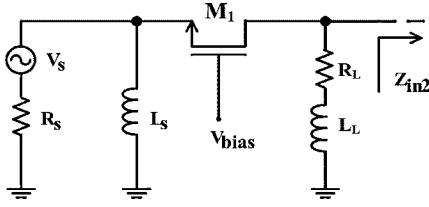
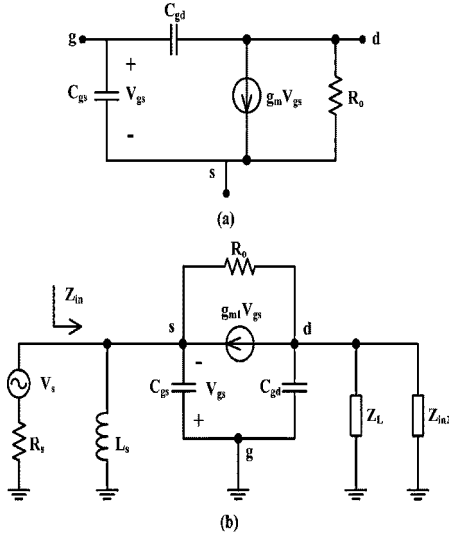Fig. 3. Configuration of a common-gate input stage.

Fig. 4. (a) MOS transistor small-signal model and (b) its usage in common-gate stage input impedance derivation.

transconductance of the MOS transistor, i.e., trading off the 50-Ω input matching.

III. CIRCUIT ANALYSIS

The actual configuration of the common-gate stage (see Fig. 3) is more complex than that shown previously in Fig. 2(d). An inductor, L_s, is placed between the source of the MOS transistor and the ground terminal forming an *LC* resonator with the gate-to-source capacitance C_{gs} in common-gate configuration. The finite output resistance of the transistor also influences the performance of the LNA. It is observed in Fig. 3 that the load impedance of the common-gate stage and the input impedance of the next stage will degrade the matching and noise performance due to the short-channel MOS transistor's relatively low output resistance which is generally around 500 Ω for a 0.18-μm CMOS process [27]. The relatively low gain of a common-gate amplifier is another important design consideration, as 15 dB of gain is targeted to amplify the received UWB signal. The small-signal model of the transistor employed in the analysis is given in Fig. 4(a), in which the gate-to-drain parasitic capacitance C_{gd} and the finite output resistance R_o are both included to observe the influence of the important parasitics on the performance of the proposed LNA.

A. Input Matching

The small-signal equivalent circuit for the impedance calculation is given in Fig. 4(b). Z_L is the impedance of the load, Z_{in2}

is the input impedance of the next stage and g_{m1} is the transconductance of the MOS transistor in common-gate configuration. The input impedance can be derived as

$$Z_{\text{in}} = \frac{1}{g_{m1} + \frac{1}{Z_S(\omega)} + \frac{1 - g_{m1}Z_o(\omega)}{R_o + Z_o(\omega)}} \qquad (2)$$

where $Z_S(\omega)$ and $Z_o(\omega)$ are given by (3) and (4) below, respectively

$$Z_S(\omega) = j\omega L_s // \frac{1}{j\omega C_{gs}} = \frac{j\omega L_s}{1 - \omega^2 C_{gs} L_s} \qquad (3)$$

$$Z_o(\omega) = \frac{1}{j\omega C_{gd}} // Z_L // Z_{\text{in}2} \qquad (4)$$

In fact, the term $(1 - g_{m1}Z_o(\omega))/(r_o + Z_o(\omega))$ in the denominator of (2) is introduced by the finite output resistance of the MOS transistor R_o due to channel length modulation effect. To obtain more insight on the impact of R_o on the input impedance, we may assume that $Z_S(\omega)$ and $Z_o(\omega)$ are both composed of high-Q inductors and capacitors and can thus be regarded as purely reactive within the frequency band of interest

$$Z_S(\omega) = jX_S(\omega) \qquad (5)$$

$$Z_o(\omega) = jX_o(\omega). \qquad (6)$$

Equation (2) can be re-written by substituting (5) and (6) into (2) and we get

$$\begin{aligned}
Z_{\text{in}} &= \frac{1}{g_{m1} - j\frac{1}{X_S(\omega)} + \frac{1 - jg_{m1}X_o(\omega)}{R_o + jX_o(\omega)}} \\
&= \frac{1}{\left(g_{m1} - \frac{g_{m1} \cdot X_o^2(\omega) - R_o}{R_o^2 + X_o^2(\omega)}\right) - j\left(\frac{1}{X_S(\omega)} + \frac{1 + g_{m1} \cdot R_o}{R_o^2 + X_o^2(\omega)} \cdot X_o(\omega)\right)}.
\end{aligned} \qquad (7)$$

The term $1/X_S(\omega)$ in (7) dominates the imaginary part because $g_{m1}R_oX_o(\omega) << R_o^2 + X_o^2(\omega)$ throughout the frequency of interest. Since $g_{m1}X_o^2(\omega) << R_o^2 + X_o^2(\omega)$, the real part in the denominator will remain relatively constant within the 3.1–10.6-GHz UWB band.

Some observations can be made based on the foregoing derivations: The transconductance of the MOS transistor in common-gate configuration should be set slightly greater than 20 mS for better matching due to the effect of the MOS transistor's finite output resistance R_o. The imperfect matching of the common-gate stage throughout the band arises from the frequency dependent $X_S(\omega)$ that dominates the imaginary part in the denominator, i.e., the impedance of the *LC* tank formed by L_s and C_{gs}. To get a good matching over the wide band, L_s and C_{gs} should be selected such that they resonate at the center of the 3.1–10.6 GHz, leaving only a 50-Ω real input impedance.

Simulations show that best input matching is achieved over the 7500-MHz bandwidth with a MOS transistor with an aspect ratio of 120 μm/0.18 μm and L_s of 7.46 nH. As shown in Fig. 5, the best input matching is achieved while g_{m1} is 21.8 mS and input matching degrades with the further increase of g_{m1}. The
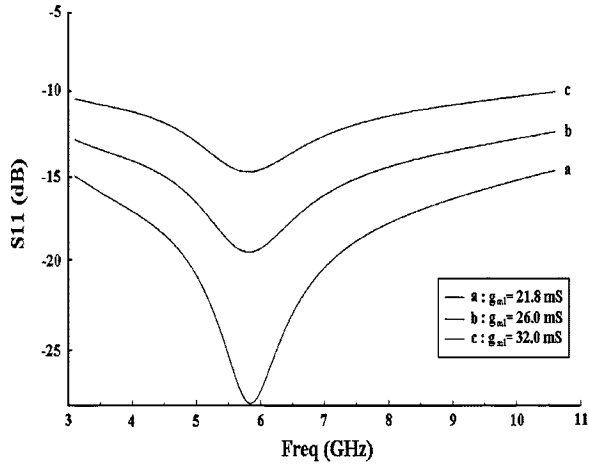
Fig. 5. S11 versus transconductance of the common-gate input matching architecture.

Fig. 6. Illustration of the gain and bandwidth enhancement method with simulation result.

highest g_{m1} that keeps S11 below -10 dB over the entire UWB bandwidth is 32 mS.

B. Gain Analysis and Variable Gain Mechanism

In order to effectively amplify the low PSD UWB signal at the receiver, a relatively high gain is desired for the LNA. For example, the LNA proposed in [11] provides a gain of 15 dB over the UWB bandwidth, and even higher gain is targeted in the design stage so as to compensate for the possible implementation loss due to process variations. Meanwhile, as the development of the other blocks in the UWB receiver front-end is still on the way, a variable gain mechanism is desired in the LNA so that it can be incorporated into different UWB receivers with different link budgets without significant modifications.

In general, a resistor is employed as the load of a wide-band amplifier with a series inductor. This combination boosts the load impedance at high frequency. However, such a load is not applicable for a common-gate LNA because the resistor substantially degrades the noise performance of the circuit. Thus, a single inductor serves as the load for our design. It resonates with the total capacitance at the output of the common-gate stage, but limits the bandwidth of the amplifier. A new technique is introduced here to broaden the bandwidth while enhancing the gain of the amplifier. Two common-source stages with inductive loads are added after the common-gate stage to increase the gain of the amplifier. The three inductive loads are selected so that they resonate with the total capacitance at the output node of each stage at three different frequencies within the 3.1- to 10.6-GHz band. Consequently, with proper tuning of the three frequency points, the bandwidth and the gain of the amplifier are both enhanced.

Fig. 6 illustrates the proposed bandwidth and the gain enhancement technique, and shows the simulation result for the power gain. The graph indicates that a relatively high while flat gain of 15.4–18.7 dB is achieved on the 3.1- to 10.6-GHz UWB band justifying our enhancement technique. However, more have to be done to compensate for the implementation losses. As can be found in many wide-band amplifier design works, the measured gain is less than the simulated gain, which is probably due to the EM radiation loss and the substrate loss
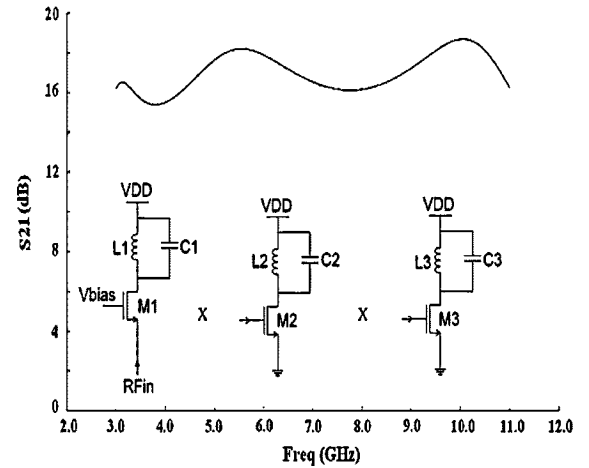
of the silicon process. Furthermore, such loss increases with frequency. Therefore, the loss at the high-end of the frequency band is assumed to be 3 dB higher than that at the low-end around the nominal gain of 15 dB, and this assumption is verified in Section V by the post-layout simulation, in which the substrate loss has been taken into consideration.

C. Noise Analysis and Optimization

Extra attention should be given to the noise characteristics of the proposed LNA as it employs a common-gate stage to achieve wide-band input matching, which is generally noisier than the narrow-band matching techniques such as inductive source degeneration. In order to optimize the noise performance, the MOS transistor noise model with the induced gate noise and the channel thermal noise is employed for the analysis (see Fig. 7) [28]. In Fig. 7, $\overline{i_{n,d}^2}$ is the PSD of the channel thermal noise which is given as

Fig. 7. MOS transistor noise model including the induced gate noise.

$$\frac{\overline{i_{n,d}^2}}{\Delta f} = 4kT\gamma g_{d0} \qquad (8)$$

where k is the Boltzmann constant, T is the absolute temperature in Kelvin, g_{d0} is the zero-bias drain conductance, and Δf is the bandwidth over which the noise figure is measured [27]–[29]. The PSD of the induced gate noise is given by

$$\frac{\overline{i_{n,g}^2}}{\Delta f} = 4kT\delta g_g \qquad (9)$$

where δ is the coefficient of the induced gate noise and g_g is the equivalent shunt gate conductance, which is given by $g_g =$
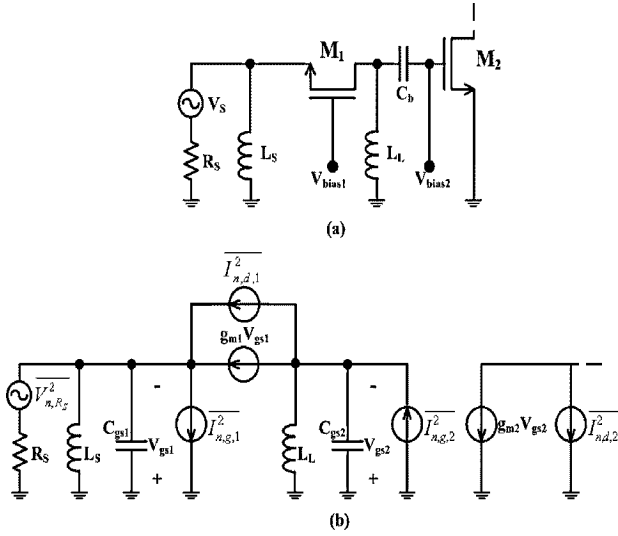
Fig. 8. Noise calculation of the common-gate stage cascaded by a common-source stage. (a) Basic schematic. (b) Equivalent small-signal circuit.

$\omega^2 C_{gs}^2/5g_{d0}$. Typically, δ is 4/3 for long-channel devices, and it increases in short-channel devices [27]–[29]. The induced gate noise is partially correlated with the channel thermal noise, with a correlation coefficient c, given by

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}}. \tag{10}$$

Theoretically, $c = -0.395j$ for long-channel devices with the noise current direction defined in Fig. 7, and its magnitude decreases as the channel gets shorter [27]. Thus, the induced gate noise can be divided into two parts as shown in Fig. 7: The first part is fully correlated with the channel thermal noise with a PSD given by $\overline{i_{n,g,c}^2}/\Delta f = 4kT\delta g_g|c|^2$ and the second part is fully uncorrelated with the channel thermal noise with a PSD given by $\overline{i_{n,g,u}^2}/\Delta f = 4kT\delta \cdot g_g \cdot (1 - |c|^2)$.

Due to the low gain of the common-gate stage, the noise contribution of the subsequent stages cannot be simply neglected. We perform the noise figure calculation at the output of the second common-source stage so as get a more accurate approximation of the noise performance of the whole amplifier. Based on the schematic of the circuit for noise analysis and its small-signal equivalent circuit given in Fig. 8, the output noise PSD contributed by the source resistor is given as

$$S_{n,R_s} = \frac{4kTR_s g_{m1}^2 g_{m2}^2 |Z_o(\omega)|^2}{(1 + g_{m1}R_s)^2 + \frac{R_s^2}{|Z_s(\omega)|^2}}. \tag{11}$$

The noise contributed by the part of the induced gate noise in M_1 that is fully uncorrelated with the drain noise is given by

$$S_{n,g,u,1} = \frac{4kT\alpha\delta \cdot (1 - |c|^2) \cdot \omega^2 C_{gs1}^2 R_s^2 g_{m1} g_{m2}^2 |Z_o(\omega)|^2}{5 \cdot \left[(1 + g_{m1}R_s)^2 + \frac{R_s^2}{|Z_s(\omega)|^2}\right]}$$

$$= \frac{\alpha\delta \cdot (1 - |c|^2) \cdot \omega^2 C_{gs1}^2 R_s}{5 \cdot g_{m1}} \cdot S_{n,R_s}. \tag{12}$$

The output noise PSD due to the two noise sources in M_1 is then given by

$$S_{n,g,d,c,1} = \left[\frac{\gamma}{\alpha R_s g_{m1}}\left(1 + \frac{R_s^2}{|Z_s(\omega)|^2}\right) \right.$$

$$+ \frac{\alpha\delta \cdot |c|^2 \omega^2 C_{gs1}^2 R_s}{5g_{m1}}$$

$$+ \left. \frac{2 \cdot |c|\sqrt{\frac{\delta\gamma}{5}}\omega C_{gs1}R_s}{jg_{m1}Z_s(\omega)} \right] \cdot S_{n,R_s} \tag{13}$$

where the first term is contributed by the channel thermal noise of M_1, the second term by the correlated part of the induced gate noise, and the last term arises from the correlation of these two noise sources. Similarly, the noise contributions by M_2 are given in (14) and (15), respectively

$$S_{n,g,u,2}$$
$$= \left\{ \frac{\alpha \cdot \delta(1 - |c|^2) \cdot \omega^2 C_{gs2}^2}{5R_s \cdot g_{m2}} \right.$$
$$\left. \cdot \left[\left(\frac{1}{g_{m1}} + R_s\right)^2 + \frac{R_s^2}{g_{m1}^2 \cdot |Z_s(\omega)|^2} \right] \right\} \cdot S_{n,R_S} \tag{14}$$

$$S_{n,g,d,c,2}$$
$$= 4kT\frac{\gamma}{\alpha}g_{m2}$$
$$+ \frac{4}{5}kT\alpha\delta \cdot |c|^2 \omega^2 C_{gs2}^2 \cdot |Z(\omega)|^2$$
$$- j8kTg_{m2}Z_o \cdot |c| \cdot \omega C_{gs2}\sqrt{\frac{\gamma\delta}{5}}$$
$$= \left(\frac{\gamma}{\alpha R_s g_{m2}|Z_o(\omega)|^2} \right.$$
$$+ \left. \frac{\alpha\delta|c|^2\omega^2}{5R_s\omega_{T2}^2} + \frac{2Z_o|c|\omega\sqrt{\frac{\gamma\delta}{5}}}{jR_s\omega_{T2}|Z_o(\omega)|^2} \right)$$
$$\cdot \left[\left(\frac{1}{g_{m1}} + R_s\right)^2 + \frac{R_s^2}{g_{m1}^2|Z_S(\omega)|^2} \right] \cdot S_{n,R_S}. \tag{15}$$

The noise factor of the common-gate input stage cascaded by a common-source stage can now be derived from (11)–(15). Following the definition in [17], the noise factor is derived as

$$F = 1 + \frac{S_{n,g,u,1} + S_{n,g,d,c,1} + S_{n,g,u,2} + S_{n,g,d,c,2}}{S_{n,R_s}}$$

$$= F_1 + \frac{S_{n,g,u,2}}{S_{n,R_S}} + \frac{S_{n,g,d,c,2}}{S_{n,R_S}} \tag{16}$$

where F_1 is the noise factor of the single common-gate stage, excluding the effect of the noise contributed by the common-source stage which is given by the later two terms. The expression of F_1 is given as

$$F_1 = 1 + \frac{\alpha\delta \cdot (1 - |c|^2) \cdot \omega^2 C_{gs1}^2 R_s}{5 \cdot g_{m1}}$$

$$+ \frac{\gamma}{\alpha R_s g_{m1}}\left(1 + \frac{R_s^2}{|Z_s(\omega)|^2}\right)$$

$$+ \frac{\alpha\delta|c|^2\omega^2 C_{gs1}^2 R_s}{5g_{m1}} + \frac{2|c|\sqrt{\frac{\delta\gamma}{5}}\omega C_{gs1}R_s}{jg_{m1}Z_s(\omega)}. \tag{17}$$

In (17), it can be observed that two approaches are available to suppress the noise figure.

1) L_s and C_{gs1} can be selected such that they resonate around the center of the 3.1- to 10.6-GHz band ensuring a maximum $|Z_s(\omega)|$ at that frequency point and maximize the average $|Z_s(\omega)|$ value over the whole 7500-MHz bandwidth. Fortunately, this coincides with the requirement on L_s and C_{gs1} for better matching as discussed above.

2) As g_{m1} appears in the denominators of all noise components, we can increase it to reduce the overall noise. However, the input matching degrades as g_{m1} increases (see Fig. 5). Nevertheless, S11 is still below -10 dB as we increase g_{m1} to our tradeoff value of 32 mS. Similarly, in (16), to minimize the noise contribution of the common-source stage, g_{m2} and ω_{T2} can be increased to minimize the noise contribution from the second stage. We should note that since the noise is mostly dependent on the first stage, this modification may not be that effective.

The choice of load inductor L_L and the transistor aspect ratios are also important. It is obvious in (17) that a smaller C_{gs1} will result in a lower noise figure. On the other hand, scaling down the width of M_1 means more current is consumed to maintain the same g_{m1}. Therefore, the M_1 width should be chosen as large as possible within the tolerable noise performance. $Z_o(\omega)$ in (16) is determined by the common-gate stage load inductance L_L and the total capacitance at the drain of M_1, i.e., $C_{\mathrm{gs2}}+C_{\mathrm{gd1}}$. An L_L value is employed such that L_L and $C_{\mathrm{gs2}}+C_{\mathrm{gd1}}$ resonate around the center of the band to avoid the boosting of noise figure at the marginal band where $|Z_o(\omega)|$ decreases greatly. The choice of L_L will yield a better noise performance around the center of the band when compared to the performance at both ends of the band (3.1 or 10.6 GHz) as the gain of the first stage reaches its minimum at those two frequencies and the noise contribution of the following stages becomes significant.

A low-Q inductor load is preferred because it reduces the overall noise as the average noise figure decreases with a slight increase in the minimum achievable value. Furthermore, accommodating the design in a CMOS technology with low-Q inductors is easier. The employment of a high-Q inductor as the load of the common-gate stage would result in a better minimum-achievable noise figure at the *center* of the band, but it would generate significant ripples in the gain curve.

Preliminary simulations show that the noise figure is kept below 4 dB over the entire bandwidth with an average noise figure of only 3 dB, which is acceptable for UWB applications. It is expected that the noise figure will increase in the post-layout simulation due to the parasitic effects. Nevertheless, the principles discussed in this section still apply to the optimization of the CMOS UWB LNA noise performance.

IV. Circuit Design

The design of the proposed CMOS UWB LNA is based on the Chartered Semiconductor Manufacturing (CHRT) 0.18-μm 1.8-V standard RFCMOS technology. For high frequency performance and minimum parasitic capacitances, a minimum channel length of 0.18 μm is chosen for all the transistors employed in the proposed circuit. The schematic of the proposed
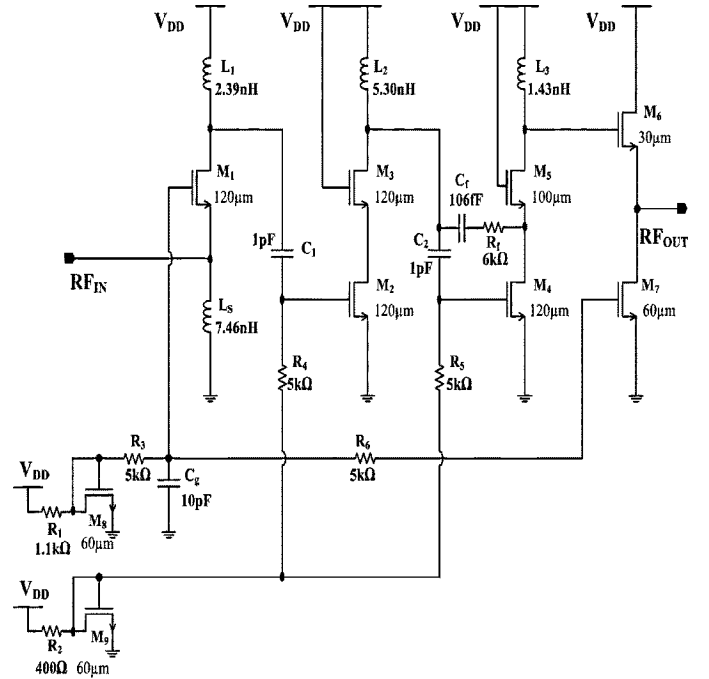

Fig. 9. Schematic of the proposed CMOS UWB LNA (with biasing circuit).

CMOS UWB LNA including the output buffer and the biasing circuit is shown in Fig. 9.

For the maximum transconductance of 32 mS (dictated by the matching criteria) with a given biasing current, the M_1 width is set to be 120 μm, with the source inductor chosen as 7.46 nH. A large capacitor of 10 pF is connected between the M_1 gate and the ground terminal to ensure a good AC grounding and to bypass the noise contributed by the biasing circuit.

Selection of M_2 width is critical due to the restriction that an inductor must be available in the component library provided by the CHRT PDK to resonate with $C_{\mathrm{gd1}}+C_{\mathrm{gs2}}$ around the center of the frequency band. Iterative simulations indicate that for the best noise performance; L_1 is chosen to be 2.39 nH while the M_2 width is 120 μm. It is worth mentioning that although M_1 and M_2 possess the same aspect ratios and the value of L_1 is much smaller than that of L_s, the resonant frequency of the LC tanks formed by L_s with C_{gs1} and L_1 with $C_{\mathrm{gs2}}+C_{\mathrm{gd1}}$ are expected to be both around the center of the frequency band. This is due to the existence of C_{gd1} and the parasitic capacitance introduced by the coupling capacitor C_1.

A cascode transistor is added for both of the two common-source stages to mitigate the Miller effect that would introduce additional problems in the selection of the peaking frequency. Furthermore, the cascode structure improves the reverse isolation and gain of the amplifier without additional power consumption.

A source-follower has been added as an output buffer for testing purposes. The output impedance is given as

$$Z_{\mathrm{out}}(\omega) = \frac{1+j\omega Z_3(\omega)C_{\mathrm{gs6}}}{g_{m6}+j\omega C_{\mathrm{gs6}}}//r_{o6}//$$

$$r_{o7} \approx \frac{1+j\omega Z_3(\omega)C_{\mathrm{gs6}}}{g_{m6}+j\omega C_{\mathrm{gs6}}} \tag{18}$$

Fig. 10. Input reflection coefficient.
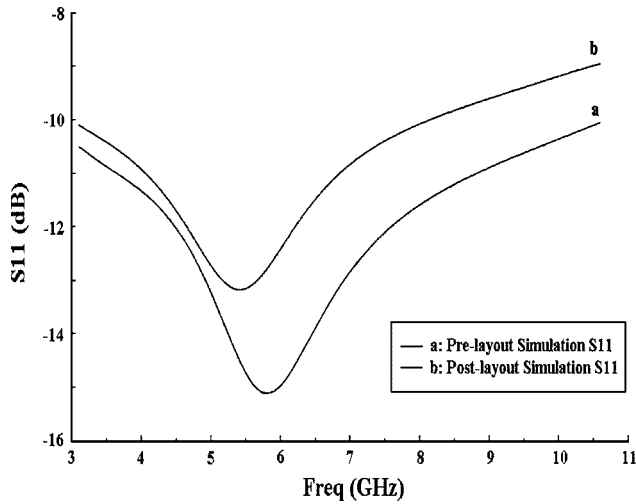

Fig. 11. Power gain.

where $Z_3(\omega)$ is the impedance of the *LC* tank formed by L_3 with $C_{gd5} + C_{gd6}$. To avoid the degradation of in-band output matching, a small inductance value of 1.43 nH is selected for L_3, achieving the highest peak. Meanwhile, a smaller C_{gs6} is desired to minimize the degradation as can be observed in (18), thus the width of the source follower transistor, M_6, is set to be only 30 μm.

With the selection of the frequency of the two peaks for input and output matching as well as noise consideration, the peak generated by L_2 with $C_{gs4} + C_{gd3}$ is determined to be at the lowest frequency of the three. The width of M_4 and the inductance of L_2 are found to be 120 μm and 5.30 nH, respectively for best gain flatness. The Q-factor of the inductors in modern CMOS technology generally vary significantly with frequency, thus a feedback resistor is introduced between the drain of M_4 and M_3, to damp the Q-factor of L_2 for better gain flatness.

The circuit is biased by means of current mirrors. To minimize the power consumption, the common-gate stage shares the same current mirror that biases the source-follower, while the two cascode stages shares another. The resistors R_3, R_4, R_5 are added for signal choking, while R_6 ensures good reverse isolation by forming a low pass filter with C_g. By adjusting the resistance of R_2, we can determine the biasing current and the transconductance of both cascode stages to adjust the overall gain of the LNA.

V. PERFORMANCE SUMMARY

The circuit simulations of the proposed design are performed in Cadence SpectreRF. The layout has been drawn and the parasitic effects have been extracted and taken into account in the post-layout simulations. Optimization has been performed in the post-layout simulation and the performance of the proposed CMOS UWB LNA is summarized in this section.

Fig. 10 shows the input reflection coefficient in both prelayout and post-layout simulations. S11 is kept below $-$ 10 dB in the pre-layout simulation while 1-dB degradation is observed in the post-layout simulation. This is mainly due to the parasitic capacitance of the input pad, which directly adds to C_{gs1} and
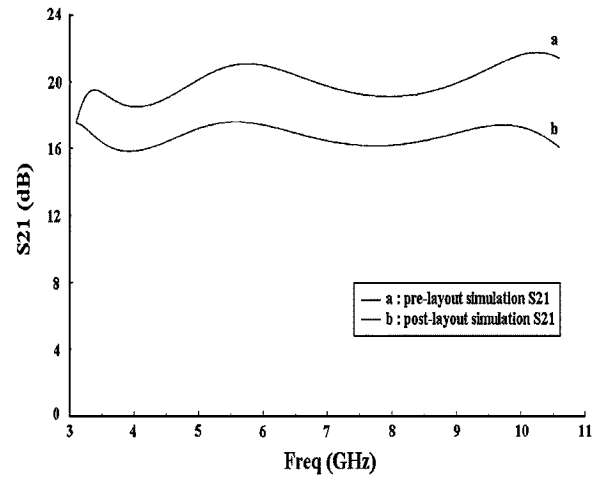
TABLE II
R_2 AND THE CORRESPONDENT POWER GAIN AND POWER CONSUMPTION

$R_2 (\Omega)$	Power Gain (dB)	Power Consumption (mW)
400	15.9-17.5	33.2
500	14.9-16.6	30.5
600	13.8-15.6	28.1
700	12.5-14.3	26.0
800	11.3-13.0	24.3
900	9.9-11.6	22.7

decreases the resonant frequency of the input *LC* tank. Nevertheless, S11 is below -9 dB over the entire 7500-MHz bandwidth, indicating an acceptable input matching.

In Fig. 11, the gain curves in both pre-layout and post-layout simulations are shown. The gain in pre-layout simulation is adjusted to increase with frequency slightly, as discussed previously. The resulting power gain in the post-layout simulation exhibits good flatness, justifying our *"pre-compensation"* technique. The proposed LNA provides 16.7$\pm$0.8 dB of gain over 3.1–10.6 GHz with a power consumption of 33.2 mW. By varying the resistance of R_2, the transconductance of the two cascode stages are both changed effectively to tune the overall gain of the LNA without significantly influencing the other parameters. This feature simplifies the modification of the design when a specific gain value is required for the LNA. Table II gives a set of the gain and power consumption of the proposed LNA corresponding to different values of R_2.

The noise performance of the proposed design is shown in Fig. 12. The noise figures in pre-layout simulation and in the two gain modes of post-layout simulation are compared. The noise figure in the pre-layout simulation is kept below 4.5 dB over the entire band with the gain given in Fig. 11 curve (a). The noise figure is below 5.7 dB with an average value of 4.1 dB in post-layout simulation where the gain is set to 16.7 dB. When the gain drops to 10.8 dB, the noise figure fluctuates by approximately 0.3 dB at the low frequency end and by 1.2 dB at the high frequency end of the band. Thus,
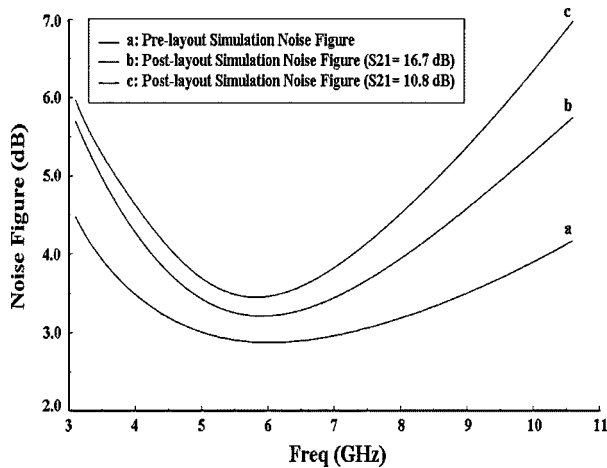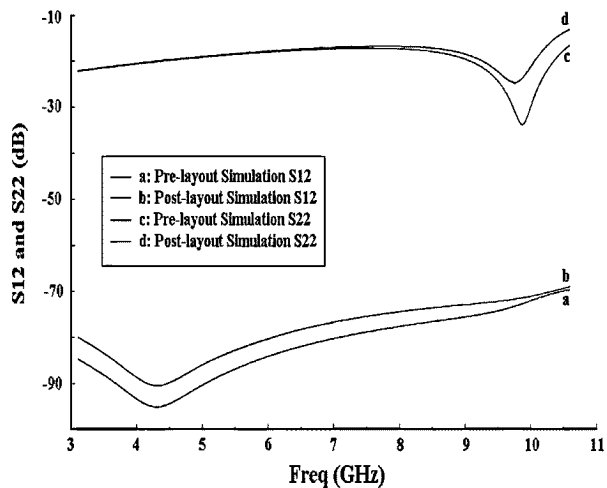
Fig. 12. Noise figure.

Fig. 13. Output matching and reverse isolation.

Fig. 14. Group-delay of the proposed UWB LNA.

Fig. 15. Post-layout simulation of the 1-dB-gain compression point.

variable gain is achieved without a substantial degradation in the noise performance.

The remaining S-parameters of the proposed UWB LNA design are shown in Fig. 13. Output matching S22 is better than − 13 dB and the reverse isolation S12 is higher than 70 dB in the post-layout simulation. For a wide-band application, a constant group-delay is desired to minimize the phase distortion. However, the requirement is not that stringent for an UWB system. As shown in Fig. 14, the group-delay of the proposed design is not constant due to the employment of LC peaking, but the 122 ± 48 ps group-delay of this design is still comparable to that of the recently reported UWB LNA designs [21], [30]. The post-layout simulation result of input-referred 1-dB compression point is shown in Fig. 15. The linearity of the proposed UWB LNA is not as good as many reported narrow-band designs; however, it is sufficient to ensure that the received UWB signal does not suffer from significant gain compression at the LNA stage due to the very low PSD of the signal. In Fig. 16, the layout design of the proposed CMOS UWB LNA is shown. The die size is 0.50 mm^2 (0.74 mm × 0.67 mm), including the pads and the guard ring.

Table III summarizes the performance of the proposed CMOS UWB LNA and makes a comparison of the circuit with the re-
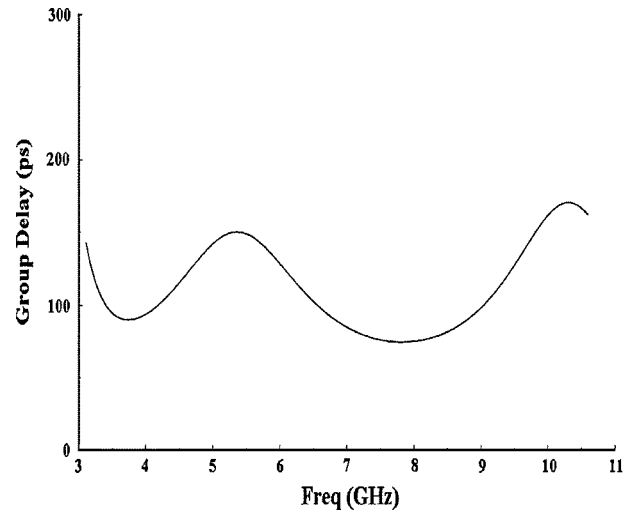

Fig. 16. Layout of the proposed circuit.

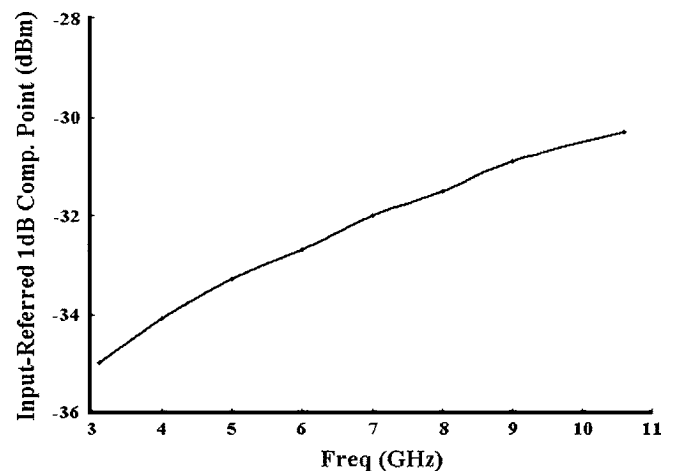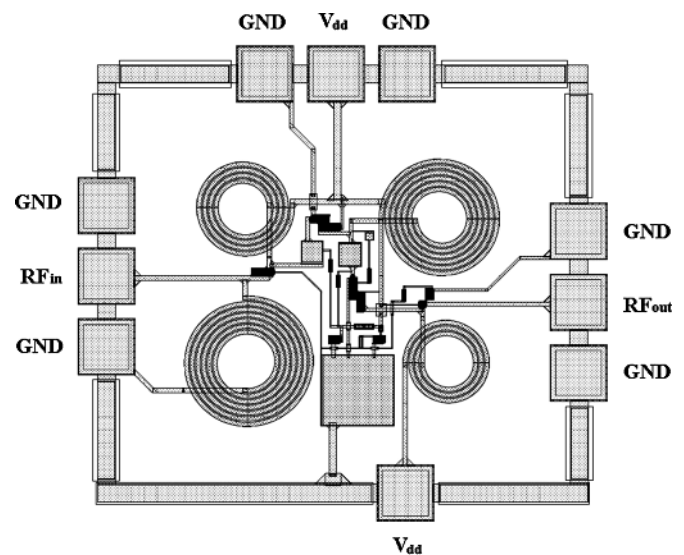cently reported designs. All the wide-band LNA works compared here are based on the conventional transistor-amplifier architecture.

TABLE III
PERFORMANCE SUMMARY OF THE RECENTLY REPORTED WIDE-BAND LNAs
AND THE PROPOSED CMOS UWB LNA

	[19]	[24]	[29]	[30]	This Work
Bandwidth [GHz]	2.4-9.5	2.0-4.6	3.1-4.8	2.0-5.2	3.1-10.6
Power Gain [dB]	7.4-10.4	6.8-9.8	16.4-17.0	15.5-16.5	15.9-17.5
Noise Figure [dB]	4.2-9.0	2.3-3.9	3.9-4.3	4.7-5.7	3.1-5.7
Input Match [dB]	<-9.4	<-9	<-15	<-9	<-9
Output Match [dB]	<-8	<-11	-	<-15	<-13
Supply Voltage [V]	1.8	1.8	1.8	2	1.8
Power Consumption* [mW]	18	16.2	21	38	33.2
Technology	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.13μm CMOS	0.18μm CMOS

*: The power consumption includes the output buffers.

VI. CONCLUSION

This paper demonstrates the design of an UWB LNA based on a standard RFCMOS technology. Acceptable input matching and noise performance are achieved after investigating the tradeoffs between the input impedance of the common-gate stage and its noise performance. By employing the *LC* peaking and pre-compensation techniques, flat gain is achieved over the 7500-MHz UWB spectrum. It is worth mentioning that this technique is especially suitable to realize wide-band designs in CMOS technology since it obviates the need for high-Q spiral inductors. The proposed fully integrated CMOS UWB LNA will be another step towards the implementation of the single-chip UWB transceivers.

REFERENCES

[1] *Ultra-Wide-Band (UWB) First Report and Order* Transl.:Federal Communications Commission (FCC), , Feb. 2002 [Online]. Available: http://hraunfoss.fcc.gov/edocs_public/attachmatch/FCC-02-48A1.pdf, available at

[2] S. Roy, J. R. Foerster, V. S. Somayazulu, and D. G. Leeper, "Ultra-wide-band radio design: The promise of high-speed, short-range wireless connectivity," *Proc. IEEE*, vol. 92, no. 2, pp. 295–311, Feb. 2004.

[3] A. F. Molisch, J. R. Foerster, and M. Pendergrass, "Channel models for ultra-wide-band personal area networks," *IEEE Wireless Commun. Mag.*, vol. 10, no. 6, pp. 14–21, Dec. 2003.

[4] R. M. Narayanan, X. Xu, and J. A. Henning, "Radar penetration imaging using ultra-wide-band (UWB) random noise waveforms," *Proc. IEE Radar, Sonar and Navigation*, vol. 151, no. 3, pp. 143–148, Jun. 2004.

[5] M. Ghavami, L. B. Michael, S. Haruyama, and R. Kohno, "A novel UWB pulse shape modulation system," *Wireless Personal Commun. J.*, vol. 23, no. 1, pp. 105–120, Oct. 2002.

[6] B. Parr, B. Cho, K. Wallace, and Z. Ding, "A novel ultra-wide-band pulse design algorithm," *IEEE Commun. Lett.*, vol. 7, no. 5, pp. 219–221, May 2003.

[7] M. Z. Win and R. A. Scholtz, "Impulse radio: How it works," *IEEE Commun. Lett.*, vol. 2, no. 2, pp. 36–38, Feb. 1998.

[8] M. Welborn, T. Miller, J. Lynch, and J. McCorkle, "Multi-user perspectives in UWB communications networks," in *Proc. IEEE Conf. Ultra Wide-Band Syst. Technol.*, , May 2002, pp. 271–275.

[9] R. Fontana, A. Ameti, E. Richley, L. Beard, and D. Guy, "Recent advances in ultra wide-band communications systems," in *Proc. IEEE Conf. Ultra Wide-Band Syst. Technol.*, , May 2002, pp. 271–275.

[10] *DS-UWB Physical Layer Submission to 802.15 Task Group 3a*, [Online]. Available: ftp://ftp.802wirelessworld.com/15/04/15-04-0137-03-003a-merger2-proposal-ds-uwb-update.doc, available at

[11] *Multi-Band OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a*, [Online]. Available: ftp://ftp.802wirelessworld.com/15/Archive/2003/Jul03/03268r3P802-15_TG3a-Multi-Band-CFP-Document.doc, available at

[12] D. Barras, F. Ellinger, and H. Jäckel, "A comparison between ultra-wide-band and narrow-band transceivers," *TRLabs/IEEE Wireless 2002*, pp. 211–214, Jul. 2002.

[13] H. G. Schantz, G. Wolenec, and E. M. III Myszka, "Frequency notched UWB antennas," in *Proc. IEEE Conf. Ultra Wide-Band Syst. Technol.*, Nov. 2003, pp. 214–218.

[14] Y. Kim and D. H. Kwon, "CPW-fed planar ultra wide-band antenna having a frequency band notch function," *Electron. Lett.*, vol. 40, no. 7, pp. 403–405, Apr. 2004.

[15] S. Sheng, L. Lynn, J. Peroulas, K. Stone, I. O'Donnell, and R. Brodersen, "A low-power CMOS chipset for spread spectrum communications," in *Proc. IEEE 43rd Int. Solid-State Circuits Conf. Dig.*, Feb. 1996, pp. 346–347.

[16] A. Rofougaran, J. Y.-C. Chang, M. Rofougaran, and A. A. Abidi, "A 1 GHz CMOS RF front-end IC for a direct-conversion wireless receiver," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 800–889, Jul. 1996.

[17] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.

[18] A. J. Joseph, "Product applications and technology directions with SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 9, pp. 1471–1478, Sep. 2003.

[19] P. F. Marsh, S. L. G. Chu, S. M. Lardizabal, R. E. Leoni III, S. Kang, R. Wohlert, A. M. Bowlby, W. E. Hoke, R. A. McTaggart, C. S. Whelan, P. J. Lemonias, P. M. McIntosh, and T. E. Kazior, "Low noise metamorphic HEMT devices and amplifiers on GaAs substrates," in *Proc. IEEE MTT-S Int. Microwave Symp. Dig*, Jun. 1999, pp. 105–108.

[20] S. Andersson, C. Svensson, and O. Drugge, "Wide-band LNA for a multistandard wireless Receiver in 0.18um CMOS," in *Proc. ESSCIRC*, Sep. 2003, pp. 655–658.

[21] A. Bevilacqua and A. M. Niknejad, "An ultra-wide-band CMOS low-noise amplifier for 3.1–10.6-GHz wireless receivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.

[22] R.-C. Liu, K.-L. Deng, and H. Wang, "A 0.6–22-GHz broadband CMOS distributed amplifier," in *Proc. IEEE RFIC Symp. Dig.*, Jun. 2003, pp. 103–106.

[23] M.-D. Tsai, K.-L. Deng, H. Wang, C.-H. Chen, C.-S. Chang, and J. G. J. Chern, "A miniature 25-GHz 9-dB CMOS cascaded single-stage distributed amplifier," *IEEE Microw. Wireless Comp. Lett.*, vol. 14, no. 12, pp. 554–556, Dec. 2004.

[24] R. E. Amaya, N. G. Tarr, and C. Plett, "A 27 GHz fully integrated CMOS distributed amplifier using coplanar waveguides," in *Proc. IEEE RFIC Symp.*, Jun. 2004, pp. 193–196.

[25] R. S. Lee, D. D. Wentzloff, and A. P. Chandrakasan, "An ultra-wide-band baseband front-end," in *Proc. IEEE RFIC Symp.*, Jun. 2004, pp. 493–496.

[26] C.-W. Kim, M.-S. Kang, P. T. Anh, H.-T. Kim, and S.-G. Lee, "An ultra-wide-band CMOS low noise amplifier for 3–5-GHz UWB system," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 544–547, Feb. 2005.

[27] C.-H. Chen, M. J. Deen, Y. Cheng, and M. Matloubian, "Extraction of the induced gate noise, channel noise, and their correlation in submicron MOSFETs from RF noise measurements," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2884–2892, Dec. 2001.

[28] A. van der Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986.

[29] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven, and V. C. Venezia, "Noise modeling for RF CMOS circuit simulation," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 618–632, Mar. 2003.

[30] D. Barras, F. Ellinger, H. Jackel, and W. Hirt, "A low supply voltage SiGe LNA for ultra-wide-band frontends," *IEEE Microw. Wireless Comp. Lett.*, vol. 14, no. 10, pp. 469–471, Oct. 2004.

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