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A Novel Composite Nonlinear Controller for Stabilization of Constant Power Load in DC Microgrid

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***Abstract*—Transportation electrification involves the wide utilization of power electronics based DC distribution networks and the integration of a large amount of power electronic loads. These power electronic loads, when tightly controlled, behave as constant power loads (CPLs) and may cause system instability when interacting with their source converters. In this paper, a composite nonlinear controller is proposed for stabilizing DC/DC boost converter feeding CPLs by integrating a nonlinear disturbance observer (NDO) based feedforward compensation with backstepping design algorithm. First, the model is transformed into the Brunovsky's canonical form using the exact feedback linearization technique, to handle the nonlinearity introduced by the CPL. Second, the NDO technique is adopted to estimate the load power variation within a fast dynamic response, serving as a feedforward compensation to increase the accuracy of output voltage regulation. Then a nonlinear controller is developed by following the step-by-step backstepping algorithm with strictly guaranteed large signal stability. The proposed controller not only ensures global stability under large variation of the CPL, but also features fast dynamic response with accurate tracking over wide operating range. Both simulations and experiments are conducted to verify the proposed strategy.**

***Index Terms*—constant power load, large signal stability, backstepping, nonlinear disturbance observer**

I. Introduction

DRIVEN by the demand to reduce gas emissions, decrease operating cost and optimize system performance, transportation sector is going through electrification revolution with the development of more electric aircraft, electric ship, hybrid electric vehicles, etc. [1]–[4]. Power-electronics based DC distribution systems are becoming increasingly common in vehicular power systems, due to their advantages in terms of weight, volume, efficiency, flexibility, isolation, controllability, etc. [5], [6]. The extensive interconnection of power electronics converters, however, lead to a large variety of dynamic interactions and may cause unstable issues. Power electronic converter loads, when tightly controlled, behave as constant power loads (CPLs). CPLs are known to have negative impedance characteristics, which may destabilize the DC bus and consequently, the whole system [1], [5], [7]. Therefore, it is significantly important to explore strategies that can achieve fast dynamic response with guaranteed system stability.

Numerous strategies have been proposed for DC/DC power electronic converter loaded by CPLs. Passive damping strategies, such as adding necessary capacitor or resistor [8] or designing LC filters [9] are simple and effective, whereas they are costly and limited by physical constraints. Active damping methods stabilize the system by modifying control loops to emulate the passive elements, such as virtual capacitor [10], virtual resistor [11] and virtual impedance [12]. These active damping methods are equivalent to injecting stabilizing power into the CPL to increase damping, which may in turn lead to the compromise of load performance. To avoid the compromise of load performance, [4] proposes a stabilizing method by modifying the control loop of source converter to emulate a virtual resistor. But the original converter control loop is still modified and thus system dynamic response is affected. Moreover, all these active damping methods are based on small signal models, they can only ensure small signal stability near the operating point. Therefore, the results are only local and when large disturbance happens, these linear control methods may become ineffective and the system may be unstable.

Taking into consideration of the nonlinearity of converters and the negative-impedance characteristics of CPLs, nonlinear control technologies should be implemented to stabilize system in the large signal sense. In [13], a hybrid model predictive control (MPC) method is proposed for a boost converter feeding a CPL, but the online computational burden of MPC prohibits its practical implementation. Sliding mode control (SMC) is well-known for its strong robustness with guaranteed large signal stability [14]. However, the variable switching frequency requirement will lead to chattering issues and the requirement for measuring output filter capacitor current will lead to a current sensor in series with the capacitor, resulting in higher equivalent series resistance (ESR), which in turn degrades ripple filtering effect and increases output impedance. In [15], a sliding-mode duty-ratio controller is proposed for DC/DC buck converter with CPL at fixed switching frequency. The proposed controller is able to stabilize the DC converter system over the entire operating range with the significant vari-

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ation in load power and input voltage. However, the measurement of dc capacitor current is still required, resulting in the aforementioned weakness. Passivity-based controller strategy is also employed for designing DC/DC boost converter feeding CPLs [16]. This technique utilizes the physical properties of system to achieve a simple control law for stabilization. However, there is high requirement for model accuracy and tracking error exists with the variation of the operating point. This motivates the design of a nonlinear controller that can stabilize system and achieve accurate tracking against uncertainties with easy implementation.

Adaptive backstepping technique is one of the most effective nonlinear control design tools for solving stabilization and tracking problems [17] and it has been applied for power electronic converter systems [18]–[20]. However, the existing literatures only consider resistive load and the implementation of backstepping technique in the case of CPL has not been reported. In addition, due to the nonminimum phase nature of boost converters, backstepping algorithm cannot deal with the objective of output voltage regulation directly and it is indirectly achieved by current/power tracking, which may lead to a non-zero steady-state tracking error due to the uncertain load variation around the nominal resistance. Nonlinear disturbance observer (NDO) is an effective technique to estimate uncertainties/disturbances online for nonlinear systems with minimum information of system dynamics [21], [22]. It attracts much interest as it provides a promising solution for disturbance rejection and uncertainty compensation, which is a key objective during controller design [23]. Based on adaptive backstepping and NDO techniques, this paper proposes a composite nonlinear controller for stabilization of DC/DC boost converter feeding CPL. The dynamic model of boost converter is first converted to the Brunovsky's canonical form for the standard backstepping design. The NDO technique is employed to estimate the uncertain load power variation within a fast dynamic response, which serves as a feedforward compensation for the tracking reference and consequently, achieves fast and accurate tracking of DC bus voltage under large load variations. Then the proposed controller is recursively constructed step by step following the backstepping algorithm. The designed control law not only ensures large signal stability, but also features fast dynamics and accurate tracking at wide operating range. The proposed design procedure is also applicable for the stabilization of other DC/DC converters.

This paper is organized as follows: Section II describes system model and the stability issue to be solved. A composite nonlinear control strategy based on backstepping and NDO techniques is proposed in Section III. Simulation verification and experiment results are shown in Section IV and Section V to demonstrate the effectiveness of the proposed control algorithm. Conclusions are drawn in Section VI.

II. SYSTEM DESCRIPTION AND PROBLEM FOMULATION

A typical DC onboard microgrid is shown in Fig. 1 [4]. The main DC bus is supplied by DC source through DC/DC source converters. As can be observed, there are a great number of

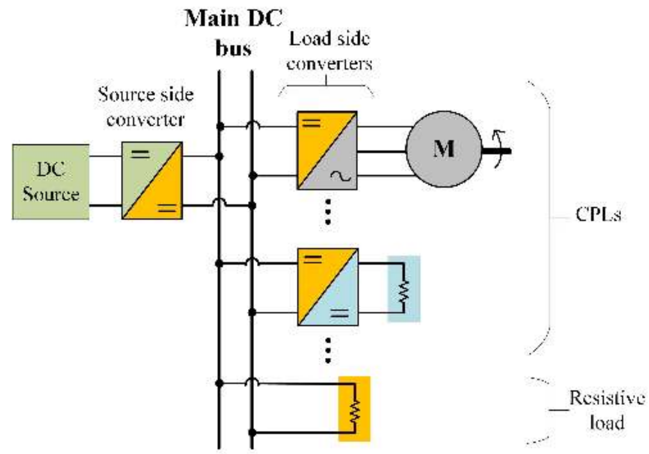

Fig. 1. A typical DC onboard microgrid

DC/DC converter loads and inverter fed motor drive loads integrated in the system. For a DC/DC converter feeding resistive load, as long as the converter output voltage is tightly regulated, the output power of the converter is constant and in turn the input power is almost constant. For an inverter-motor drive system, when its speed is tightly controlled, as torque remains constant for a certain operating period, the output power is constant and the input power of the inverter is constant. These tightly controlled converter loads are known as constant power loads (CPLs).

The voltage-current characteristics of a CPL is given by

$$i_{CPL} = \frac{P_{CPL}}{v_{CPL}} \tag{1}$$

where P_{CPL} is the power of CPL, i_{CPL} and v_{CPL} are the instantaneous values of input current and voltage of the CPL.

The CPL has negative impedance characteristics and this will pose negative impact on system performance [7], especially when the CPL is connected in cascaded with a source converter, it will decrease system damping or even cause instability.

Fig. 2 shows a simplified dc distribution system, i.e. an energy source provides DC power through a DC/DC boost converter, feeding a CPL. The lumped resistive load is denoted as R and the lumped CPL is represented by a controlled

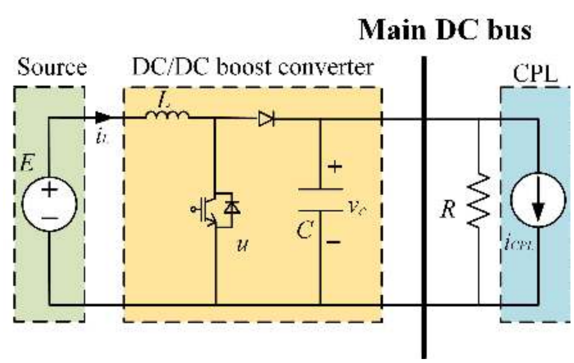

Fig. 2. The simplified DC distribution system

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current source based on power of CPL P_{CPL} and bus voltage according to (1). The dynamic model can be represented as

$$\left\{\begin{array}{l} L\frac{di_L}{dt} = E-(1-u)v_C \\ C\frac{dv_C}{dt} = (1-u)i_L - \frac{v_C}{R} - \frac{P_{CPL}}{v_C} \end{array}\right. \quad (2)$$

where i_L and v_C are the instantaneous inductor current and capacitor voltage of boost converter; E is the voltage of energy source; u is the duty ratio of the switch, which represents the control input signal.

The control objective is that the DC-link capacitor voltage v_C should track the reference voltage v_{Cref} even under large disturbances. As resistive load has damping effect and CPL will decrease damping, the worst case in terms of system stability is that the DC load is pure CPL [8]. Since CPL introduces nonlinearity into system, conventional linear controllers are not sufficient to guarantee system stability under large signal disturbances [16]. This motivates the development of a novel nonlinear controller to stabilize CPL, which will be illustrated in the next section.

III. Design of the proposed controller

The design procedure of the proposed composite controller is illustrated in this section. First, the state-space model in (3) is transformed to the canonical form for standard backstepping design. Second, the NDO is employed to estimate the load variation to improve tracking accuracy and system dynamics. Finally the proposed controller is designed by the step-by-step backstepping algorithm with guaranteed globally asymptotical stability.

A. Coordinate transformation

For the design of the proposed backstepping controller, the system model in (2) should first be transformed into the standard form. Based on the result of exact feedback linearization of DC/DC converters [24], a diffeomorphism can be applied in which the new coordinate has the meaning of the total stored energy and rate of change of stored energy, respectively.

The total energy stored in the dynamic system is expressed as

$$x_1 = \frac{1}{2}Li_L^2 + \frac{1}{2}Cv_C^2 \quad (3)$$

Taking the derivative of (3) yields

$$\dot{x}_1 = Li_L\dot{i}_L + Cv_C\dot{v}_C = Ei_L - \frac{v_C^2}{R} - P_{CPL} \quad (4)$$

Based on (4), a new state x_2 and an uncertain term d_1 can be defined as follows

$$x_2 = Ei_L - \frac{v_C^2}{R_0} \quad (5)$$

$$d_1 = -P_{CPL} + \frac{v_C^2}{R_0} - \frac{v_C^2}{R} \quad (6)$$

where R_0 represents the nominal resistance of the resistive load.

Taking the derivative of both sides in (5) yields

$$\begin{aligned} \dot{x}_2 = & \frac{E^2}{L} + \frac{2v_C^2}{R_0^2C} - \left(\frac{Ev_C}{L} + \frac{2i_Lv_C}{R_0C}\right)(1-u) \\ & + \frac{2}{R_0C}\left(P_{CPL} - \frac{v_C^2}{R_0} + \frac{v_C^2}{R}\right) \end{aligned} \quad (7)$$

Now define the intermediate control law v and the uncertain term d_2 as

$$v = \frac{E^2}{L} + \frac{2v_C^2}{R_0^2C} - \left(\frac{Ev_C}{L} + \frac{2i_Lv_C}{R_0C}\right)(1-u) \quad (8)$$

$$d_2 = \frac{2}{R_0C}\left(P_{CPL} - \frac{v_C^2}{R_0} + \frac{v_C^2}{R}\right) \quad (9)$$

Then the system in (2) can be transformed to a canonical form as

$$\left\{\begin{array}{l} \dot{x}_1 = x_2 + d_1 \\ \dot{x}_2 = v + d_2 \end{array}\right. \quad (10)$$

In the system expressed by (10), x_1, x_2 are state variables, d_1 and d_2 are uncertain items and v is the intermediate control signal. As can be observed, the system model is expressed in the Brunovsky's canonical form, which is suitable for the employment of backstepping algorithm.

For the control of DC/DC boost converter, the control objective is to design the control law u so that DC bus voltage v_C can track its reverence value v_{Cref} asymptotically. After the coordinate transformation, the voltage tracking objective is converted to designing the intermediate control law v to achieve the asymptotic tracking of state x_1 to its reference value x_1^*, which is given by

$$x_1^* = \frac{1}{2}Li_{Lref}^2 + \frac{1}{2}Cv_{Cref}^2 = \frac{1}{2}L\left(\frac{P_{ref}}{E}\right)^2 + \frac{1}{2}Cv_{Cref}^2 \quad (11)$$

where P_{ref} is the value of the total load power, expressed as

$$P_{ref} = P_{CPL} + \frac{v_{Cref}^2}{R} \quad (12)$$

Once the intermediate control signal v in (10) is designed, the final control law u in the original system (2) can be obtained according to (8) as

$$u = 1 - \left(\frac{E^2}{L} + \frac{2v_C^2}{R_0^2C} - v\right) \Big/ \left(\frac{Ev_C}{L} + \frac{2i_Lv_C}{R_0C}\right) \quad (13)$$

B. Load power estimation via NDO

It can be observed from (11) and (12) that reference value x_1^* varies with load power, which is an uncertain value and this may cause tracking error. As NDO is an effective technique to estimate uncertainties [23], it is employed to estimate uncertain items d_1, d_2 and total load power in (12) to achieve accurate tracking and fast dynamic response.

Note that the uncertainties d_i (i=1, 2) are related to load power according to (6) and (9), hence from a practical point of view, their values and derivatives should be bounded. Moreover, the load power is seen as constant at steady state. Therefore, the following assumptions can be made:

Assumption 1: The uncertain variables d_i, $\dot{d}_i$, (i=1, 2) for the system (10) satisfy the following two conditions:

$$d_i(t) \in L_\infty, \dot{d}_i(t) \in L_\infty \quad (14)$$

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$$\lim_{t\to\infty} \dot{d}_i = 0 \tag{15}$$

According to NDO in [23], the uncertain item d_1 is estimated by

$$\begin{cases} \hat{d}_1 = l_1(x_1 - p_1) \\ \dot{p}_1 = x_2 + \hat{d}_1 \end{cases} \tag{16}$$

where p_1 is an auxiliary state of the NDO and l_1 is a positive constant, denoted as the NDO gain.

Similarly, the uncertain item d_2 is estimated by

$$\begin{cases} \hat{d}_2 = l_2(x_2 - p_2) \\ \dot{p}_2 = v + \hat{d}_2 \end{cases} \tag{17}$$

where p_2 is an auxiliary state of the NDO and l_2 is a positive constant.

According to (16) and (17), the estimation error of d_i (i=1, 2) and its derivative are expressed as

$$\tilde{d}_i = d_i - \hat{d}_i \tag{18}$$

$$\dot{\tilde{d}}_i = \dot{d}_i - \dot{\hat{d}} = \dot{d}_i - l_i\tilde{d}_i \tag{19}$$

Based on (6), (12) and (16), the total load power P_{ref} in (12) can be estimated as

$$P_{ref} = \frac{v_{Cref}^2}{R_0} - \hat{d}_1 \tag{20}$$

Then the reference value of state x_1 in (11) is reformulated as

$$x_1^* = \frac{1}{2}\frac{L}{E^2}\left(\frac{v_{Cref}^2}{R_0} - \hat{d}_1\right)^2 + \frac{1}{2}Cv_{Cref}^2 \tag{21}$$

C. Recursive backstepping design

Based on the standard model in (10) and load power estimated by NDO, the proposed controller can be designed by following adaptive backstepping algorithm in this section. As the design objective is to enforce the state variables x_1 and x_2 to track their desired values x_1^* and x_2^* asymptotically, a new set of coordinate is introduced as

$$\begin{aligned} z_1 &= x_1 - x_1^* \\ z_2 &= x_2 - x_2^* \end{aligned} \tag{22}$$

Step 1:

Taking the derivative of z_1 along its trajectory yields

$$\dot{z}_1 = z_2 + x_2^* + d_1 - \dot{x}_1^* \tag{23}$$

Consider the Lyapunov function defined as

$$V_1 = \frac{1}{2}z_1^2 + \frac{1}{2}\tilde{d}_1^2 \tag{24}$$

The derivative of (24) along its trajectory is

$$\dot{V}_1 = z_1(x_2^* + z_2 + \hat{d}_1 - \dot{x}_1^*) + z_1\tilde{d}_1 - l_1\tilde{d}_1^2 + \tilde{d}_1\dot{d}_1 \tag{25}$$

To stabilize (23) with the Lyapunov function (24), the virtual control law x_2^* is designed as

$$x_2^* = -k_1z_1 - \hat{d}_1 + \dot{x}_1^* \tag{26}$$

Then the resulting expression of $\dot{V}_1$ is obtained as

$$\dot{V}_1 = -k_1z_1^2 + z_1z_2 + z_1\tilde{d}_1 - l_1\tilde{d}_1^2 + \tilde{d}_1\dot{d}_1 \tag{27}$$

As is seen from (27), there is no guarantee that $\dot{V}_1$ is negative definite. In the next step, the intermediate control signal v is selected such that this condition is satisfied.

Step 2:

Again taking the derivative of z_2 along its trajectory yields

$$\dot{z}_2 = v + d_2 + k_1\dot{z}_1 + \dot{\hat{d}}_1 - \ddot{x}_1^* \tag{28}$$

Select the Lyapunov function

$$V_2 = V_1 + \frac{1}{2}z_2^2 + \frac{1}{2}\tilde{d}_2^2 \tag{29}$$

whose derivative is expressed as

$$\begin{aligned} \dot{V}_2 = &-k_1z_1^2 + z_1z_2 + z_1\tilde{d}_1 - l_1\tilde{d}_1^2 + \tilde{d}_1\dot{d}_1 + z_2[v + d_2 \\ &+ k_1(z_2 - k_1z_1 + \tilde{d}_1) + l_1\tilde{d}_1 - \ddot{x}_1^*] - l_2\tilde{d}_2^2 + \tilde{d}_2\dot{d}_2 \end{aligned} \tag{30}$$

To stabilize (28) with the Lyapunov function (29), the intermediate control law v is designed as

$$v = -k_2z_2 - \hat{d}_2 + \ddot{x}_1^* \tag{31}$$

Theorem 1: The closed-loop system consisting of (2), (10), (22), (26) and (31) is globally asymptotically stable and DC bus voltage v_C can track its reference value v_{Cref} asymptotically.

Proof. With Lemma 3 in Appendix, following relations hold

$$z_1z_2 \le 0.5z_1^2 + 0.5z_2^2 \tag{32}$$

$$z_1\tilde{d}_1 \le 0.5z_1^2 + 0.5\tilde{d}_1^2 \tag{33}$$

$$\tilde{d}_1\dot{d}_1 \le 0.5\tilde{d}_1^2 + 0.5\dot{d}_1^2 \tag{34}$$

$$z_2k_1(z_2 - k_1z_1) \le 0.5z_1^2 + \left(\frac{k_1^4}{2} + \frac{1}{2k_1^2}\right)z_2^2 \tag{35}$$

$$z_2(k_1 + l_1)\tilde{d}_1 \le 0.5\tilde{d}_1^2 + \frac{(k_1 + l_1)^2}{2}z_2^2 \tag{36}$$

$$\tilde{d}_2\dot{d}_2 \le 0.5\tilde{d}_2^2 + 0.5\dot{d}_2^2 \tag{37}$$

By substituting (32)-(37) into (30) and doing some algebraic manipulations, eqn. (30) can be derived as

$$\begin{aligned} \dot{V}_2 \le &-(k_1 - 1.5)z_1^2 - \left[k_2 - 0.5 - \left(\tfrac{k_1^4}{2} + \tfrac{1}{2k_1^2}\right) - \tfrac{(k_1+l_1)^2}{2}\right] \\ &\cdot z_2^2 \ - (l_1 - 1.5)\tilde{d}_1^2 - (l_2 - 0.5)\tilde{d}_2^2 + \tfrac{1}{2}\dot{d}_1^2 + \tfrac{1}{2}\dot{d}_2^2 \end{aligned} \tag{38}$$

By selecting $l_1 \ge 3$, $l_2 \ge 2$, $k_1 \ge 2.5$ and

$$k_2 \ge \frac{k_1^4}{2} + \frac{1}{2k_1^2} + \frac{(k_1 + l_1)^2}{2} + 1.5$$

the derivative of V_2 can be obtained as

$$\begin{aligned} \dot{V}_2 \le &-(k_1 - 1.5)z_1^2 - \left[k_2 - 0.5 - \left(\tfrac{k_1^4}{2} + \tfrac{1}{2k_1^2}\right) - \tfrac{(k_1+l_1)^2}{2}\right] \\ &\cdot z_2^2 \ - (l_1 - 1.5)\tilde{d}_1^2 - (l_2 - 0.5)\tilde{d}_2^2 + \tfrac{1}{2}\dot{d}_1^2 + \tfrac{1}{2}\dot{d}_2^2 \end{aligned} \tag{39}$$

Since V_2 involves V_1, its stabilization automatically guarantees the stability of the first loop in Step 1. Considering Lemma 1 in Appendix and Assumption 1, and taking $\dot{d}_i$ (i=1, 2) as perturbation inputs, eqn. (39) provides the proof that the closed-loop system of (2), (10), (22), (26) and (31) is globally input-to-state stable (ISS).

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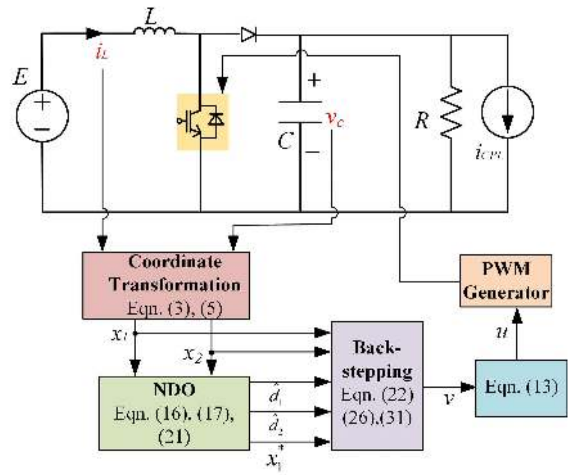

Fig. 3. Control architecture of the proposed controller

By using Lemma 2 and Assumption 1 with (39), the closed-loop ISS system is globally asymptotically stable with $\lim_{t\to\infty} z_1 \to 0$. This implies the asymptotic tracking of x_1 at x_1^* and thus DC bus voltage v_C can track its reference value v_{Cref} asymptotically. □

Based on the procedure developed above, the control architecture of the proposed controller is depicted in Fig. 3.

Remark: It is worth mentioning that the design procedure for the proposed controller is also applicable to other DC/DC converter topologies such as buck converter and buck-boost converter. The system model is first transformed into canonical form in (10) based on exact feedback linearization technique. Then the nonlinear controller for that specific system can be designed by following the NDO estimation procedure in (16)-(21) and the backstepping procedure in (22)-(39). With the NDO and backstepping algorithm, the designed composite controller can achieve fast dynamic response and accurate bus voltage tracking with guaranteed large signal stability.

IV. Simulation results

System model described by Fig. 2 with the proposed controller in Fig. 3 is simulated in Matlab/Simulink to validate the effectiveness of the proposed controller. The system parameters are listed in Table I. As the worst case in terms of stability is pure CPL without resistive load, the nominal resistive load is 0W and R_0 is seen as infinite (set at a very large value such as 100000 Ω). First, the procedure for tuning design parameters is illustrated and then the simulation results under different operating conditions will be presented.

A. Tuning of design parameters

The proposed composite nonlinear controller consists of two NDOs for the load estimation and a backstepping controller for the DC bus voltage regulation. As the NDOs provide the reference value for the backstepping controller, NDOs should be designed first with the control parameters k_1 and k_2 roughly selected as 200 and 2000. Fig.4 shows the dynamic response of the observed load variation when CPL increases from 50W

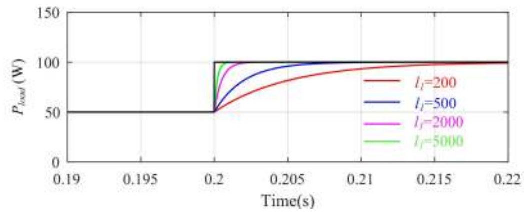

Fig. 4. Load estimation response with different value of l_1

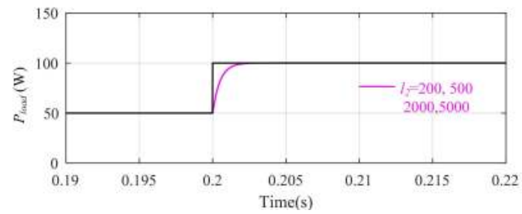

Fig. 5. Load estimation response with different value of l_2

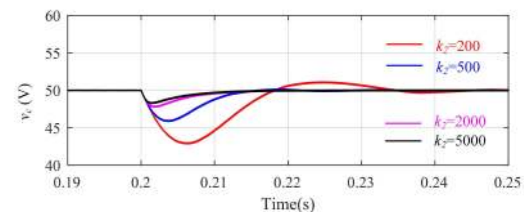

Fig. 6. Voltage tracking response with different values of k_2

to 100W under different values of l_1 (l_1=200, 500, 2000 and 5000), while the NDO gain l_2 is fixed at 200. As can be observed from Fig. 4, the NDOs can track the load variation within a very short transition (in milliseconds) and a larger l_1 will result in a faster convergence rate. Fig. 5 shows the simulation results under different values of l_2 (l_2=200, 500, 2000 and 5000) when l_1 is fixed at 2000. It reveals that the impact of l_2 on system performance is much smaller than that of l_1.

Next, the gains k_1 and k_2 are tuned while the NDO gains l_1 and l_2 are fixed at 2000 and 200. As the objective of the backstepping controller is to regulate the bus voltage to its desired value, the dynamic responses of bus voltage with different controller gains are investigated. The simulation results with different values of k_2 (k_2=200, 500, 2000 and 5000) are shown in Fig. 6 when k_1 is fixed at 200. It is shown that a larger k_2 will lead to a shorter settling time for the voltage tracking. Fig. 7 shows the simulation results with different values of k_1 (k_1=200, 500, 1000, 2000 and 5000) when k_2 is fixed at 2000. It can be observed that a larger k_1 will cause a faster

TABLE I
System Parameters

Variables	Description	Value
V_{Cref}	DC bus voltage reference	50V
E	Converter input voltage	25V
f_s	Switching frequency	20kHz
L	Inductance	1mH
C	Capacitance	0.47mF

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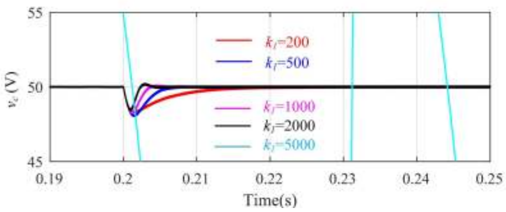

Fig. 7. Voltage tracking response with different values of k_1

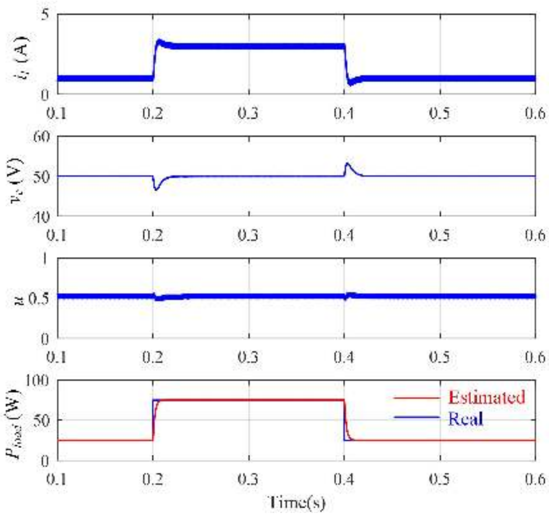

Fig. 8. Simulation results with resistive load and CPL

convergence rate, however, a too large value may lead to large overshoot. It should be noticed that, as a common problem of existing high gain control methods, a larger gain will cause deterioration of system robustness against the measurement noise. Therefore, we should select proper values based on the required system dynamics. Furthermore, as the NDO provides the reference value for the backstepping controller, the dynamic response of load estimation should be designed faster than the voltage tracking dynamics. For example, if the required voltage tracking settling time is within 20ms, the dynamics of load estimation can be expected as around 10ms. Thus l_1 and l_2 can be selected as 500 and 200, while the gains of k_1 and k_2 can be selected at 200 and 2000. This set of the parameters will be used in the simulations and experiments below to verify the effectiveness of the proposed controller and to show its advantage in terms of stability by comparing with the conventional PI controller with similar dynamics.

B. Simulation verification

First, the situation with the integration of both resistive load and CPL is considered and the simulation result is shown in Fig. 8. Originally, there is 25W resistive load at DC bus. Then 50W CPL is connected at 0.2s and disconnected at 0.4s. As can be observed, at each load change period, bus voltage can be enforced to the nominal value within 10ms and the control signal u, which is the duty ratio of the converter, is maintained at 0.5 as expected. Moreover, since the total load power is estimated as (20) by NDO, the effectiveness of NDO

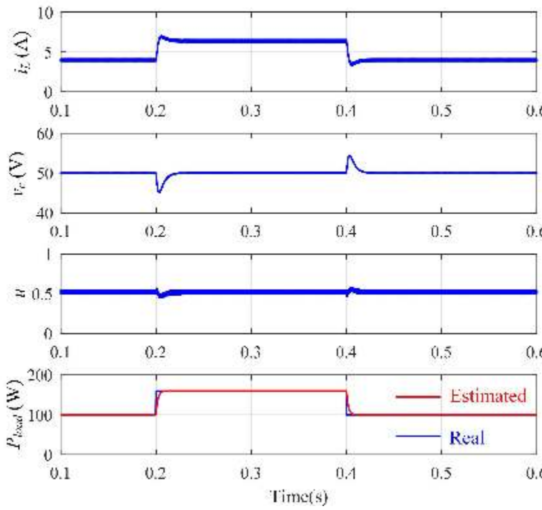

Fig. 9. Simulation results with CPL variation

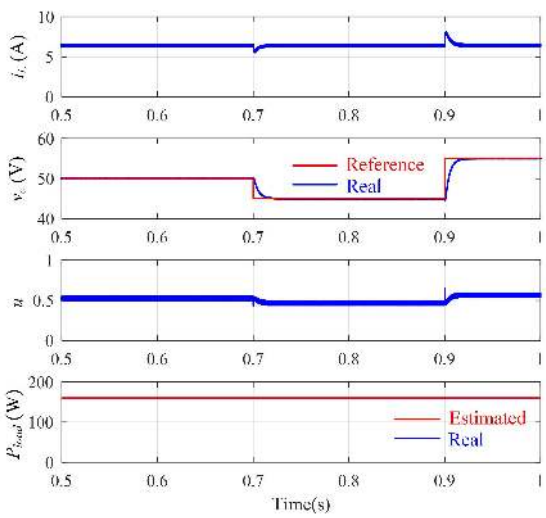

Fig. 10. Simulation results with output voltage variation

estimator is validated by the fourth plot in Fig. 8. It indicates that after each step change, the real value of power variation is tracked by the estimated value within 5ms and the result is quite accurate.

As the worst case is the pure CPL, the resistive load is removed and only CPL is connected to the DC bus. Fig. 9 shows the voltage and current responses caused by the variation of CPL from 100W to 160W at 0.2s and from 160W to 100W at 0.4s. It is shown that system is always stable and its output voltage accurately tracks its reference value at 50V in the presence of large CPL changes.

The system response with the variation of DC bus voltage under the pure CPL condition is shown in Fig. 10. The CPL is maintained at a heavy load condition of 160W. At 0.2s, the DC bus voltage reference value changes from 50V to 45V; at 0.4s, it increases from 45V to 55V. It reveals that bus voltage accurately tracks its reference value within 10ms after the variation, and the duty ratio is at 0.5,0.445 and 0.545

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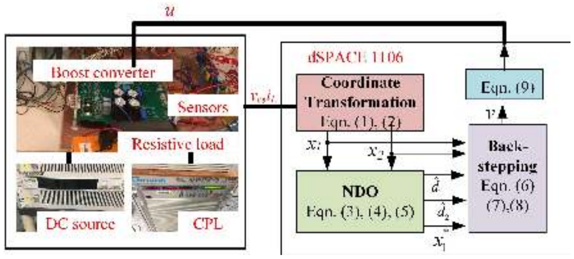

Fig. 11. Experimental setup

for different DC bus voltage reference values.

V. EXPERIMENT RESULTS

The experimental setup shown in Fig. 11 is built in the laboratory to verify the effectiveness of the proposed strategy, which consists of DC power supply, DC/DC boost converter, dSPACE DS1106 and loads. The control algorithm shown in Fig. 3 is implemented in dSPACE to generate PWM signals for DC/DC boost converter with a sampling frequency of 20kHz. Parameters are the same as that listed in Table I and in the simulation verification cases. Chroma programmable load is configured to operate in constant power mode to emulate the CPL. Chroma programmable load and the resistive load are connected to the output of boost converter to generate different loading profiles.

A. System performance under the proposed strategy

Fig.12 shows the dynamic response of the system under the proposed controller with the integration of both resistive load and CPL. Originally, 25W resistive load is connected at the DC bus. At 0.4s, 50W CPL is integrated and at 1.48s, the CPL is disconnected. It can be observed that at each time, voltage responses immediately and can track its reference value accurately with the settling time less than 40ms.

Then the resistive load is removed and the system is loaded by pure CPL. Fig. 13 shows the dynamic response of output voltage, input voltage and inductor current. The original load is set as 100W. Then CPL increases to a heavy load condition of 160W. It is shown that the output voltage accurately tracks its reference value at 50V within 40ms and the system is stable.

The impact of output voltage variation is shown in Fig.14. Only CPL is connected at the DC bus and it is maintained at a heavy load condition of 160W. At 2.1s, when output voltage reference value decreases from 50V to 45V, its real value quickly tracks to the reference value and the inductor current increases a little due to the constant power operation. As can be observed, stable operation is guaranteed under the output voltage variation.

The impact of input voltage variation is shown in Fig. 15. The load maintains at 50W. At 1.1s, the input voltage decreases from 25V to 20V, inductor current increases consequently whereas the output voltage maintains at 50V with negligible disturbance. Thus, the proposed method ensures stable operation under the input voltage variation.

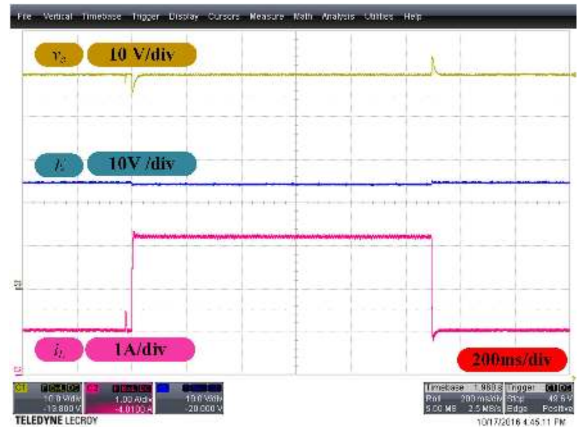

Fig. 12. Experiment results with both resistive load and CPL under the proposed controller

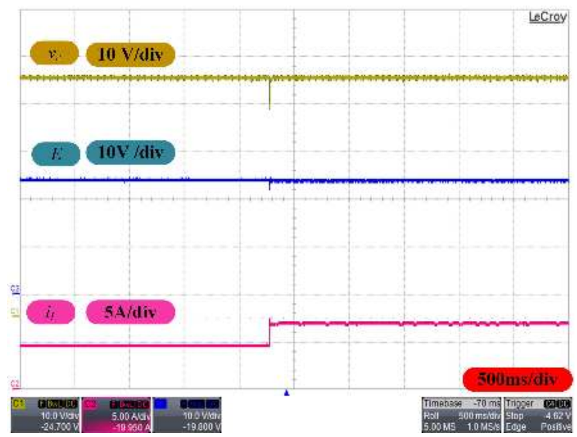

Fig. 13. Experiment results with the variation of large CPL under the proposed controller

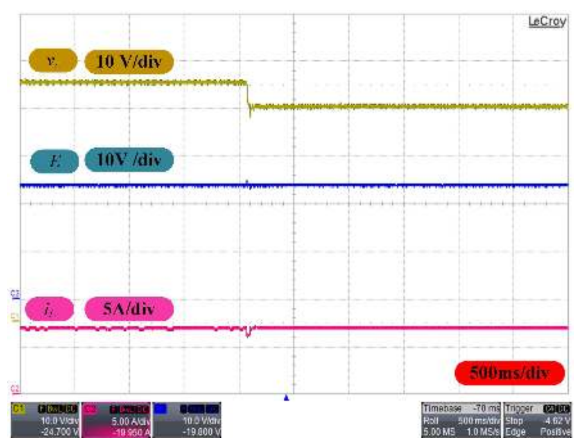

Fig. 14. Experiment results with output voltage variation under the proposed controller

Based on the above results, the proposed controller ensures fast dynamic performance, accurate voltage tracking and guaranteed system stability, being consistent with the theoretical results in Theorem 1 and simulation verification in Section IV-B. There do exist some minor discrepancies between simulation and experimental results. The dynamic response

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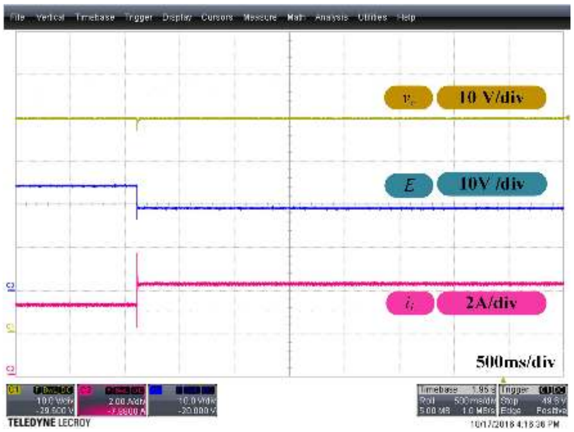

Fig. 15. Experiment results with input voltage variation under the proposed controller

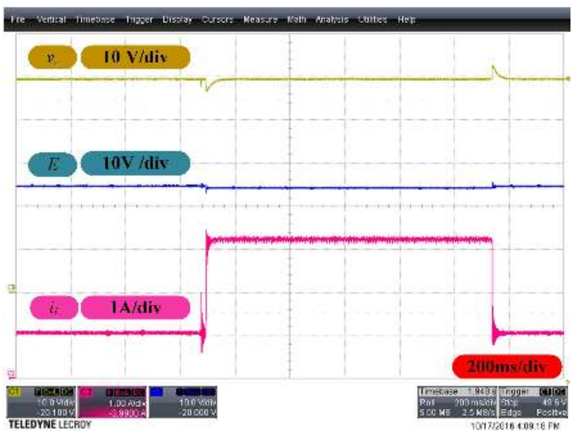

Fig. 16. Experiment results with both resistive load and CPL under conventional PI controller

for experimental case is a bit slower than the corresponding simulation result. This is acceptable because in the simulation studies, we use the ideal constant power load with the step change, whereas in the experimental tests, the variation of CPL (Chroma load in CPL mode) is restricted by its programmable controller bandwidth. Moreover, the experimental results suffer from real-life system conditions such as EMI, noise, ESR, delays and various uncertainties/disturbances, which are not considered in the simulations.

B. Comparison with conventional PI controller

To further illustrate the advantages of the proposed controller, the conventional double-loop PI controller is implemented for the boost converter with inner current loop and outer voltage loop [25].

As PI parameters have impact on system stability and dynamic response, faster dynamics will lead to less stability margin [25]. To have a fair comparison, the PI controller parameters are tuned to have similar dynamic response with the proposed controller. In this case, inner and outer loop PI gains k_{cp}, k_{ci}, k_{vp} and k_{vi} are set at 0.0628, 39.4, 0.8 and 37.1, respectively. Other parameters are the same as that in Table I. Fig. 16 shows the dynamic response under conventional PI

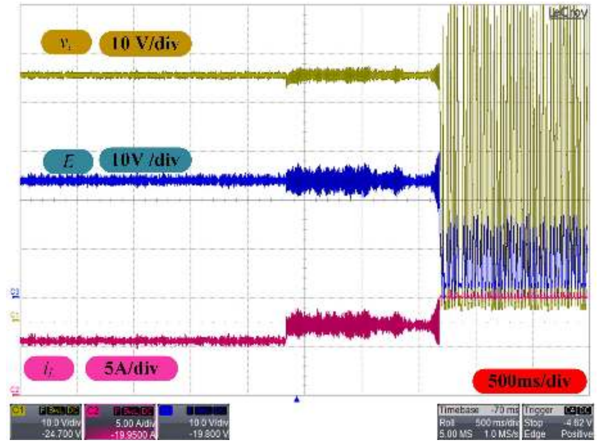

Fig. 17. Experiment results with variation of large CPL under conventional PI controller

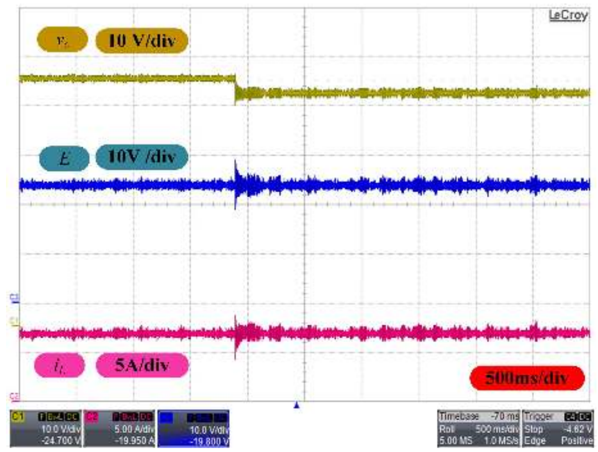

Fig. 18. Experiment results with output voltage variation under conventional PI controller

controller with the same loading profile in Fig. 12. It reveals that with load changes, voltage tracking is achieved with settling time around 40ms, which is similar to that under the proposed strategy. Then stability margin of the two methods are compared.

To compare the stability margin, the case of large CPL variation in Fig.13 is applied for the system under the PI controller. When the CPL steps from 120W to 160W, large oscillation occurs and increases until the system collapses (i.e. the inductor current i_L reaches its upper limit of 10A), as is shown in Fig. 17. But for the proposed controller, the experiment result in Fig. 13 shows accurate voltage tracking under stable operation. With the same loading profile, the proposed strategy achieves the control objective and maintains system stability, whereas the conventional PI controller fails to do so.

Similarly, the impact of output voltage variation implemented in Fig. 14 is investigated for the system with the PI controller in Fig.18. When the output voltage reference value steps down from 50V to 46V with CPL fixed at 150W, large oscillation occurs at the inductor current i_L, as is shown in Fig.18. But the dynamic response in Fig. 14 illustrates that stable operation with accurate tracking is still maintained with the proposed controller under the same condition.

Therefore, based on the above comparisons, with similar dynamic performance, the proposed controller can guarantee accurate voltage tracking with large CPL variation and output voltage variation, which cannot be done by the conventional PI controller.

VI. Conclusion

This paper proposes a composite nonlinear controller for DC/DC boost converter feeding CPL based on NDO and backstepping algorithm. The system model is first converted to the canonical form. The NDO technique is employed to estimate load power within fast dynamic response to ensure accurate voltage tracking. Then followed by a recursive design procedure, the proposed controller is designed with guaranteed large signal stability. Both simulations and experiments are conducted to verify the effectiveness of the proposed controller. The advantages of the proposed controller are further illustrated by its comparison with the conventional PI controller. The proposed controller design procedure is also applicable for stabilization of other DC/DC converters.

Appendix

Preliminaries utilized in the paper during the derivative procedure in Section III are stated as follows:

Consider the following system

$$\dot{x} = f(t, x, u) \tag{A.1}$$

where $f : [0, \infty) \times R^n \times R^m \to R^n$ is a continuous function with $f(0) = 0$.

Definition 1: A continuous function $\alpha : [0, a) \to [0, \infty)$ belongs to class function if it is strictly increasing and $\alpha(0) = 0$. It belongs to class K_∞ functions if $\alpha = \infty$ and $\alpha(r) \to \infty$.

Lemma 1 [26]: Let $V : [0, \infty) \times R^n \to$ be a continuous differentiable function such that

$$\alpha_1(\|x\|) \leq V(t, x) \leq \alpha_2(\|x\|) \tag{A.2}$$

$$\frac{\partial V}{\partial t} + \frac{\partial V}{\partial x} f(t, x, u) \leq -\Gamma(x), \forall \|x\| \geq \rho(\|u\|) > 0 \tag{A.3}$$

$\forall (t, x, u) \in [0, \infty) \times R^n \times R^m$, where α_1, α_2 are class K_∞ functions, ρ is a class K function, and $\Gamma(x)$ is a continuous positive definite function on R^n. Then the system is globally input-to-state stable (ISS).

Lemma 2 [26]: If the system (A.1) is globally input-to-state stable and $\lim_{t\to\infty} u = 0$, then the system is also globally asymptotically stable.

Lemma 3 [27]: Let c, d be positive constants. Given any positive constant , the following inequality holds

$$|x|^c |y|^d \leq \frac{c}{c+d} \gamma^{c/d} |x|^{c+d} + \frac{d}{c+d} \gamma^{-c/d} |y|^{c+d} \tag{A.4}$$

References

[1] A. Emadi, A. Khaligh, C. H. Rivetta, and G. A. Williamson, "Constant power loads and negative impedance instability in automotive systems: definition, modeling, stability, and control of power electronic converters and motor drives," *IEEE Transactions on Vehicular Technology*, vol. 55, no. 4, pp. 1112–1125, 2006.

[2] G. A. Whyatt and L. A. Chick, "Electrical generation for more-electric aircraft using solid oxide fuel cells," *Pacific Northwest National Laboratory*, 2012.

[3] N. Doerry and K. McCoy, "Next generation integrated power system: Ngips technology development roadmap," DTIC Document, Tech. Rep., 2007.

[4] M. Wu and D. D.-C. Lu, "A novel stabilization method of lc input filter with constant power loads without load performance compromise in dc microgrids," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4552–4562, 2015.

[5] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "Dc microgrids-part i: A review of control strategies and stabilization techniques," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4876–4891, 2016.

[6] J. Xiao, P. Wang, L. Setyawan, and Q. Xu, "Multi-level energy management system for real-time scheduling of dc microgrids with multiple slack terminals," *IEEE Transactions on Energy Conversion*, vol. 31, no. 1, pp. 392–400, 2016.

[7] N. Bottrell, M. Prodanovic, and T. C. Green, "Dynamic stability of a microgrid with an active load," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5107–5119, 2013.

[8] A. Kwasinski and C. N. Onwuchekwa, "Dynamic behavior and stabilization of dc microgrids with instantaneous constant-power loads," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 822–834, 2011.

[9] M. Cespedes, L. Xing, and J. Sun, "Constant-power load system stabilization by passive damping," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1832–1836, 2011.

[10] P. Magne, D. Marx, B. Nahid-Mobarakeh, and S. Pierfederici, "Large-signal stabilization of a dc-link supplying a constant power load using a virtual capacitor: impact on the domain of attraction," *IEEE Transactions on Industry Applications*, vol. 48, no. 3, pp. 878–887, 2012.

[11] A. M. Rahimi and A. Emadi, "Active damping in dc/dc power electronic converters: A novel method to overcome the problems of constant power loads," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 5, pp. 1428–1439, 2009.

[12] X. Zhang, X. Ruan, and Q.-C. Zhong, "Improving the stability of cascaded dc/dc converter systems via shaping the input impedance of the load converter with a parallel or series virtual impedance," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7499–7512, 2015.

[13] J. Neely, S. Pekarek, R. DeCarlo, and N. Vaks, "Real-time hybrid model predictive control of a boost converter with constant power load," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, pp. 480–490. IEEE, 2010.

[14] A. P. Tahim, D. J. Pagano, and E. Ponce, "Nonlinear control of dc-dc bidirectional converters in stand-alone dc microgrids," in *2012 IEEE 51st IEEE Conference on Decision and Control (CDC)*, pp. 3068–3073. IEEE, 2012.

[15] Y. Zhao, W. Qiao, and D. Ha, "A sliding-mode duty-ratio controller for dc/dc buck converters with constant power loads," *IEEE transactions on industry applications*, vol. 50, no. 2, pp. 1448–1458, 2014.

[16] J. Zeng, Z. Zhang, and W. Qiao, "An interconnection and damping assignment passivity-based controller for a dc–dc boost converter with a constant power load," *IEEE Transactions on Industry Applications*, vol. 50, no. 4, pp. 2314–2322, 2014.

[17] J. Zhou and C. Wen, *Adaptive backstepping control of uncertain systems: Nonsmooth nonlinearities, interactions or time-variations*. Springer, 2008.

[18] S. M. Ashabani and Y. A.-R. I. Mohamed, "A flexible control strategy for grid-connected and islanded microgrids with enhanced stability using nonlinear microgrid stabilizer," *IEEE Transactions on Smart Grid*, vol. 3, no. 3, pp. 1291–1301, 2012.

[19] T.-S. Lee and M.-L. Chen, "Applied nonlinear control with adaptive backstepping technique for a three-phase ac/dc boost converter," in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*, pp. 567–571. IEEE, 2008.

[20] H. El Fadil and F. Giri, "Backstepping based control of pwm dc-dc boost power converters," in *2007 IEEE International Symposium on Industrial Electronics*, pp. 395–400. IEEE, 2007.

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[21] W.-H. Chen, J. Yang, L. Guo, and S. Li, "Disturbance-observer-based control and related methods-an overview," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 2, pp. 1083–1095, 2016.

[22] C. Zhang, J. Wang, S. Li, B. Wu, and C. Qian, "Robust control for pwm-based dc–dc buck power converters with uncertainty via sampled-data output feedback," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 504–515, 2015.

[23] S. Li, J. Yang, W.-H. Chen, and X. Chen, *Disturbance observer-based control: methods and applications*. CRC press, 2014.

[24] H. SIRA-RAMIREZ and M. Ilic-Spong, "Exact linearization in switched-mode dc-to-dc power converters," *International journal of control*, vol. 50, no. 2, pp. 511–524, 1989.

[25] S. Bacha, I. Munteanu, A. I. Bratcu *et al.*, "Power electronic converters modeling and control," *Advanced Textbooks in Control and Signal Processing.-London: Springer*, vol. 454, 2014.

[26] H. K. Khalil and J. Grizzle, *Nonlinear systems*, vol. 3. Prentice hall New Jersey, 1996.

[27] C. Qian and W. Lin, "A continuous feedback approach to global strong stabilization of nonlinear systems," *IEEE Transactions on Automatic Control*, vol. 46, no. 7, pp. 1061–1079, 2001.

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