



Article

# A Novel Concept of Electron–Hole Enhancement for Superjunction Reverse-Conducting Insulated Gate Bipolar Transistor with Electron-Blocking Layer

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**Abstract:** A novel snapback-free superjunction reverse-conducting insulated gate bipolar transistor (SJ-RC-IGBT) is proposed and verified by simulation. In the SJ-RC-IGBT, the parasitic P/N/P/N structure as thyristor or Shockley diode demonstrates large conductivity due to an overabundance of carriers for reverse conduction. By preventing electrons from leaking across the N+ region at the collector side, the extra electron-blocking (EB) layer introduced in the SJ-RC-IGBT can dramatically enhance electron–hole pairs in the N/P-pillars. Hence, the SJ-RC-IGBT demonstrates a low on-state voltage ( $V_{on}$ ). In addition, snapback-free characteristics and a large safe operating area (SOA) are also achieved in the SJ-RC-IGBT. During the turn-off process, a significant amount of electrons are extracted by parasitic MOS across the EB layer at the collector side to decrease the turn-off loss ( $E_{off}$ ). According to the optimized results, the SJ-RC-IGBT with EB layer obtains an ultralow  $E_{off}$  of  $3.9 \text{ mJ/cm}^2$  at  $V_{on} = 1.38 \text{ V}$  with 88% and 81% decreases, respectively, compared with the conventional reverse-conducting IGBT (CRC-IGBT) and superjunction IGBT (SJ-IGBT).

**Keywords:** reverse-conducting IGBT; snapback-free; thyristor; electron-blocking; superjunction IGBT; SOA; superjunction



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## 1. Introduction

The reverse-conducting insulated gate bipolar transistor (RC-IGBT) is a crucial component for packing in a single power module at a low package cost, and it plays vital roles in medium and high voltage inverters [1,2]. The RC-IGBT works in a forward and reverse state, necessitating [3–6]: (i) reverse conduction with a uniform current distribution; (ii) forward conduction with the lowest possible on-state voltage ( $V_{on}$ ) and without a snapback effect at the high carrier injection for conductive modulation; (iii) high-speed switching for the lowest possible turn-off power dissipation by accelerating carrier extraction. It is well known that the conventional RC-IGBT (CRC-IGBT) is achieved by anti-parallel to a freewheeling diode (FWD) as an anode-short IGBT for reverse conduction. However, the CRC-IGBT easily results in a snapback phenomenon and a relatively high  $V_{on}$  at forward conduction and non-uniform current distribution at reverse conduction [3], which are, however, in conflict with the design requirements. The reverse-conducting capability and the snapback-free are desirable pursuits of the RC-IGBT design [7]. Although the snapback-free can be achieved by these techniques, such as a floating p-region in the trench collector [8] and discontinuous field-stop (FS) layer [9], these RC-IGBTs are at the expense of  $V_{on}$  and the forward conducting uniformity compared with conventional IGBTs. Therefore, in the RC-IGBT, an anti-parallel thyristor [10] or a Shockley diode [11] are introduced other than a FWD in the CRC-IGBT to realize both reverse conduction and suppress the snapback effect, which easily causes reverse snapback [7]. Moreover, the issue of current crowding is another challenge for obtaining a large safe operating area (SOA) in these RC-IGBTs. To eliminate the current-crowding problem, the edge-termination concept [12]

is proposed and evaluated in the RC-IGBT to reduce injected holes into edge termination and avoid the recovery in the diode mode in lieu of the IGBT mode during the turn-off process. The current crowding is partially smoothed by the termination region, but the snapback effect is inevitable in the active region. To ensure snapback-free, a controllable collector trench gate RC-IGBT, which is controlled by an additional gate-driving signal [13], and an automatically controlled anode gate IGBT [14] are proposed, whereas the circuitry complexity or on-state resistance is also increased.

Further, the RC-IGBT needs to not only eliminate the snapback phenomenon but also account for the trade-off between  $V_{on}$  and turn-off loss ( $E_{off}$ ). To optimize this trade-off, the superjunction seems a good candidate for minimizing the  $E_{off}$  by unipolar and bipolar mode at a high or low doping concentration of the superjunction drift region [15]. The superjunction IGBT (SJ-IGBT) as an effective method to accelerate carrier extraction from the drift region for depletion has been proven to reduce  $E_{off}$  by simulations in [16], experiments in [17], and models in [18]. To the best of our knowledge, the suppression of the snapback effect in the RC-IGBT employing the superjunction is firstly realized by the anode-shortened structure at the sacrifice of  $V_{on}$  [19]. For reducing  $V_{on}$ , a shorted-collector trench and carrier-storage (CS) layer introduced in the superjunction IGBT [20] can enhance carriers-injection for decreasing  $V_{on}$  and  $E_{off}$  but without a reverse-conducting capability. In addition, the “anode-side” superjunction IGBT helps effectively extract carriers and has potential for the RC-IGBT analogous to a MOS-controlled thyristor with a reduced snapback [21].

When compared to a standard RC-IGBT [19,21], a superjunction trench clustered insulated gate bipolar transistor (SJ-TCIGBT) with no reverse-conduction capability can simultaneously reduce  $V_{on}$  and  $E_{off}$ . In this study, we also introduced a superjunction structure for RC-IGBTs [20]. In addition, the backside thinning method, which is added to traditional IGBTs as a thin n-base and a low-doped field-stop layer, can significantly minimize  $E_{off}$  [22]. In contrast to this feature, RC-IGBTs have a backside N+ doping area that reduces turn-off loss at the expense of substantial forward static losses. Therefore, a superjunction structure for RC-IGBTs includes a “double-side carrier storage layer” concept to improve conductance modulation in the drift zone and further reduce the  $V_{on}$  compared with the RC-IGBTs in [19–21].

In this paper, the state-of-the-art superjunction reverse-conducting IGBT (SJ-RC-IGBT) for superior  $V_{on}$ - $E_{off}$  trade-off is proposed and verified by simulation. A feature is that an additional trench collector is inserted into the N/P-pillars for separating the N+ and P+ collector regions. In the reverse conduction, the parasitic P/N/P/N thyristor in the SJ-RC-IGBT is triggered on for a large conductivity to latch up other parasitic BJTs. Both of the N/P-pillars can offer a conduction path to uniform the space charges distribution. In the forward conduction, the  $V_{on}$  is reduced by a large amount of excess hole injected from P+ collector region into the N-pillar and its carrier-storage effect is enhanced by the CS layer. In addition, the electron-blocking (EB) layer can also enhance the carrier-storage effect, which restricts the electrons in the N/P-pillars leaking via the bypath of this trench collector into the N+ collector region for achieving a low  $V_{on}$ . Highlighting that the carrier-storage effect is weakened by anode-shortened N+ region in the collector is correspondingly compensated by the EB layer to eliminate the snapback effect. Nevertheless, the inherent large account of excess carriers can be extracted rapidly during the turn-off process.  $E_{off}$  is dramatically reduced by this extraction path generated by the N+ collector region, EB layer, and trench collector.

In Section 2, the forward- and reverse-conducting mechanisms of the SJ-RC-IGBT are investigated and revealed. In Section 3, the optimized results are discussed for the SJ-RC-IGBT performance. At the forward breakdown voltage of 1540 V, a small  $V_{on}$  of 1.27 V is obtained much lower than that of the CRC-IGBT at  $E_{off} = 3.65 \text{ mJ/cm}^2$ .

## 2. Device Structure and Conduction Mechanism

### 2.1. Device Structure Profile

Figure 1a–c show the schematic views of the SJ-RC-IGBT, SJ-IGBT and CRC-IGBT, respectively. The dimensions are shown in the figure. If it has no special specification, the key doping concentrations are  $N_{\text{pillar}} = 3 \times 10^{15} \text{ cm}^{-3}$ -doping concentration of the N/P-pillars,  $N_{\text{CS}} = 1 \times 10^{16} \text{ cm}^{-3}$ -doping concentration of the CS layer, and  $N_{\text{FS}} = 2 \times 10^{16} \text{ cm}^{-3}$ -doping concentration of the FS layer. In the SJ-RC-IGBT, the doping concentration of the EB layer ( $N_{\text{EB}}$ ) is  $2 \times 10^{16} \text{ cm}^{-3}$ . In the CRC-IGBT, the doping concentration of N-drift ( $N_{\text{d}}$ ) is  $1 \times 10^{13} \text{ cm}^{-3}$ . Two-dimensional simulator MEDICI have been carried out, and the physical models—CONMOB (carrier mobility model dependence on doping concentration), FLDMOB (carrier mobility model dependence on high electric field), SRFMOB2 (enhanced surface mobility model), CONSRH (Shockley–Read–Hall recombination model), AUGER (Auger recombination model), BGN (Slotboom bandgap narrowing model), and IMPACT.I (impact ionization model)—are included [22]. The simulation is verified with data and calibrated [23]. The carrier lifetime ( $\tau$ ) is set at  $1 \mu\text{s}$  [24].

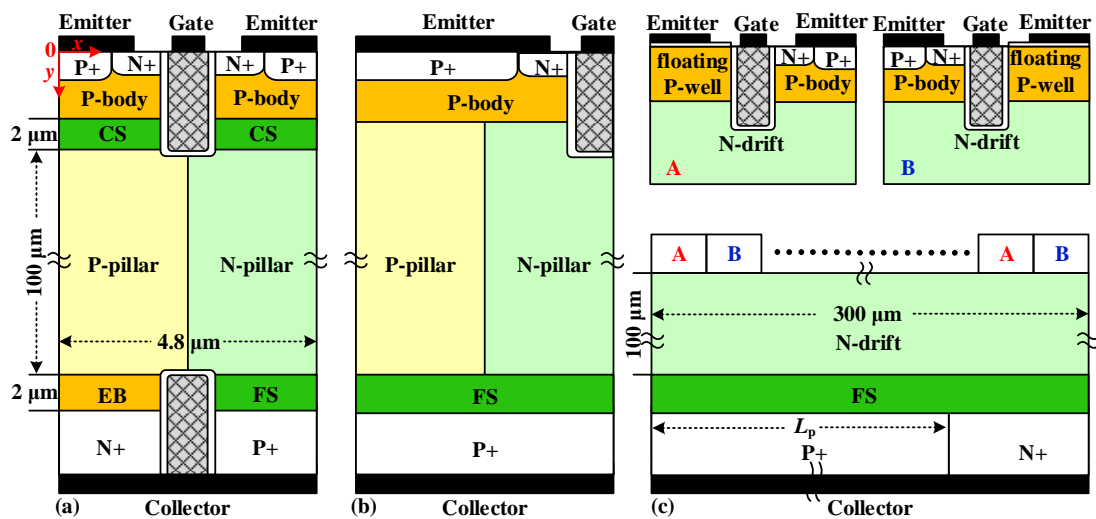
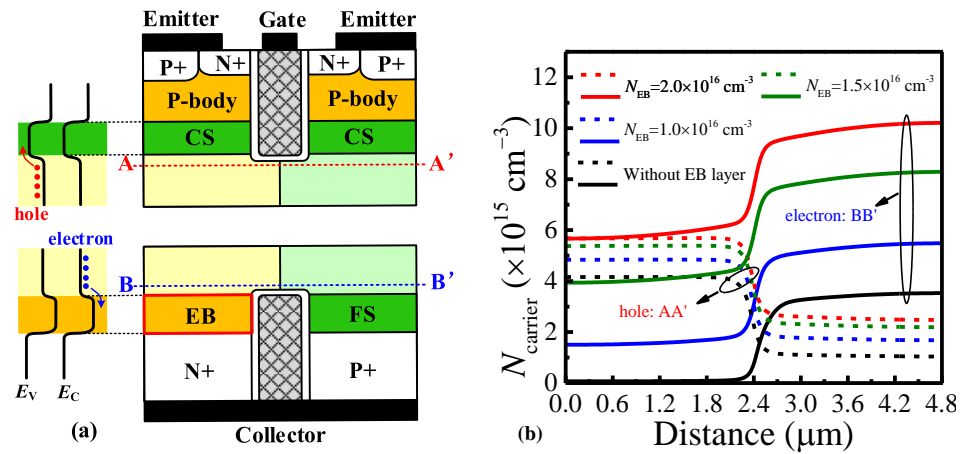


Figure 1. Schematic cross-sections of (a) SJ-RC-IGBT, (b) SJ-IGBT, and (c) CRC-IGBT. The cell-unit width of SJ-RC-IGBT and SJ-IGBT is  $4.8 \mu\text{m}$  and of CRC-IGBT is  $300 \mu\text{m}$ .

Compared with the SJ-IGBT and CRC-IGBT, the main feature is that an EB layer at the bottom of the P-pillar and an additional trench collector inserted into the N-pillar and P-pillar to separate the N+/P+ collector regions are implanted in the SJ-RC-IGBT. At the emitter side, the injected holes in the N/P-pillars are blocked by the CS layer, and at the collector side, the injected electrons are blocked by the EB layer. Therefore, electron-hole pairs in the N/P-pillars are further improved by the CS layer and EB layer higher than the SJ-RC-IGBT without the EB layer. In the SJ-RC-IGBT, the EB layer and CS layer help the reduction of  $V_{\text{on}}$ . During the turn-off process, the trench collector can speed up extraction of the excess carriers from the N/P-pillars for a low  $E_{\text{off}}$ . Otherwise, if the CS layer is introduced in the SJ-IGBT, the optimization of the  $V_{\text{on}}-E_{\text{off}}$  trade-off is also achieved but without the reverse-conducting capability, as given in [22].

In order to illustrate the carrier-storage effect of the EB layer and CS layer, Figure 2a shows the schematic energy-band views and carrier distributions at  $V_{\text{G}} = 15 \text{ V}$  and  $V_{\text{CE}} = 1 \text{ V}$ . The doping concentration of the EB layer increasing from  $1.0 \times 10^{16} \text{ cm}^{-3}$  to  $2.0 \times 10^{16} \text{ cm}^{-3}$  can enhance the electron concentration along line BB' from  $\sim 1.5 \times 10^{15} \text{ cm}^{-3}$  to  $\sim 5.8 \times 10^{15} \text{ cm}^{-3}$  in the P-pillar and from  $\sim 5.5 \times 10^{15} \text{ cm}^{-3}$  to  $\sim 9.8 \times 10^{15} \text{ cm}^{-3}$  in the N-pillar, as shown in Figure 2b. The structure without the EB layer means that the corresponding region is filled by the P-pillar. It is obviously found that the EB layer as electron barrier can

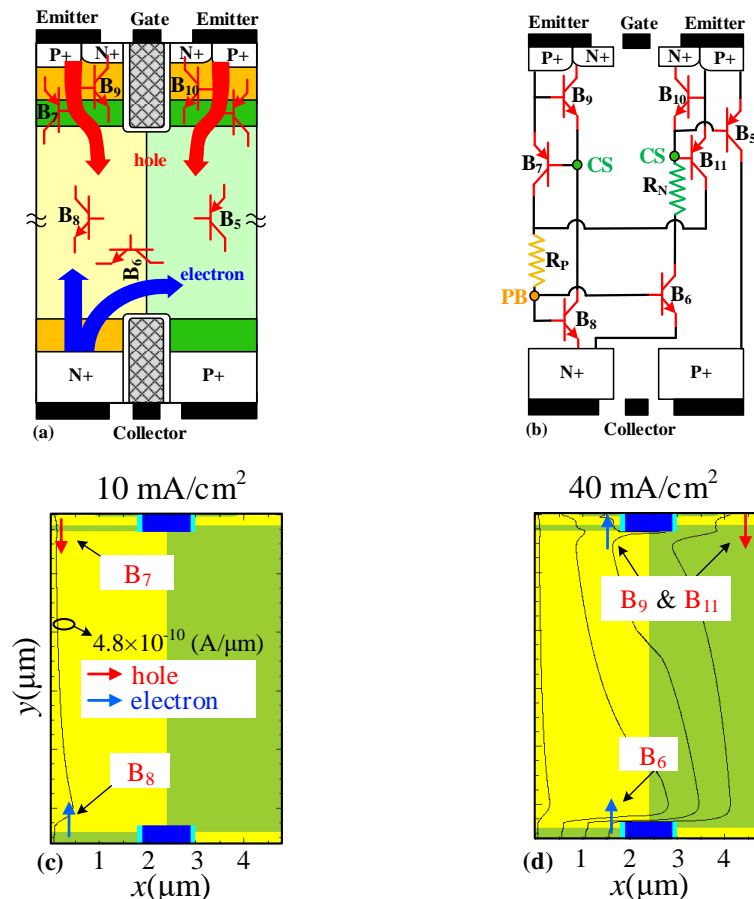
enhance the carrier-storage effect in the N/P-pillars, but in the absence of the EB layer, the hole-storage effect by the CS layer is weakened.



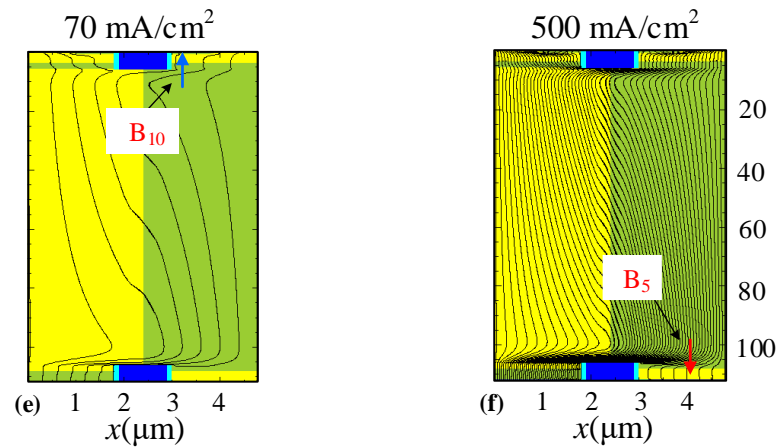
**Figure 2.** The effect of  $N_{EB}$  on carrier distribution. (a) Diagram of carrier-storage effect along cut lines position. (b) The influence of  $N_{EB}$  on hole concentration in the vicinity of CS layer and electron concentration in the vicinity of EB layer at the condition of  $V_G = 15 \text{ V}$  and  $V_{CE} = 1 \text{ V}$ .

2.2. Reverse- and Forward-Conducting Mechanism

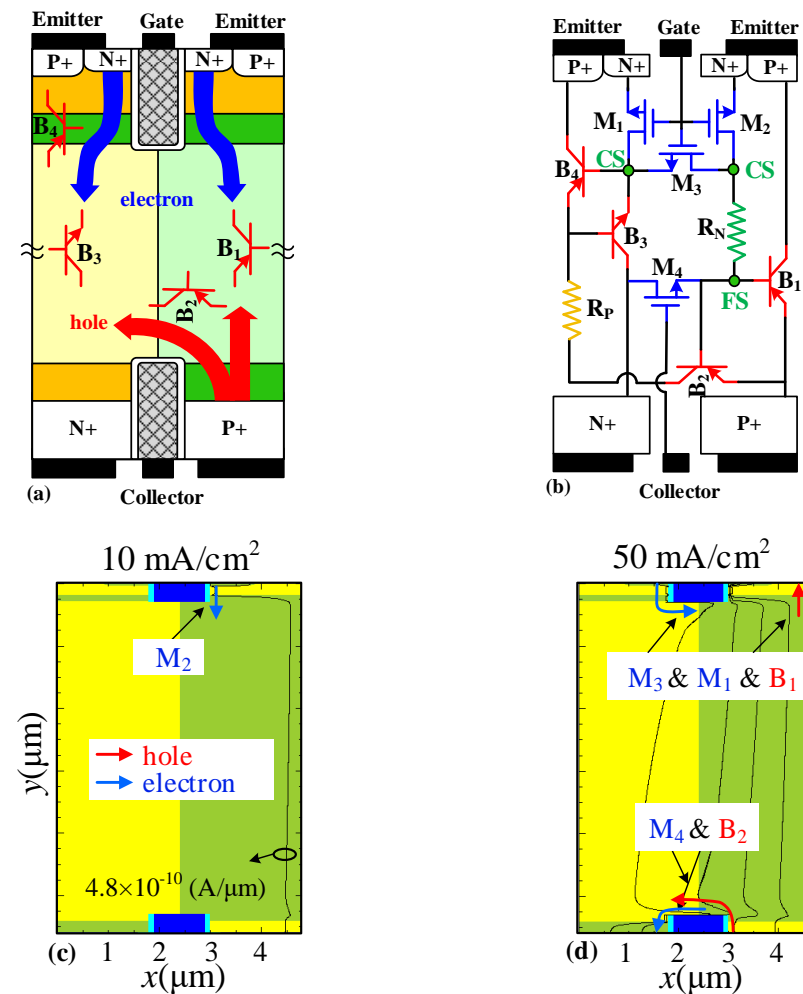
Figures 3 and 4 show the reverse/forward-conducting mechanisms of the SJ-RC-IGBT, the corresponding equivalent circuits, and the current distributions under different conduction current density. The parasitic Bipolar Junction Transistors (BJTs) are marked in Figures 3a and 4a.



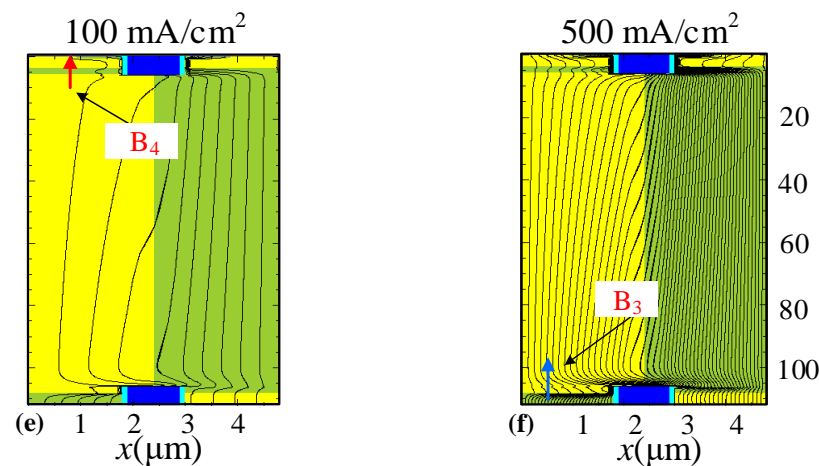
**Figure 3.** Cont.



**Figure 3.** The reverse conduction and equivalent circuit of SJ-RC-IGBT. (a) Reverse-conducting mechanism. (b) Equivalent circuit at reverse conduction. Reverse-conducting current distribution of SJ-RC-IGBT at (c) 10 mA/cm<sup>2</sup>, (d) 40 mA/cm<sup>2</sup>, (e) 70 mA/cm<sup>2</sup>, and (f) 500 mA/cm<sup>2</sup>. The bias condition of reverse conduction is that the collector and gate are grounded, and the emitter is positively biased. All the contours of current density are  $4.8 \times 10^{-10}$  A/ $\mu$ m. Blue arrows represent electron injection and red arrows represent hole injection.



**Figure 4.** Cont.



**Figure 4.** The forward conduction and equivalent circuit of SJ-RC-IGBT. (a) Forward-conducting mechanism. (b) Equivalent circuit at forward conduction. Forward-conducting current distribution of SJ-RC-IGBT at (c) 10 mA/cm<sup>2</sup>, (d) 50 mA/cm<sup>2</sup>, (e) 100 mA/cm<sup>2</sup>, and (f) 500 mA/cm<sup>2</sup>. The bias condition of forward conduction is that the gate and collector are positively biased, and the emitter is grounded. All the contours of current density are  $4.8 \times 10^{-10}$  A/ $\mu$ m. Blue arrows represent electron injection and red arrows represent hole injection.

At reverse conduction, holes are injected from the P+ region at the emitter side into the N/P-pillars and electrons are injected from the N+ region at the collector side, as shown in Figure 3a. In the beginning, BJTs B<sub>7</sub> and B<sub>8</sub> are turned on as the first thyristor, then BJTs B<sub>6</sub> and B<sub>11</sub> are turned on as the second thyristor. With an increase of the reverse current, the voltage drop across the junction of the P-body/CS layer is larger than  $\sim 0.7$  V, with BJTs B<sub>9</sub> and B<sub>10</sub> triggered on. At last, BJT B<sub>5</sub> is turned on by the effective base current at a positive biased emitter. The equivalent circuit of the SJ-RC-IGBT at reverse conduction is illustrated in Figure 3b.

Figure 3c–f show the distributions of current at reverse conduction. At 10 mA/cm<sup>2</sup>, holes are injected from the emitter region and electrons are injected from the collector region of the SJ-RC-IGBT as two serial P/N junctions. Because of the narrow CS layer, BJTs B<sub>7</sub> and B<sub>8</sub> work as a thyristor with a low voltage drop. With an increase of reverse bias of the emitter, the conduction current is increased from 40 mA/cm<sup>2</sup> to 70 mA/cm<sup>2</sup> for BJTs B<sub>6</sub>, B<sub>9</sub>, B<sub>10</sub>, and B<sub>11</sub> on and from 70 mA/cm<sup>2</sup> to 500 mA/cm<sup>2</sup> for BJT B<sub>5</sub> on. Eventually, at a high reverse current condition, the N/P-pillars become high conductivity regions.

At forward conduction, the parasitic MOSFETs (M<sub>1</sub>, M<sub>2</sub>, and M<sub>3</sub>) around the gate are firstly turned on. Electrons from the N+ emitter region and holes from the P+ collector region are injected into the N/P-pillars, as shown in Figure 4a. The forward equivalent circuit is illustrated in Figure 4b. The injected electrons into the N-pillar trigger on BJTs B<sub>1</sub> and B<sub>2</sub>. With the forward current increasing, the junction of the P-pillar/CS layer will be forward biased sufficiently large enough to inject minority carriers from the P-pillar to the CS layer, and then BJT B<sub>4</sub> is triggered on. Since the base region of BJT B<sub>4</sub> is formed by a narrow CS layer with a relatively high doping concentration, BJT B<sub>4</sub> works as a low gain BJT. As forward conduction increases, the junction of the P-pillar/CS layer is further positively biased. The parasitic BJT B<sub>3</sub> is turned on. There is a weak conduction channel for electrons in M<sub>4</sub> (parasitic MOSFET around the trench collector) to offer a path for electron extraction when the SJ-RC-IGBT is turned off.

Figure 4c–f show the distributions of current at forward conduction. At low forward conduction (10 mA/cm<sup>2</sup>), electrons injected from MOSFET M<sub>2</sub> as unipolar current is intended for the base of BJT B<sub>1</sub>. Up to 50 mA/cm<sup>2</sup>, holes injected from the P+ collector region and electrons injected from MOSFETs M<sub>3</sub> and M<sub>1</sub> can activate BJTs B<sub>1</sub> and B<sub>2</sub>. When the conduction current increases to 100 mA/cm<sup>2</sup>, BJT B<sub>4</sub> works at on-state. At last, the N+ collector region potential is high enough for triggering BJT B<sub>3</sub> on at 500 mA/cm<sup>2</sup>. There

are two conduction channels with a low barrier for electrons from MOSFET  $M_1$  to MOSFET  $M_4$  around the trench collector.

### 3. Results and Discussion

#### 3.1. Conduction Characteristics

Figure 5 shows the forward/reverse I-V curves of the SJ-RC-IGBT, SJ-IGBT, and CRC-IGBT. From Figure 5a, it is obviously found that the SJ-IGBT and SJ-RC-IGBT turn on with snapback-free, but the CRC-IGBT has a snapback phenomenon at  $L_p = 170 \mu\text{m}$  and  $200 \mu\text{m}$ . Due to the inhibition of unipolar conduction provided by the  $N^+$  collector area, the snapback effect in the CRC-IGBT can be fully removed when  $L_p$  increases to  $270 \mu\text{m}$ . As shown in the inset of Figure 5a, the forward conduction exceeds that of the SJ-IGBT after  $I_{CE}$  of the SJ-RC-IGBT exceeds  $33.1 \text{ A/cm}^2$ . The minimum voltage drop ( $1.24 \text{ V}$ ) at  $I_{CE} = 100 \text{ A/cm}^2$  is also obtained in the SJ-RC-IGBT. Figure 5b shows the reverse I-V curves of the SJ-RC-IGBT and CRC-IGBT. Although the reverse voltage drop of the CRC-IGBT can be decreased with the reduction of  $L_p$ , this is a contradiction as an elimination of the snapback phenomenon. However, the SJ-RC-IGBT demonstrates superior performance: a small reverse voltage drop and a uniform distribution of current. The thyristor is prone to snapback during the conduction process due to the positive feedback of the P/N/P/N structure needing some conditions, with the main factor being  $\tau$ . The positive feedback cannot be formed if the  $\tau$  is too small, as the thyristor will withstand voltage until the minority carriers can pass through the base region, then the snapback will occur. In [11], the RC-IGBT with Shockley diode (SH-RC-IGBT) has a snapback-free at a reverse voltage drop of  $0.95 \text{ V}$ . Further lowering the reverse voltage drop in SH-RC-IGBT makes it challenging to activate the parasitic thyristor without snapback. Hence, the RC-IGBT with Shockley diode (SH-RC-IGBT) has a snapback phenomenon even though it has the bigger  $\tau$  with lower reverse voltage drop, as shown is Figure 5c, but it is snapback-free for the SJ-RC-IGBT. This is due to the electron being injected into the N-pillar through the boundary of the trench collector.

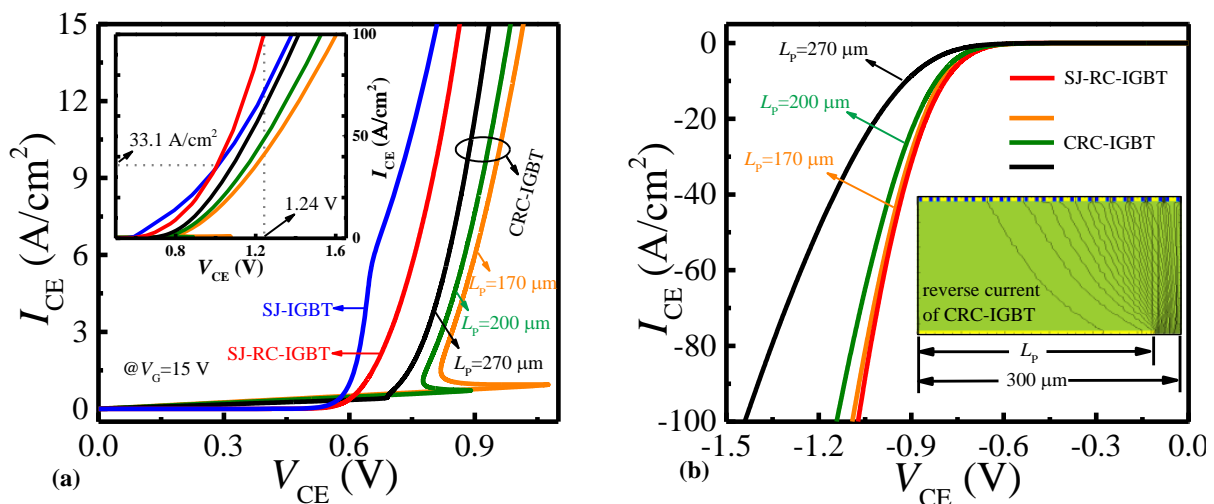
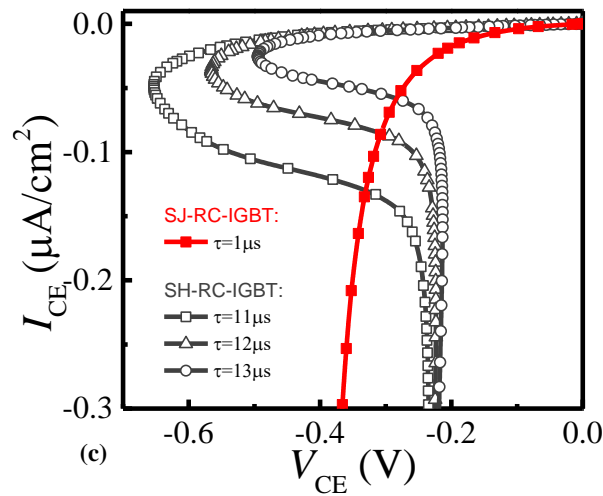


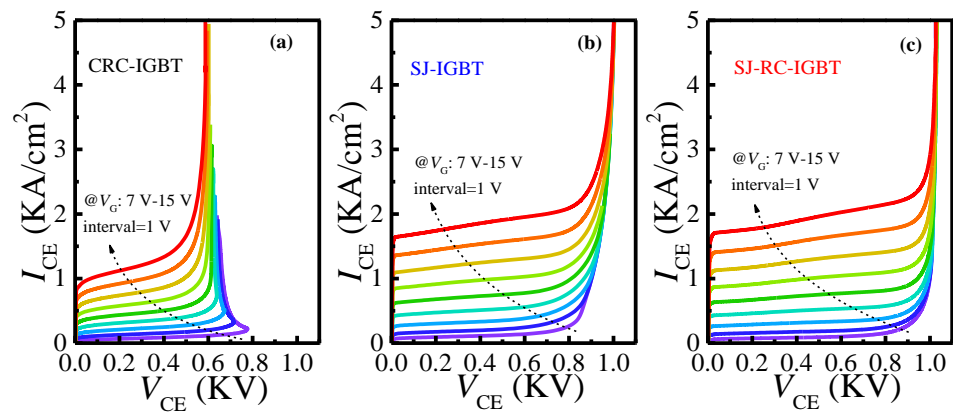
Figure 5. Cont.



**Figure 5.** (a) Forward conduction of  $I_{CE}$  versus  $V_{CE}$  and (b) reverse conduction of  $I_{CE}$  versus  $V_{CE}$ . In CRC-IGBT,  $L_p$  (the length of P+ collector region) is changed at forward and reverse conduction. (c) Reverse snapback curves. FP-RC-IGBT is referenced from [8].

### 3.2. Safe Operating Area

Conventionally, the instability of the IGBT is prone to trigger on parasitic BJTs, giving rise to a non-uniform current distribution at quasi-saturation conduction and high voltage bias. As shown in Figure 6a, the I-V curves of the CRC-IGBT snapback below 800 V much lower than that of the SJ-IGBT, as shown in Figure 6b, and the SJ-RC-IGBT, as shown in Figure 6c. This is mainly because the non-uniform current regenerates high space charge modulation in the absence of a uniform electric field. In the SJ-IGBT and SJ-RC-IGBT, the N/P-pillars can offer a uniform conduction path without crowding space charges and avoiding immature breakdown. Although the saturation current density of the SJ-RC-IGBT is higher than the CRC-IGBT, the SOA of the SJ-RC-IGBT is continuously improved, due to uniform current regions sustained by the N/P-pillars.



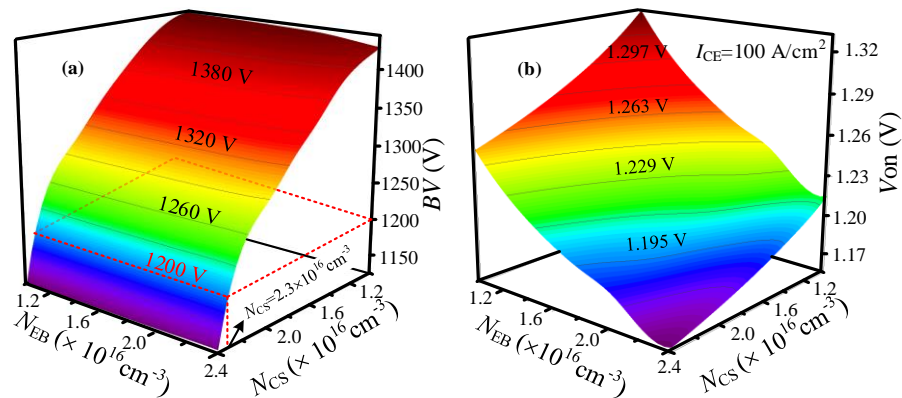
**Figure 6.** I-V characteristics of three IGBTs with a ramp-up  $V_G$  from 7 V to 15 V (The lines from blue-purple to red indicate increase in  $V_G$  from 1 V to 5 V with 1 V interval.): (a) I-V characteristics of CRC-IGBT, (b) I-V characteristics of SJ-IGBT, and (c) I-V characteristics of SJ-RC-IGBT.

### 3.3. BV and $V_{on}$ Optimization

Figure 7a shows the breakdown voltage (BV) versus  $N_{EB}$  and  $N_{CS}$ . In the range of  $N_{EB} = 1.2 \times 10^{16} \text{ cm}^{-3}$ – $2.4 \times 10^{16} \text{ cm}^{-3}$ , BV has a small variation at a certain  $N_{CS}$ . Figure 7b shows  $V_{on}$  versus  $N_{EB}$  and  $N_{CS}$ . During forward conduction,  $V_{on}$  is influenced by the ambipolar effect. The increase of  $N_{CS}$  leads to a high hole potential barrier near the P-body to restrict hole extraction. Meanwhile, the increase of  $N_{EB}$  results in raising the electron



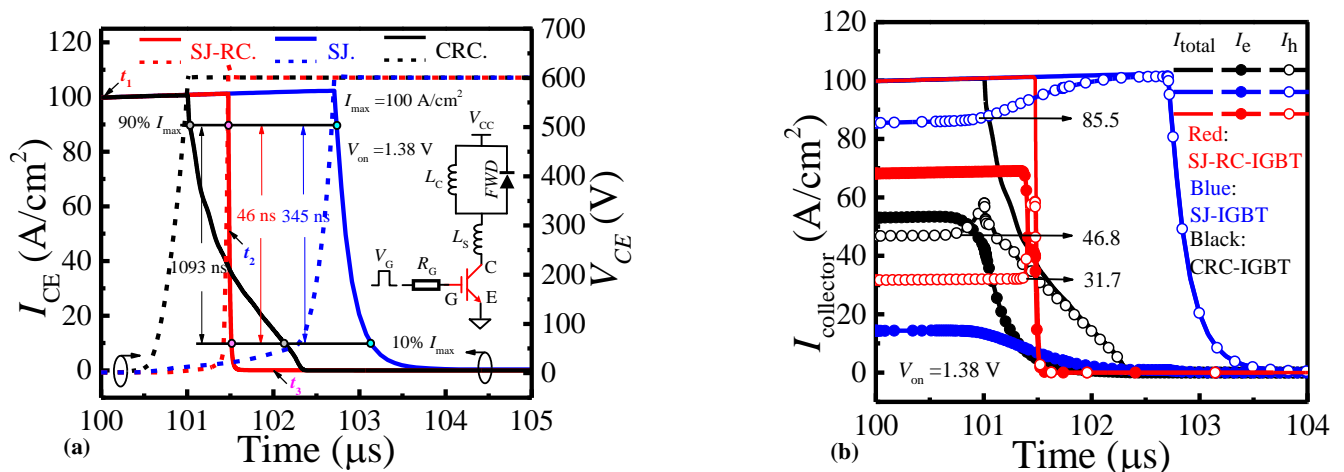
potential barrier to enhance hole injection in the N-pillar for achieving high conductive modulation. Hence, both an  $N_{CS}$  and  $N_{EB}$  increase can reduce  $V_{on}$ .



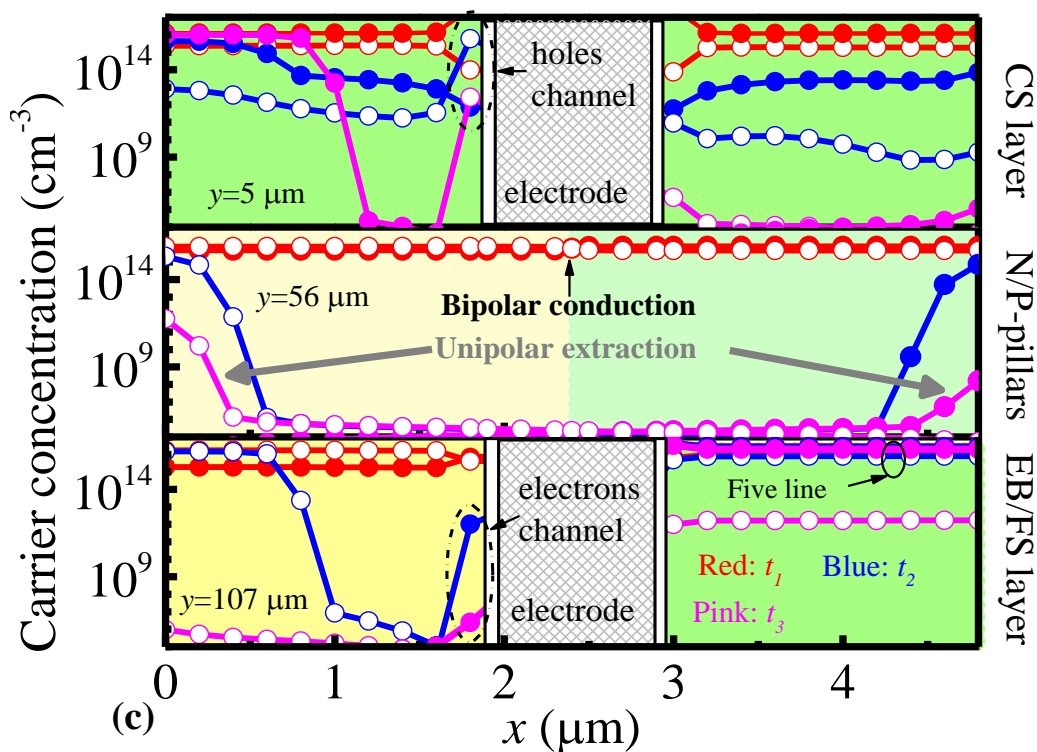
**Figure 7.** BV and  $V_{on}$  dependence on doping concentration in SJ-RC-IGBT. (a) Effect of  $N_{CS}$  and  $N_{EB}$  on BV. (b) Effect of  $N_{CS}$  and  $N_{EB}$  on  $V_{on}$ .

### 3.4. Turn-Off Characteristics

Figure 8a shows the turn-off process of the SJ-RC-IGBT, SJ-IGBT, and CRC-IGBT. In the SJ-RC-IGBT,  $I_{CE}$  falling from 90 A/cm<sup>2</sup> to 10 A/cm<sup>2</sup> needs 46 ns by a huge reduction of 95.8% compared with the CRC-IGBT and 86.7% compared with the SJ-IGBT. The high performance of the turn-off process is generally attributed to two aspects—(i) low injection of excess carriers, as shown in Figure 8b, and (ii) extracting channels, as implied in Figure 8c. (i) In the SJ-RC-IGBT, the injection of holes is at a low level, but the conductive modulation is at high level in contrast with the SJ-IGBT and CRC-IGBT. (ii) At  $t_1$ , a high density of electron–hole pairs exists at all of the CS layer, N/P-pillars, and EB layer. Although from  $t_2$  to  $t_3$ , the electron and hole in the main regions of the CS layer, N/P-pillars, and EB layer are remarkably reduced, a relatively high hole density remains along the left side of the gate in the CS layer and electron channel along the trench collector in the EB layer.



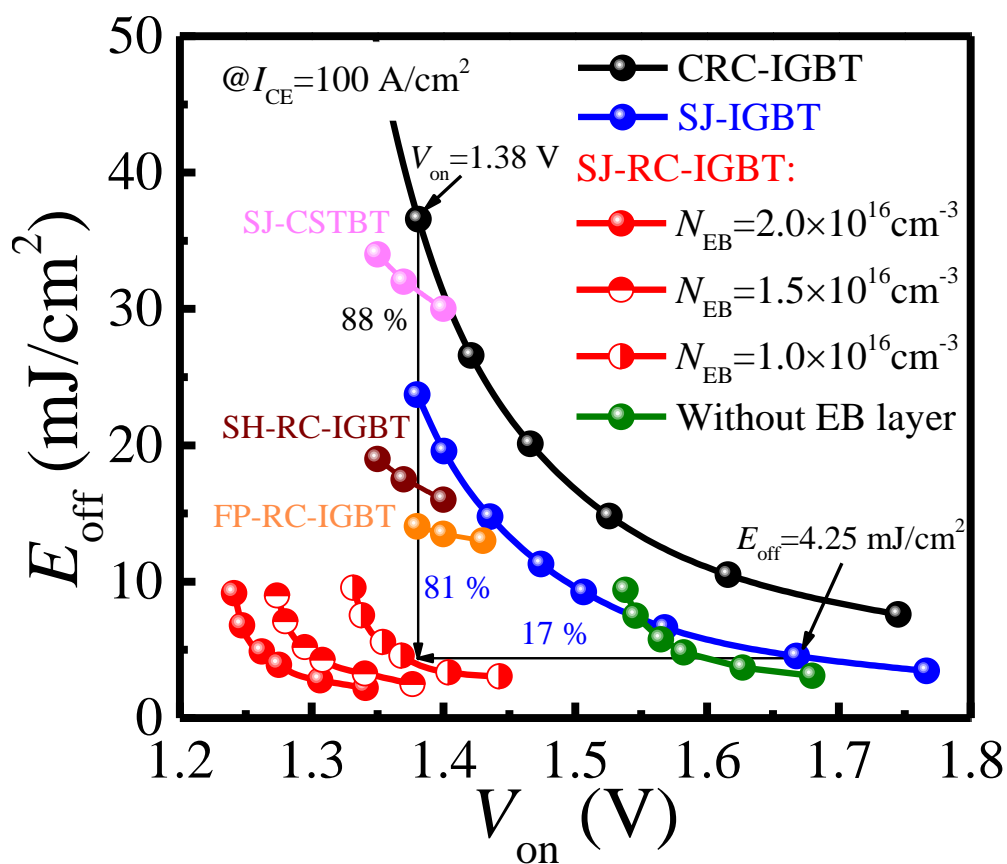
**Figure 8.** Cont.



**Figure 8.** (a) Turn-off waveforms of SJ-RC-IGBT, SJ-IGBT, and CRC-IGBT. The inset shows the simulation circuit with  $R_G = 10 \Omega$  and  $L_s = 5 \text{ nH}$ . (b) Electron current ( $I_e$ ), hole current ( $I_h$ ), and total current ( $I_{\text{total}}$ ) at the collector of SJ-RC-IGBT, SJ-IGBT, and CRC-IGBT during turn-off. (c) Electron/hole concentrations in CS layer, N/P-pillars, and EB/FS layer of SJ-RC-IGBT. Hollow and solid represent hole and electron, respectively.

### 3.5. Trade-Off between Forward Conduction and Turn-Off Loss

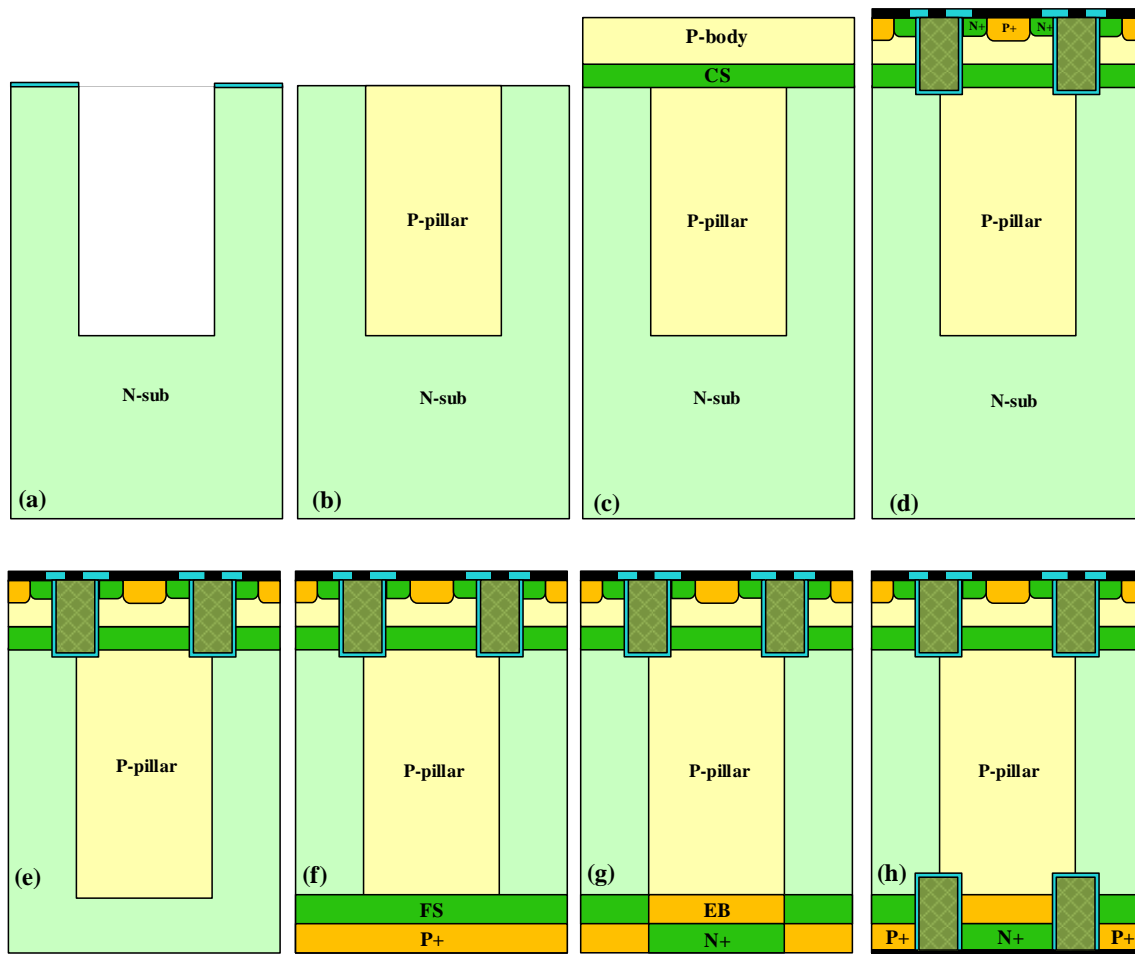
Figure 9 shows the trade-off between  $E_{\text{off}}$  and  $V_{\text{on}}$  at  $I_{\text{CE}} = 100 \text{ A/cm}^2$ . With an increase of  $N_{\text{EB}}$  from  $1.0 \times 10^{16} \text{ cm}^{-3}$  to  $2.0 \times 10^{16} \text{ cm}^{-3}$ ,  $V_{\text{on}}$  of the SJ-RC-IGBT is reduced from 1.38 V to 1.27 V at  $E_{\text{off}} = 4.25 \text{ mJ/cm}^2$ , as shown in Figure 9. It can be seen that the SJ-RC-IGBT with EB layer ( $N_{\text{EB}} = 1.0 \times 10^{16} \text{ cm}^{-3}$ ) has  $V_{\text{on}}$  of 1.38 V at  $E_{\text{off}} = 4.25 \text{ mJ/cm}^2$ , which is 17% lower than the SJ-IGBT, as shown in Figure 9. It is worth emphasizing that the EB layer in the SJ-RC-IGBT can enhance the conductivity in the N/P-pillars for gaining a lower  $V_{\text{on}}$  due to restricting electrons leaking via the P-pillar into the N+ collector region, as the effect of the CS layer for blocking holes. Nevertheless, if the SJ-RC-IGBT is without the EB layer, a high speed of turn-off switching is easy to obtain in the SJ-RC-IGBT from green dots, as shown in Figure 9, but it inevitably results in improving  $V_{\text{on}}$ . In brief, the SJ-RC-IGBT with EB layer exhibits superior  $E_{\text{off}}\text{-}V_{\text{on}}$  trade-off over the FP-RC-IGBT [8], SJ-CSTBT [22], SH-RC-IGBT [11], SJ-IGBT, and CRC-IGBT.



**Figure 9.**  $E_{off}$ - $V_{on}$  relationship of SJ-RC-IGBT, SJ-IGBT, and CRC-IGBT.  $E_{off}$ - $V_{on}$  relationship at  $I_{CE} = 100 \text{ A/cm}^2$ . FP-RC-IGBT is referenced from [8]. SH-RC-IGBT is referenced from [11]. SJ-CSTBT is referenced from [22].

#### 4. Key Fabrication Process of the SJ-RC-IGBT

Figure 10 shows the key fabrication process of the SJ-RC-IGBT. First, a deep trench is formed by reactive ion etching, and the deep trench can achieve a fairly large aspect ratio, as shown in Figure 10a. Figure 10b shows the trench refilling by anisotropic epitaxial growth; after epitaxy, the flat surface is achieved by chemical mechanical polishing. The surface defects were then repaired by sacrificing oxidation. The final surface is shown in Figure 10b. Before forming the MOS part, the CS layer and P-body are formed by epitaxial growth, as shown in Figure 10c. The rest of the facade is formed by standard trench gate process, with the final configuration of the emitter region and trench gate shown in Figure 10d. The backside process is essential in the design of the RC-IGBT. First, through the back thinning to achieve the required width of the drift region, as shown in Figure 10e, then the FS layer, P+ collector, EB layer, and N+ collector are formed by backside implantation, as shown in Figure 10f,g. Last, the trench collector and electrode process on the back is similar to that on the front. Through the above process flow, the SJ-RC-IGBT finally forms the structure shown in Figure 10h.



**Figure 10.** The key fabrication process steps of the SJ-RC-IGBT. (a) Deep trench etching based on reactive ion etching, (b) trench refilling by anisotropic epitaxial growth, (c) epitaxial growth of CS layer and P-body, (d) forming trench MOS structure and electrode, (e) back thinning, (f) forming FS layer and P+ collector by backside implantation, (g) forming EB layer and N+ collector by backside implantation, and (h) forming backside trench and electrode.

## 5. Conclusions

A SJ-RC-IGBT with EB layer is proposed and investigated for revealing its complex conduction mechanism at the forward and reverse conditions. This innovative mechanism aids optimizing the trade-off between  $E_{off}$  and  $V_{on}$ . In comparison with the CRC-IGBT, the SJ-IGBT and SJ-RC-IGBT without EB layer and  $E_{off}$  and  $V_{on}$  in SJ-RC-IGBT with EB layer demonstrate superior advantages. Moreover, the N/P-pillars to deliver a uniform distribution of space charges without compromising the SOA at high forward conduction has considerably increased the SOA of the SJ-RC-IGBT.

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## References

1. Ozpineci, B.; Chinthavali, M.S.; Tolbert, L.M.; Kashyap, A.S.; Mantooth, H.A. A 55-kW three-phase inverter with Si IGBTs and SiC schottky diodes. *IEEE Trans. Ind. Appl.* **2009**, *45*, 278–285. [[CrossRef](#)]
2. Napoli, E.; Spirito, P.; Strollo, A.G.M.; Frisina, F.; Fragapane, L.; Fagone, D. Design of IGBT with integral freewheeling diode. *IEEE Electron. Device Lett.* **2002**, *23*, 532–534. [[CrossRef](#)]
3. Takahashi, H.; Yamamoto, A.; Aono, S.; Minato, T. 1200V reverse conducting IGBT. In Proceedings of the International Symposium on Power Semiconductor Devices ICs (ISPSD), Tokyo, Japan, 24–27 May 2004.
4. Jiang, M.X.; Shen, Z.J. Simulation study of an injection enhanced insulated-gate bipolar transistor with p-base schottky contact. *IEEE Trans. Electron. Devices* **2016**, *63*, 1991–1995. [[CrossRef](#)]
5. Huang, M.M.; Gao, B.; Yang, Z.M.; Lai, L.; Gong, M. A carrier-storage-enhanced superjunction IGBT with ultralow loss and on-state voltage. *Electron. Device Lett.* **2018**, *39*, 264–267. [[CrossRef](#)]
6. Duan, B.X.; Sun, L.C.; Yang, Y.T. Analysis of the novel snapback-free LIGBT with fast-switching and improved latch-up immunity by TCAD simulation. *IEEE Trans. Electron. Devices* **2019**, *40*, 63–66. [[CrossRef](#)]
7. Findlay, E.M.; Udrea, F. Reverse-conducting insulated gate bipolar transistor: A review of current technologies. *IEEE Trans. Electron. Devices* **2019**, *66*, 219–231. [[CrossRef](#)]
8. Jiang, H.P.; Zhang, B.; Chen, W.J.; Li, Z.J.; Liu, C.; Rao, Z.G.; Dong, B. A snapback suppressed reverse-conducting IGBT with a floating p-region in trench collector. *IEEE Electron. Device Lett.* **2012**, *33*, 417–419. [[CrossRef](#)]
9. Deng, G.Q.; Luo, X.R.; Wei, J.; Zhou, K.; Huang, L.H.; Sun, T.; Liu, Q.; Zhang, B. A snapback-free reverse conducting insulated-gate bipolar transistor with discontinuous field-stop layer. *IEEE Trans. Electron. Devices* **2018**, *65*, 1856–1861. [[CrossRef](#)]
10. Hsu, W.C.W.; Udrea, F.; Hsu, H.Y.; Lin, W.C. Reverse-conducting insulated gate bipolar transistor with an anti-parallel thyristor. In Proceedings of the International Symposium on Power Semiconductor Devices ICs (ISPSD), Hiroshima, Japan, 6–10 June 2010.
11. Zhu, L.H.; Chen, X.B. A novel snapback-free reverse conducting IGBT with anti-parallel shockley diode. In Proceedings of the International Symposium on Power Semiconductor Devices ICs (ISPSD), Kanazawa, Japan, 26–30 May 2013.
12. Zhang, W.L.; Zhu, Y.J.; Lu, S.J.; Tian, X.L.; Teng, Y. Increase of the reliability of the junction terminations of reverse-conducting insulated gate bipolar transistor by appropriate backside layout design. *IEEE Electron. Device Lett.* **2014**, *35*, 1281–1283. [[CrossRef](#)]
13. Wei, J.; Luo, X.R.; Huang, L.H.; Zhang, B. Simulation study of a novel snapback-free and low turn-off loss reverse-conducting IGBT with controllable trench gate. *IEEE Electron. Device Lett.* **2018**, *39*, 252–255. [[CrossRef](#)]
14. Zhu, L.H.; Chen, X.B. An investigation of a novel snapback-free reverse-conducting IGBT and with dual gates. *IEEE Trans. Electron. Devices* **2012**, *59*, 3048–3053. [[CrossRef](#)]
15. Antoniou, M.; Udrea, F.; Bauer, F. The superjunction insulated gate bipolar transistor optimization and modeling. *IEEE Trans. Electron. Devices* **2010**, *57*, 594–600. [[CrossRef](#)]
16. Oh, K.H.; Lee, J.; Lee, K.H.; Kim, Y.C.; Yun, C. A simulation study on novel field stop IGBTs using superjunction. *IEEE Trans. Electron. Devices* **2006**, *53*, 884–890.
17. Oh, K.H.; Kim, J.; Seo, H.; Jung, J.; Kim, E.; Kim, S.S.; Yun, C. Experimental investigation of 650V superjunction IGBTs. In Proceedings of the International Symposium on Power Semiconductor Devices ICs (ISPSD), Žofín Palace, Czech Republic, 12–16 July 2013.
18. Wang, Z.G.; Zhang, H.; Kuo, J.B. Turn-OFF Transient Analysis of Superjunction IGBT. *IEEE Trans. Electron. Devices* **2019**, *66*, 991–998. [[CrossRef](#)]
19. Antoniou, M.; Udrea, F.; Bauer, F.; Nistor, I. A new way to alleviate the RC IGBT snapback phenomenon: The superjunction solution. In Proceedings of the International Symposium on Power Semiconductor Devices ICs (ISPSD), Hiroshima, Japan, 6–10 June 2010.
20. Zhou, K.; Luo, X.R.; Huang, L.H.; Liu, Q.; Sun, T.; Li, Z.J.; Zhang, B. An ultralow loss superjunction reverse blocking insulated-gate bipolar transistor with shorted-collector trench. *IEEE Electron. Device Lett.* **2016**, *37*, 1462–1465. [[CrossRef](#)]
21. Antoniou, M.; Lophitis, N.; Udrea, F.; Bauer, F.; Vemulapati, U.R.; Badstuebner, U. On the investigation of the “Anode Side” superjunction IGBT design concept. *IEEE Electron. Device Lett.* **2017**, *38*, 1063–1066. [[CrossRef](#)]
22. Li, Z.G.; Jiang, F.X.C.; Li, B.H.; Lin, X.N. A new way to break through the limitation of cs-layer doping on the breakdown voltage of CSTBT: The superjunction solution. In Proceedings of the IEEE International Conference of IEEE Region 10, Xi’an, China, 22–25 October 2013.
23. Luther-King, N.; Narayanan, E.M.S.; Coulbeck, L.; Crane, A.; Dudley, R. Comparison of Trench Gate IGBT and CIGBT Devices for Increasing the Power Density From High Power Modules. *IEEE Trans. Power Electron.* **2010**, *25*, 583–591. [[CrossRef](#)]
24. *Medici User Guide, Version D-2010.03*; Synopsys Inc.: Mountain View, CA, USA, 2010.

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