IEEE Open Journal of
Power Electronics

Received 25 February 2021; accepted 30 March 2021. Date of publication 1 April 2021;
date of current version 13 May 2021. The review of this paper was arranged by Editor F. Wang.

Digital Object Identifier 10.1109/OJPEL.2021.3070527

A Novel Current-Source-Based Gate Driver With Active Voltage Balancing Control for Series-Connected GaN HEMTs

ZHENGDA ZHANG [1] (Student Member, IEEE), CHUNHUI LIU [1] (Student Member, IEEE), MENGZHI WANG [1], YUNPENG SI [1] (Student Member, IEEE), YIFU LIU [1], AND QIN LEI [1,2] (Member, IEEE)

[1] School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ 85283 USA
[2] School of Electrical, Computer and Energy Engineering, Arizona State University, Chandler, AZ 85248 USA

CORRESPONDING AUTHOR: ZHENGDA ZHANG (e-mail: zzhan235@asu.edu)

This work was supported by the U.S. National Science Foundation under Award 1847693.

ABSTRACT The voltage rating of the commercial Gallium Nitride (GaN) power devices are limited to 600/650 V due to the lateral structure. Stacking the low-voltage rating devices is a straightforward approach to block higher dc link voltage. However, the unbalanced voltage sharing can occur due to the discrepancies in the gate driving loops, the device parameter tolerance and the device-to-ground displacement currents for the series-connected devices in the stack. The voltage imbalance may cause the over-voltage breakdown, in particular for GaN devices, which do not have the avalanche breakdown mechanism. In this article, a novel controllable current source gate driver is proposed, which addresses the voltage imbalance issue of series-connected GaN HEMTs for both hard switching and soft switching scenarios. The proposed current source gate driver controls the device switching timing and the dv/dt with fine accuracy by directly regulating the device gate current. Without the employment of the lossy snubber circuit or the external Miller capacitor, the switching energy and the switching speed are almost not compromised for each individual device. Meanwhile, the current mirror circuits are utilized as the discontinuous pulsed current sources, which produce negligible additional gate driving loss. A series-connected GaN-based multiple pulse tester is built to validate the proposed current source gate driver and the voltage balancing strategies. It is demonstrated that the drain-to-source voltage difference of the series-connected GaN devices is below 10% for different load current and different switching speed (dv/dt) conditions. Moreover, it is found that the series-connected GaN solution can save 33.6% switching energy compared with the benchmark SiC solution under the same operating condition.

INDEX TERMS Gallium nitride, HEMTs, stacking, current control, driver circuits, parasitic capacitance, switching loss.

I. INTRODUCTION

Medium voltage (MV) dc is considered an enabling and promising technique in future power distribution grid, microgrids, shipboard power system, offshore wind farms, high-power drive systems and electric vehicle (EV) charging stations [1]–[5]. In MV dc systems, Silicon Carbide (SiC) devices are gradually replacing Si-IGBTs due to the much reduced switching energy and the high operating temperature capabilities. However, the reverse recovery loss of the intrinsic body diode of the SiC devices is still inevitable. Though external SiC Schottky diode can be paralleled with the SiC MOSFETs to cut down the reverse recovery loss, the costs will be increased.

Gallium Nitride (GaN) power devices offer low specific on-state resistance, fast switching speed and high operating temperature capabilities compared with Silicon (Si) counterpart. All of these are beneficial for the efficiency, power density, specific power, as well as the reliability of power electronics converters [6]. Though Silicon Carbide (SiC) excels in high-temperature applications, the material characteristics of GaN

TABLE 1. Critical Parameters of a 1.2 kV/30 a SiC MOSFET and Two Series-Connected 600 V/30 a GaN HEMTs

Parameters	Single 1.2 kV SiC MOSFET	Two series-connected 600 V GaN HEMTs
Part number	CREE C3M0075120J	Infineon IGOT60R070D1
Typical on-resistance (R_{dson})	75 mΩ	55 mΩ × 2
Output capacitance (C_{oss})	58 pF	72 pF ÷ 2
Reverse recovery charge (Q_{rr})	109 nC	0
Gate charge (Q_g)	48 nC	5.8 nC × 2

are superior in high-efficiency, high-frequency converters [7]. In particular, due to the absence of the intrinsic body diode in the structure, the reverse recovery loss in GaN devices are totally eliminated. Therefore, GaN devices will produce less switching energy. Meanwhile, GaN devices have much smaller input capacitance compared with SiC devices, so the gate driving loss can be reduced as well.

However, not like the SiC devices, which have the availability of 1.7 kV rating device on the market and 15 kV rating device in the research stage [8], [9]. The highest voltage rating of the commercial GaN HEMTs is only at 600/650 V level because of the lateral structure. The vertical GaN devices are considered to have higher voltage rating [10], but they have not yet been produced on a commercial level. The insufficient voltage rating of GaN HEMTs hinders their appliance in the MV dc systems.

Stacking converters and stacking switches are the two most common approaches to block higher dc link voltage. The cascaded H-bridges and multilevel converters can be categorized as the stacking converter solution. The advantages of this solution include lower dv/dt, lower EMI and lower output harmonics [11]. However, the complexity of the hardware structure as well as the control scheme are greatly increased for this solution. Stacking switches is much simpler in terms of both the hardware structure and the control scheme. The two series-connected 600/650 V GaN HEMTs can compete with the 1.2 kV SiC MOSFET and the three series-connected 600/650 V GaN HEMTs can compete with the 1.7 kV SiC MOSFET. The critical parameters of a 1.2 kV SiC MOSFET and two series-connected 600 V GaN HEMTs with similar current rating are listed in Table 1. Though the equivalent R_{dson} of series-connected GaN is higher than the R_{dson} of a single SiC MOSFET, the reverse recovery charge is completely eradicated for the series-connected GaN solution. The output capacitance and the gate charge are reduced significantly for the series-connected GaN solution as well. The deficiency of higher equivalent R_{dson} for the series-connected GaN solution can be compensated by increasing the die size or paralleling the devices. Meanwhile, for the general hard switching MV applications, the switching loss is typically more dominant [9]. The series-connected GaN solution can improve the system efficiency compared with the SiC solution [5]. Moreover, cost reduction of GaN devices will progress faster than for SiC devices due to significant lower substrate costs and Si-CMOS manufacturing line compatibility [12].

The biggest challenge for the series-connected device approach is to address the dynamic voltage sharing issue among the switches in the stack, which can cause the over-voltage breakdown for the individual low-voltage switch. It is more challenging for the series-connected GaN solution, because of the extremely fast switching speed and the highly nonlinear Miller capacitance. Meanwhile, GaN devices are more vulnerable to the over-voltage damage due to the lack of avalanche breakdown mechanism [7]. The drain-to-source voltage imbalance among the series-connected switches can be introduced by the following factors. First, the gate driving loop can have discrepancies for the switches in the stack. The gate driving signals can be unsynchronized due to the variance of the propagation delays in the path. The gate driving loop parasitics can be different as well if the circuit connection and layout are not the same for different channels. Second, the device parameter tolerance can cause the unbalanced dynamic voltage sharing. The device input capacitance, output capacitance and the threshold voltage are all within certain range after the manufacturing process. The dynamic voltage sharing can be affected by the tolerance of these parameters. Last but not least, the displacement current flowing through the device-to-ground parasitic capacitances will cause distinctions in the gate current as well as in the drain current for different switches in the stack. The distinctions in the gate or drain current will naturally result in unbalanced voltage sharing for different switches, even if the gate driving loops and device parameters are perfectly matched. The last factor is considered to be the major cause for the unbalanced voltage sharing for the series-connected fast-switching switches [13]–[15]. In particular, the GaN devices have very small input and output capacitances, so the device-to-ground parasitic capacitances will have a stronger effect on the dynamic voltage sharing for the series-connected GaN devices.

Some researchers have been working on the topic of series-connected GaN devices. In [16], a 1.2 kV super-cascode GaN transistor is demonstrated, which is based on two series-connected depletion-mode GaN. The structure has the same drawbacks as the typical cascode GaN, such as the undesired voltage sharing between the low-voltage Si MOSFET and the high-voltage depletion-mode GaN during the switching transient and large parasitic inductance in the package due to the multiple dies [17]. Meanwhile, an extra balancing capacitor is needed to assist the dynamic voltage sharing, which introduces additional loss. In [12], a 1.2 kV GaN transistor is made up by the series connection of an enhancement-mode GaN transistor and a depletion-mode GaN transistor. A charge-pump-based gate driver circuit is used to properly drive the top device. However, the device parameter mismatch can be severe for the two different type of GaN devices and no discussion is made on the dynamic voltage sharing for the two devices. An integrated gate driver circuit is proposed in [5], [18] to solve the issue of voltage imbalance for series-connected

enhancement-mode GaN devices and a detailed mathematical model is developed as well. However, for this open-looped method, the circuit parameters need to be carefully tuned to achieve the desired switching timing for the series-connected devices, which makes this method very sensitive to the variance in the operating conditions, such as load current, dc link voltage and temperature. To sum, a practical strategy for addressing the voltage imbalance issues in series-connected GaN devices is lacked in the existing literatures.

However, a lot of efforts have been conducted for the voltage balancing of the series-connected IGBT in the past [19]–[25]. In recent years, a lot of researchers began to focus on the voltage balancing of series-connected SiC MOSFETs as well [13], [14], [26]–[28]. Most of the voltage balancing strategies can be grouped as the drain-side approach and the gate-side approach [13]. The snubber-based strategies belong to the drain-side approach. The pure passive snubber is usually very lossy. To reduce the additional loss produced by the snubber, the active energy recovery snubber circuits are proposed in [22], [27] with the cost of increasing circuit complexity and decreasing the circuit reliability. However, the device drain-to-source voltage rising slew rate is penalized with the employment of the snubber circuit. More switching energy will be produced during the switching transients. For the gate-side approach, the coupled gate driving method utilizes a single gate driver to drive all the series-connected switches in the stack [26], [29]–[32], in which the gate driving circuit parameters including the extra voltage balancing components need to be carefully tuned to achieve desired switching timing for each individual switch. It makes this method less adaptive to variable operating conditions. Hence, this method is not suitable for mass production. The active gate driving control is another main-stream strategy on the gate-side. In [14], [33], the gate driving signals are actively controlled to attain the desired switching timing for the series-connected switches. The unit step in the controller needs to be very small (below 1 ns) to achieve the satisfying voltage balancing, which makes the accuracy of this approach not reliable. In [13], a current mirror is in series with a large extra Miller capacitor to serve as a controllable extra Miller capacitor. The drain-to-source dv/dt of each device can be regulated to achieve well-balanced voltage sharing. However, this strategy is only suitable for the devices with large input capacitance, such as high current rating power modules and Si devices, in which the turn-off dv/dt is mostly determined by the charging speed of the Miller capacitance. For the discrete wide-band-gap (WBG) devices, the input capacitance is significantly smaller. During the turn-off transient, the input capacitance can be discharged below the threshold before the drain-to-source voltage starts to rise and no Miller plateau will be observed in the gate-to-source voltage. In other words, during the dv/dt transient, the device channel is already cut off and the device can be regarded as a junction capacitor. The value of the extra Miller capacitor needs to be dominant in the output capacitance ($C_{oss} = C_{gd} + C_{ds}$) in order to regulate the dv/dt properly. For discrete GaN devices, the intrinsic Miller capacitance is extremely small and it is significantly smaller than its drain-to-source capacitance (C_{ds}). The large extra Miller capacitor will greatly slow down the dv/dt of the switch and more switching energy will be produced during the switching transient. Meanwhile, the large extra Miller capacitor will enhance the crosstalk between the power loop and the gate driving loop. The gate driving loop will be more sensitive to the dv/dt and ringings in the power loop.

In this study, a controllable current-source-based gate driver is proposed. The gate current is directly controlled, so the device switching timing and dv/dt can be regulated with fine accuracy. Regardless of the origin of the voltage imbalance, the drain-to-source voltages of the switches in the stack can always be roughly equalized for both soft switching and hard switching scenarios. Meanwhile, without the employment of the lossy snubber circuits or the extra Miller capacitor, the switching energy and switching speed of the device are almost not compromised. Moreover, the current mirror circuits are utilized as the fast-responded discontinuous pulsed current sources, so the extra gate driving loss is negligible. Sufficient experiments have been conducted to validate the proposed current source gate driver and the voltage balancing strategies in a variety of operating conditions.

The rest of the article is organized as follows. Section II discusses the root cause of the unbalanced voltage sharing in different switching scenarios. The corresponding voltage balancing strategies are presented in Section III. Section IV introduces the operating principles and practical design considerations of the proposed current source gate driver. Section V demonstrates the experimental verification. Finally, Section VI concludes this article.

II. ROOT CAUSE OF THE UNBALANCED VOLTAGE SHARING IN DIFFERENT SWITCHING SCENARIOS

As mentioned in the introduction, the unbalanced voltage sharing can be caused by: (1) the discrepancies in the gate driving loops; (2) the device parameter tolerance; (3) the device-to-ground displacement currents for the series-connected devices in the stack.

For the discrepancies in the gate driving loops, it can be alleviated by using symmetrical connection and circuit layouts for the series-connected switches in the stack. For the device parameter tolerance, it can be overcome by adding small external gate-to-source/drain-to-source capacitors. For the device-to-ground displacement current, however, it is hard to be passively compensated, because the device-to-ground parasitic capacitance is typically unknown. Therefore, the active compensation mechanism should be employed. Basically, the major task in this study is to actively compensate the voltage imbalance caused by the device-to-ground displacement currents.

The effect of the device-to-ground parasitic capacitance on the dynamic voltage sharing for the series-connected devices have already been discussed in the previous studies [13], [14], [34]–[38]. It is still necessary to make a summary of the effect

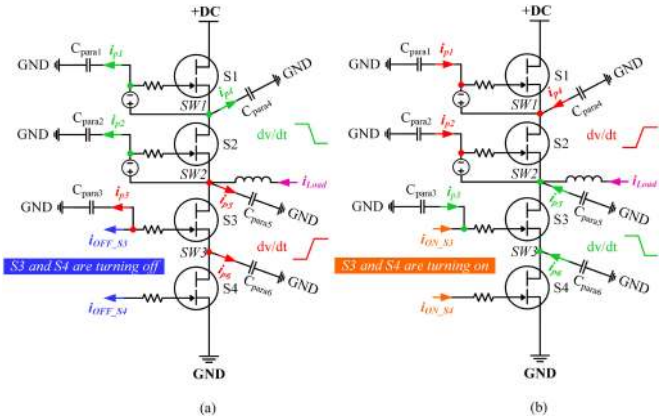

FIGURE 1. (a) Device-to-ground displacement currents during the lower arm switches 'soft' turn-off transient. (b) Device-to-ground displacement currents during the lower arm switches 'hard' turn-on transient.

in different switching scenarios, because it is the precondition of the proposed voltage balancing strategies.

A. SOFT SWITCHING SCENARIO

As is shown in Fig. 1, two GaN switches are series-connected for both upper arm and lower arm in a phase-leg. The upper arm switches (S_1 and S_2) are in the off-state and the lower arm switches (S_3 and S_4) are actively controlled. The device gate-to-ground parasitic capacitances are labeled as C_{para1}, C_{para2} and C_{para3} in the figure. Since there is almost no dv/dt between the gate and ground for S_4, very little displacement current will be produced. The parasitic capacitance between the gate and ground for S_4 is not shown in the figure. In the real system, the gate-to-ground parasitic capacitances consist of the isolation capacitance of the isolated dc-dc power supplies, the isolation capacitance for the isolated gate drivers and the device gate to heat sink parasitic capacitance (if the heat sink is grounded). The device drain-to-ground parasitic capacitances are labeled as C_{para4}, C_{para5} and C_{para6} in the figure. Similarly, since there is no dv/dt between the drain and ground for S_1, no displacement current will be produced. The parasitic capacitance between the drain and ground for S_1 is not shown in the figure as well. In the real system, the major drain-to-ground parasitic capacitance comes from the PCB interlayer capacitance for the discrete devices. For the fast-switching GaN-based power converters, the flux-cancellation PCB layout techniques are usually employed to reduce the power loop parasitic inductance. To achieve the flux-cancellation between the switching nodes and the power ground, they are normally placed in the two adjacent layers of a PCB and overlapped pretty well. If the overlapping area between the switching node and the power ground is assumed to be only 10 mm$\times$10 mm, the interlayer stray capacitance will be around 30 pF, which is already significant compared with the junction capacitance of the discrete GaN devices.

Since the device drain-to-source voltage rises during the turn-off transient and falls during the turn-on transient, the over-voltage is less likely to occur during the turn-on transient. Therefore, most of the previous studies only discussed the voltage balancing strategies during the switch turn-off transient. Strictly speaking, the previous studies only discussed the switch 'soft' turn-off transient, in which the load current will assist the charging/discharging of the device junction capacitances. As shown in Fig. 1(a), the lower arm switches S_3 and S_4 are experiencing 'soft' turn-off due to the load current direction. During the 'soft' turn-off process, S_3 will have higher gate current compared with S_4 due to the displacement current flowing through C_{para3}. Meanwhile, S_3 will have higher drain current as well compared with S_4, because of the current drawn by the drain-to-ground parasitic capacitance C_{para6}. For the 'soft' turn-off transient, the device drain-to-source dv/dt can be restricted by either the device gate current (i_{gate}) or the device drain current (i_{drain}), as illustrated in the following equation,

$$i_{\text{gate}} \geq C_{\text{gd}} \frac{dV_{\text{ds}}}{dt},$$
$$i_{\text{drain}} \geq (C_{\text{gd}} + C_{\text{ds}}) \frac{dV_{\text{ds}}}{dt}, \quad (1)$$

where C_{gd} is the device gate-to-drain capacitance (Miller capacitance) and C_{ds} is the device drain-to-source capacitance.

It is clear that when the supplied gate current from the gate driver is sufficient, the 'soft' turn-off dv/dt will be mostly determined by the drain/load current magnitude; when the supplied gate current from the gate driver is not sufficient, the 'soft' turn-off dv/dt will be limited by the supplied gate current magnitude. However, for both cases, S_3 will exhibit higher dv/dt than S_4 does if no compensation mechanism is employed. For the upper arm switches, S_2 will have higher drain current compared with S_1, because the parasitic capacitance C_{para4} will draw some current. The slew rate of the falling drain-to-source voltage for S_2 will be larger than that for S_1. The over-voltage is much less likely to happen for the upper arm switches, because the drain-to-source voltages of the two switches start to fall at the same time.

B. HARD SWITCHING SCENARIO

When the lower arm switches are turned on, as shown in Fig. 1(b), the lower arm switches S_3 and S_4 are experiencing 'hard' turn-on due to the load current direction. During the 'hard' turn-on process, S_3 will have higher gate current compared with S_4 due to the displacement current flowing through C_{para3}. The slew rate of the falling drain-to-source voltage for S_3 will be larger than that for S_4. The over-voltage is less likely to happen, as long as the turn-on timing of the series-connected switches are well matched. It should be mentioned that, if there is several nanosecond turn-on timing difference among the series-connected switches, the over-voltage can still occur [33]. For the upper arm complimentary switches S_1 and S_2, however, the over-voltage can occur due to the uneven rising drain-to-source voltages of the two switches. The upper arm switches S_1 and S_2 are actually experiencing 'hard' turn-off during this process, because the drain-to-source voltages

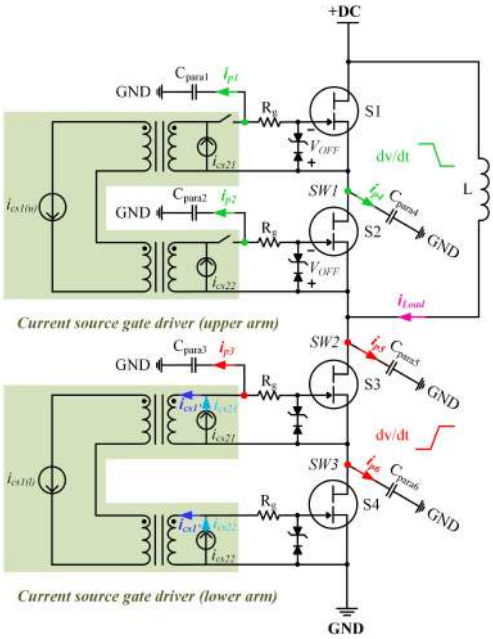

FIGURE 2. Simplified model of the proposed current source gate driver during the lower arm switches 'soft' turn-off transient.

are forced to be pulled up. Due to the displacement current from C_{para4}, S_2 will have higher dv/dt compared with S_1. If no compensation mechanism is employed, S_2 will sustain higher voltage, which can cause the over-voltage breakdown. This phenomenon is overlooked by most the previous studies. Actually, this phenomenon is very hard to solve from the gate-side by using the conventional voltage source gate driver, because the upper arm switches are already in the off-state. In this study, a controllable current-source-based gate driver is proposed. The gate current is directly controlled with fine accuracy. The above phenomenon can be solved by regulating the gate-to-source voltage of S_2 close to its threshold voltage for a very small interval in order to reduce its dv/dt and eventually achieve the balanced voltage sharing.

The detailed voltage balancing strategies for both switching scenarios will be introduced in the next section.

III. VOLTAGE BALANCING STRATEGIES FOR DIFFERENT SWITCHING SCENARIOS

A. SOFT SWITCHING SCENARIO

The simplified model of the proposed current source gate driver in a series-connected GaN-based chopper circuit during the lower arm switches 'soft' turn-off transient are shown in Fig. 2. For the soft switching scenario, the load current or the magnetizing current will assist the charging/discharging of the device junction capacitances during the turn-off transient. For the 'soft' turn-on transient, since the device drain-to-source voltage already drops to zero before the gate-to-source voltage reaches the threshold, the over-lapping switching loss is minimal. This process is also called the zero voltage switching (ZVS). To sum, for the soft switching scenario, the dv/dt happens during the device turn-off transient. Therefore, the voltage balancing strategy should be implemented during the device turn-off transient.

For the simplified model of the proposed current source gate driver, as shown in Fig. 2. A large current source (i_{cs1}) is employed on the primary side of the isolation transformer to provide the turn-on/turn-off pulse currents. Two small current sources (i_{cs21}, i_{cs22}) are implemented on the secondary side of the isolation transformer to compensate the voltage sharing difference caused by the gate/drain current variance. The purpose of employing a large current source on the primary side and two small current sources on the secondary side are explained as follows. First, this approach eliminates the potential drain-to-source voltage imbalance caused by the gate driving propagation delay. If only separate current sources are employed for each device in the stack, it is hard to guarantee the consistent propagation delay as well as the current amplitude. Meanwhile, the matrix transformer is utilized to guarantee the consistent gate loop parasitics for all the switches in the stack, because the unit transformer for each channel is exactly the same. The induced current ($i_{cs1'}$) is the major component of the supplied current from the gate driver. Second, this approach improves the resolution of the gate current regulation. If only a single current source is used to supply the transient gate current as well as the compensation current, the resolution of the gate current regulation will be reduced. During the turn-on and turn-off transients, the required supplied gate current is usually relatively high (several hundred of mA to 1∼2 A) to achieve a fast switching event and reduce the switching energy. However, the compensation gate current which is used to precisely regulate the switch turn-off timing or the dv/dt needs much smaller amplitude. The small current sources on the secondary side (i_{cs21}, i_{cs22}) are able to accomplish the gate current regulation with fine accuracy.

During the lower arm switches turn-off transient, the upper arm gate driver is disconnected and the current source output current is controlled to be zero. The Zener diodes between the gate and source of the upper arm switches S_1 and S_2 are employed to sustain the desired turn-off voltage. It should be mentioned that the current mirror circuits are utilized as the fast-responded discontinuous current sources. The current mirror circuits are actually voltage-controlled current sources, so the output current amplitude can be easily regulated. The operating principle of the current mirror circuits will be discussed in Section IV.

To explain the operating principles of the active gate current control for drain-to-source voltage balancing in the soft switching scenario, two possible cases are taken into consideration.

The first case occurs when the gate current magnitude determines the dv/dt during the turn-off transient. For this case, the supplied current from the gate driver is not sufficient and most of the supplied current is used to charge the Miller capacitance (C_{gd}) during the dv/dt transient and the Miller plateau emerges. Actually, in terms of reducing the turn-off switching energy, the supplied turn-off gate current should be

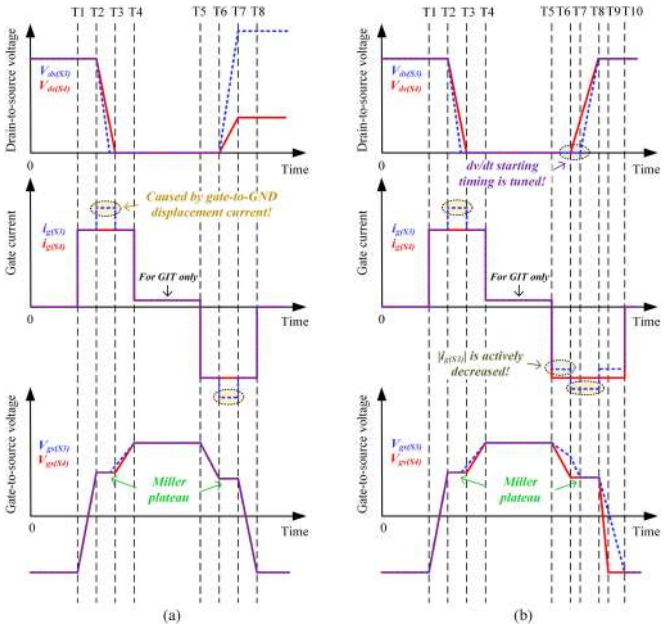

FIGURE 3. **(a) Theoretical waveforms for case 1 without active gate current control. (b) Theoretical waveforms for case 1 with active gate current control.**

large enough to cut off the device channel as soon as possible. Then the device dv/dt should be mostly determined by the load current amplitude. However, in some real applications, such as inverter-fed motor drives, the dv/dt has limit due to the concern of insulation or EMI issues [39], [40]. It is common to reduce the gate current in order to restrict the dv/dt to the limit value. Therefore, the first case will still occur in real applications even for GaN devices which have tiny Miller capacitance. To achieve this scenario, extra input capacitance ($C_{gs} + C_{gd}$) can be employed for the GaN devices to slow down the discharging of the gate during the turn-off transient.

The theoretical waveforms for case 1 without/with the active gate current control are shown in Fig. 3(a), 3(b), respectively. Without the active gate current control, the gate current for S_3 ($i_{g(S3)}$) will be larger than the gate current for S_4 ($i_{g(S4)}$) during both the turn-on and turn-off transients. As mentioned earlier, the gate current increase is due to the displacement current flowing through the device gate-to-ground parasitic capacitance. The displacement current flowing through the gate-to-ground parasitic capacitance (C_{para3}) can be expressed as,

$$i_{p3} = C_{para3}\frac{dV_{g3-to-GND}}{dt}. \tag{2}$$

For the turn-on transient, the slew rate of drain-to-source voltage for S_3 ($V_{ds(S3)}$) is faster, so it will fall to zero first. If the turn-on timing of the series-connected switches are well synchronized, the over-voltage is unlikely to occur. However, if there are several nanosecond turn-on delay among the series-connected switches, the over-voltage can still happen [33]. The proposed current source gate driver structure guarantees well-synchronized turn-on timing for the switches in the stack, so the over-voltage is not a concern during the switch turn-on transient. For the turn-off transient, the dv/dt of S_3 will be larger than that for S_4 as well due to the contribution of gate-to-ground displacement current. The over-voltage is very likely to happen if no compensation mechanism is implemented. The small current sources on the secondary side (i_{cs21}, i_{cs22}) should be kicked in during the turn-off transient. The overall gate current can be calculated as,

$$i_{g(S3)} = i_{cs1'} + i_{p3} - i_{cs21}. \tag{3}$$

As shown in Fig. 3(b), by increasing the compensation current amplitude (i_{cs21}) for S_3, the overall gate current amplitude for S_3 is actively reduced. Then the turn-off dv/dt starting timing for S_3 can be delayed. In this way, even though the dv/dt of S_3 is still larger than that of S_4, the drain-to-source voltages for the two switches can reach the steady-state value at the same time. Finally, the balanced voltage sharing is achieved by implementing the active gate current control.

The second case occurs when the drain current magnitude or the load current magnitude determines the dv/dt during the turn-off transient. For this case, the supplied current from the gate driver is sufficient to discharge the gate below the threshold during most of the time in the dv/dt transient. The excessive supplied current from the gate driver will discharge the gate-to-source capacitance very quickly. Since the channel of the device is cut off during most of the time in the dv/dt transient, the switching energy is reduced for this case. This case is common for GaN devices due to the very small gate charge.

The theoretical waveforms for case 2 without/with the active gate current control are shown in Fig. 4(a), 4(b), respectively. Again, without the active gate current control, the gate current for S_3 will be larger than the gate current for S_4 during both the turn-on and turn-off transients due to the existence of the gate-to-ground parasitic capacitance. However, the voltage imbalanced during the turn-off transient is no longer caused by the gate current difference, because the device channels are already cut off during most of the time in the turn-off dv/dt transient. Instead, the voltage imbalance is caused by the drain current difference. As shown in Fig. 2, the drain current of S_4 will be smaller than the drain current of S_3 due to the current drawn by the drain-to-ground parasitic capacitance (C_{para6}). Then the junction capacitance charging speed of the bottom switch S_4 will be slower than the top switch S_3, which results in the voltage imbalance between the two switches. Similarly, the voltage imbalance can be avoided by delaying the dv/dt starting timing of the top switch, as shown in Fig. 4(b). It is achieved by increasing the compensation current magnitude and reducing the overall gate current for the top switch.

To sum, for both cases in the soft switching scenario, the balanced voltage sharing can be obtained by tuning the starting timing of the dv/dt during the turn-off transient. The following analysis explains how to adjust the dv/dt starting timing from the gate side.

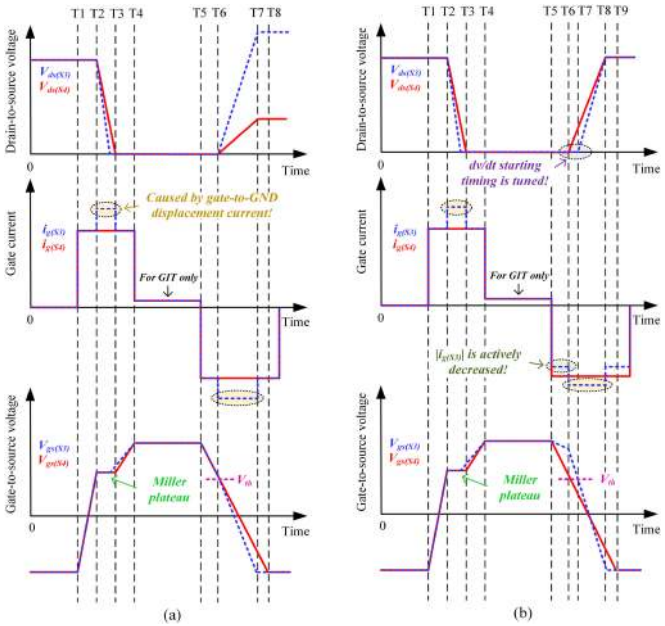

FIGURE 4. **(a) Theoretical waveforms for case 2 without active gate current control. (b) Theoretical waveforms for case 2 with active gate current control.**

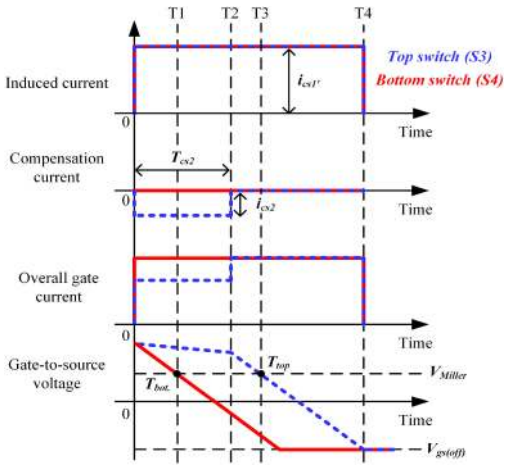

FIGURE 5. **Detailed gate current and voltage waveforms for the lower arm switches during the 'soft' turn-off transient.**

The detailed gate current and voltage waveforms during the 'soft' turn-off transient are shown in Fig. 5. Based on the semiconductor characteristics, the drain-to-source voltage starts to rise when the gate-to-source voltage reaches the Miller plateau voltage (V_{Miller}). Therefore, the moment when the device gate-to-source voltage drops to the Miller plateau voltage can be regarded as the starting timing of the drain-to-source dv/dt. It should be mentioned that the gate-to-ground displacement currents only occur during the dv/dt transient, so it will not affect the starting timing of the dv/dt. The gate-to-ground displacement currents are not reflected in Fig. 5. As discussed earlier, the top switch S_3 naturally exhibits higher dv/dt due to the existence of device-to-ground displacement currents. The secondary side current source for the top switch should be kicked in to provide the compensation current and delay the starting timing of the dv/dt for the top switch. If the device parameters are considered to be well matched, the difference of the dv/dt starting timing for the two switches can be calculated as,

$$\Delta T = T_{\text{top}} - T_{\text{bot.}} = \frac{i_{\text{cs2}} \cdot T_{\text{cs2}}}{i_{\text{cs1}'}}, \tag{4}$$

where $i_{\text{cs1}'}$ is the magnitude of the induced primary current; i_{cs2} is the magnitude of the compensation current and T_{cs2} is the pulse-width of the compensation current.

Based on (4), it is clear that the starting timing difference (ΔT) for the series-connected switches is determined by the product of the magnitude and pulse-width of the compensation current. Therefore, the two control freedoms can be utilized to obtain the desired starting timing difference. It is equivalent to directly control the gate charge of the device. It should be mentioned that the resolution of the compensation pulse-width is restricted by the controller minimum clock cycle. As mentioned earlier, the sub-nanosecond unit time step is required if the pulse-width is the only control freedom in the conventional voltage source gate driver [14], [33]. With the proposed approach, the compensation current magnitude can be set at a relatively small value. High resolution tuning can still be achieved even with larger unit time step of the compensation pulse-width. Hence, the digital control will be more reliable for the proposed approach.

To determine the compensation current magnitude and pulse-width, the following analysis is conducted. The product of the magnitude and pulse-width of the compensation current is defined as the compensation gate charge (Q_{com}). For the first case, as shown in Fig. 3, the gate-to-ground displacement current (i_{p3} in Fig. 2) actually brings more gate charge for the top switch (S_3). Therefore, the compensation gate charge should counteract the extra gate charge brought by gate-to-ground the displacement current. The following equation can be derived,

$$Q_{\text{com}} = C_{\text{para3}} \cdot \frac{V_{\text{dc}}}{2}, \tag{5}$$

where V_{dc} is the dc bus voltage and C_{para3} is the gate-to-ground parasitic capacitance of S_3.

For the second case, as shown in Fig. 4, the dv/dt is no longer determined by the gate charge, because the device channel is already cut off during the dv/dt transient. The proposed strategy is basically utilizing the dv/dt starting timing difference to compensate the slew rate difference. During the $T_6 \sim T_7$ interval in Fig. 4(b), since the gate-to-source voltage of S_3 is above the threshold, it can be regarded as an on-state resistor. The equivalent circuit during this interval is shown in Fig. 6(a). During the $T_7 \sim T_8$ interval in Fig. 4(b), the gate-to-source voltage of S_3 drops below the threshold, so it should be regarded as a junction capacitor. The equivalent circuit during this interval is shown in Fig. 6(b). Based on the equivalent

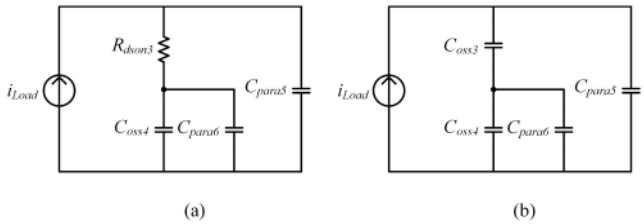

FIGURE 6. (a) Equivalent circuit for the lower arm switches during $T_6 \sim T_7$ interval (in Fig. 4(b)). (b) Equivalent circuit for the lower arm switches during $T_7 \sim T_8$ interval (in Fig. 4(b)).

circuit model, the following equation can be derived for this case,

$$Q_{\text{com}} = \frac{(C_{\text{oss4}} - C_{\text{oss3}} + C_{\text{para6}}) \cdot (C_{\text{oss4}} + C_{\text{para5}} + C_{\text{para6}})}{(C_{\text{oss4}} + C_{\text{para6}}) \cdot i_{\text{Load}}} \cdot \frac{V_{\text{dc}}}{2} \cdot i_{\text{cs1}'}. \tag{6}$$

where the definition of the parameters is consistent with the definition in Fig. 2.

It should be mentioned that (5) and (6) are derived based on the simplified circuit model. Meanwhile, the circuit parameters may change with the operating conditions, such as temperature. Therefore, it is still necessary to slightly adjust the compensation current magnitude and the pulse-width based on the actual system and operating conditions. In this study, the compensation current magnitude and pulse-width are tuned off-line based on the experimental platform and the operating conditions. The closed-loop implementation will be investigated in the future study, which will make the proposed method more adaptive to different operating conditions.

B. HARD SWITCHING SCENARIO

The simplified model of the proposed current source gate driver in a series-connected GaN-based chopper circuit during the lower arm switches 'hard' turn-on transient are shown in Fig. 7. For the hard switching scenario, the dv/dt happens during the device turn-on transient and the drain-to-source voltages of the complimentary switches in the upper arm are forced to be pulled up. Therefore, the complimentary switch S_1 and S_2 can be considered to be 'hard' turned off.

As mentioned earlier, without appropriate compensation mechanism, severe voltage imbalance is very likely to occur for S_1 and S_2 due to the existence of the drain-to-ground parasitic capacitance (C_{para4} in Fig. 7). The drain currents of S_1 and S_2 during this transient have the following relation,

$$\begin{aligned} i_{\text{drain(S2)}} &= i_{\text{drain(S1)}} + i_{\text{p4}}, \\ i_{\text{p4}} &= C_{\text{para4}} \frac{dV_{\text{SW1-to-GND}}}{dt}. \end{aligned} \tag{7}$$

If S_1 and S_2 are in the off-state during the entire lower arm switches 'hard' turn-on transient, S_2 will exhibit higher dv/dt due to the higher drain current, which can eventually lead to the over-voltage breakdown. The equivalent circuit is shown

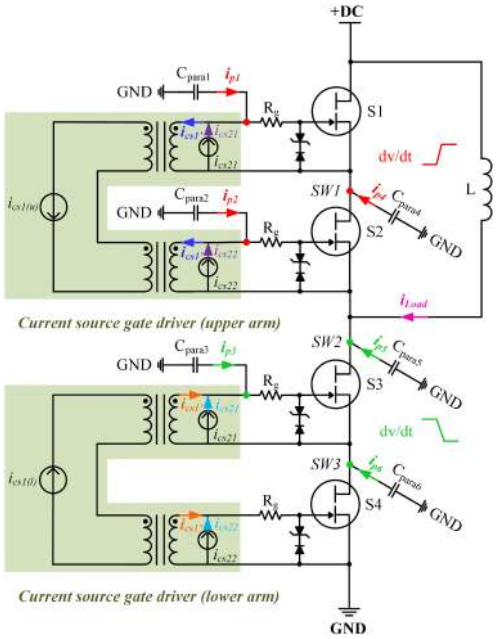

FIGURE 7. Simplified model of the proposed current source gate driver during the lower arm switches 'hard' turn-on transient.

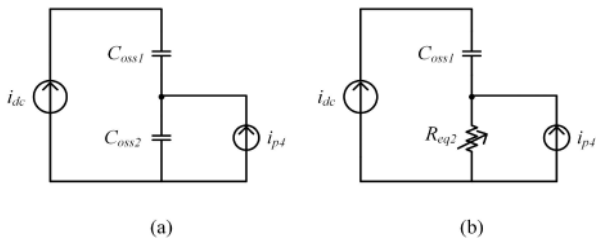

FIGURE 8. (a) Equivalent circuit for the upper arm switches during the hard switching transient without active gate current control. (b) Equivalent circuit for the upper arm switches during the hard switching transient with active gate current control.

in Fig. 8(a). The two switches can be regarded as junction capacitors because of the gate-off states. If the junction capacitances of the two switches are assumed to be close, the voltage rise for S_2 will be faster due to more charging current for its junction capacitor.

The proposed voltage balancing strategy for the hard switching scenario is explained as follows. As is shown in Fig. 9, the compensation current i_{cs2} is injected for the bottom switch S_2 before the dv/dt occurs. The gate-to-source voltage of S_2 is elevated to V_{pk}, which is close to its threshold value. Then the impedance of S_2 will be reduced. However, since the device channel just starts to conduct, the impedance of the channel is still very high compared with the normal on-state resistance (R_{dson}). For instance, the drain-to-source impedance at the threshold voltage for the Infineon 600 V/30 A e-mode GaN (IGOT60R070D1) is around 3.8 kΩ. Hence, once the gate-to-source voltage of S_2 reaches around the threshold level, the switch can be regarded as an equivalent

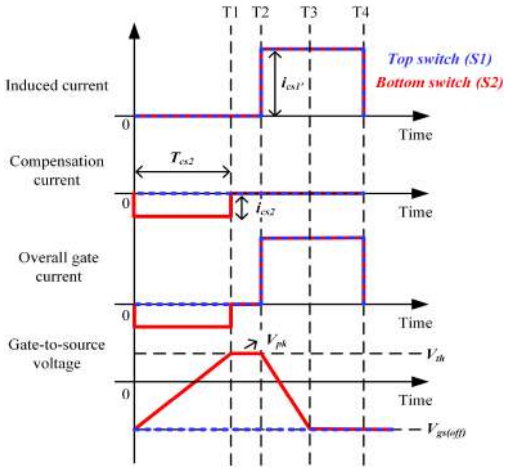

FIGURE 9. **Detailed gate current and voltage waveforms for the upper arm switches during the hard switching transient.**

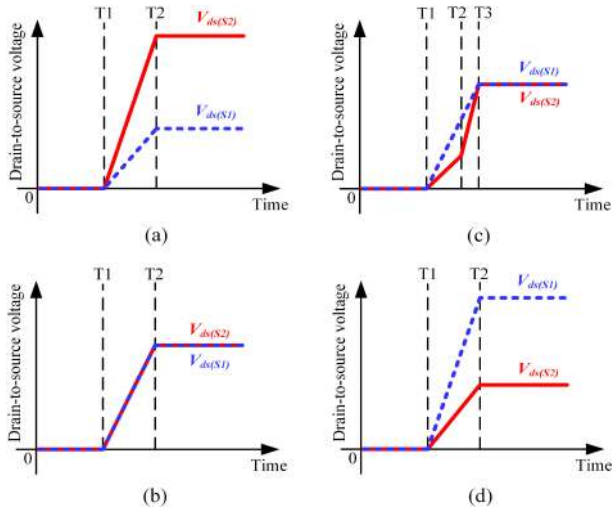

FIGURE 10. **(a) Scenario 1 (under-compensated). (b) Scenario 2 (well-compensated). (c) Scenario 3 (well-compensated). (d) Scenario 4 (over-compensated).**

large resistor, as is shown in Fig. 8(b). In this way, the dv/dt of S_2 can be reduced and the series-connected switches are able to achieve the balanced voltage sharing. Meanwhile, a large turn-off current (the induced current) should be applied to pull down the gate-to-source voltage of S_2 back to the turn-off gate voltage ($V_{\mathrm{gs(off)}}$) right after the compensation process to guarantee the safe turn-off of S_2.

For the proposed compensation method, the dv/dt of the bottom switch S_2 is proportional to its impedance, which can be determined by gate-to-source voltage. The peak gate-to-source voltage (V_{pk}) can be controlled by both the compensation current amplitude (i_{cs2}) and the pulse-width (T_{cs2}). The peak gate-to-source voltage can be obtained by,

$$V_{\mathrm{pk}} = V_{\mathrm{gs(off)}} + \frac{i_{\mathrm{cs2}} \cdot T_{\mathrm{cs2}}}{C_{\mathrm{gs}}}. \tag{8}$$

The duration of the peak voltage is determined by the starting timing of the large turn-off current, which is labeled as T_2 in Fig. 9. With the employment of the proposed compensation method, four different scenarios can occur in terms of the drain-to-source voltages of the two upper arm switches, which are shown in Fig. 10. First, if the compensation is not sufficient, the impedance of S_2 will be still comparable to the impedance of S_1. For this scenario, the dv/dt of S_2 will still be higher than that for S_1 because of the higher drain current. The steady-state voltage of S_2 will be higher than the steady-state voltage of S_1, which is shown in Fig. 10(a). Second, if the impedance reduction of S_2 just compensates the contribution of the device drain-to-ground displacement current, the dv/dt of the two switches can be equalized, as shown in Fig. 10(b). For this scenario, S_1 and S_2 are able to reach the steady-state voltages at the same time and the balanced voltage sharing is obtained. Third, if the impedance reduction of S_2 is more dominant than the contribution of the displacement current, the dv/dt of S_2 will be lower than that for S_1. However, if the large turn-off current is implemented in the middle of the dv/dt transient, the gate-to-source voltage of S_2 will drop right after that, which will increase the impedance of S_2 significantly. Therefore, after implementation of the turn-off current, the dv/dt of S_2 will be higher than that for S_1 again. For this scenario, as is shown in Fig. 10(c), the two switches can still achieve balanced voltage sharing. Last but not least, if the impedance reduction of S_2 is more dominant than the contribution of the displacement current and the large turn-off current is not implemented yet during the entire dv/dt transient, the dv/dt of S_1 will be higher than the dv/dt of S_2 during the entire dv/dt transient. As is shown in Fig. 10(d), the over-voltage breakdown can happen to the top switch S_1. This phenomenon can be considered as the over-compensated scenario, which should be avoided.

It is clear that for the well-compensated scenarios (b) and (c), the upper arm switches exhibit the desired compensation results, while for the under-compensated scenario (a) and the over-compensated scenario (d), the upper arm switches still exhibit the unbalanced voltage sharing. With the appropriate control of the compensation current amplitude and pulse-width as well as the starting timing of the large turn-off current, the desired voltage sharing scenarios (b) and (c) can be obtained. Since the proposed current source gate driver directly controls the device gate current with fine accuracy, the desired well-compensated scenarios are achieved for different operating conditions, which will be demonstrated in Section V.

It should be mentioned that the proposed method will not increase the risk of shooting through or introduce excessive extra loss. It is true that the gate-to-source voltage of S_2 is elevated to its threshold. Due to the series-connected structure, other switches in the stack are still at the gate-off state, so the shoot-through will not occur during the switching transient. Actually, the proposed method may not be suitable

for the conventional single-switch-based two-level voltage source converter, but it makes sense in the device in-series structure. Meanwhile, during the lower arm switches 'hard' turn-on transient, the load current has been transfered into the lower arm switches before the dv/dt starts. The current flowing through the upper arm switches is only the junction capacitance charging current from the dc link, which is extremely small due to the low junction capacitance value of GaN devices. Even though S_2 is an equivalent large resistor during the dv/dt transient, the extra loss is still negligible. Moreover, prior to the turn-on of the lower arm switches (during the dead-time), the elevated gate-to-source voltage of S_2 is beneficial for reducing its conduction loss, because the source-to-drain voltage drop of the device is decreased.

To determine the compensation current magnitude and the pulse-width in the hard switching scenario, it is hard to write down an analytical equation, because the resistance of the device is a multi-variable function of its gate-to-source voltage, drain-to-source voltage and its drain current. A good selection is to make the gate-to-source voltage of the device with higher dv/dt (S_2) right at its threshold voltage, so the following equation can be derived for the compensation gate charge,

$$Q_{\text{com}} = (V_{\text{th}} - V_{\text{gs(off)}}) \cdot C_{\text{gs}}. \tag{9}$$

If the under-compensated scenario is observed, the compensation gate charge should be increased. If the over-compensated scenario is observed, the compensation gate charge should be reduced. Meanwhile, the starting timing of the large turn-off gate current can be fixed at certain delay after the complimentary switches are turned on. In this study, the compensation current magnitude and pulse-width are tuned off-line based on the experimental platform and the operating conditions. The closed-loop implementation will be investigated in the future study.

IV. OPERATING PRINCIPLES AND PRACTICAL DESIGN CONSIDERATIONS OF THE PROPOSED CURRENT SOURCE GATE DRIVER

A. OPERATING PRINCIPLES OF THE PROPOSED CURRENT SOURCE GATE DRIVER

The circuit diagram of the proposed current source gate driver is shown in Fig. 11. The detailed operating principles of this circuit are explained as follows.

1) PRIMARY SIDE CURRENT SOURCE

The current mirror circuits are utilized as the primary side current source. The turn-on transient pulse current and turn-off transient pulse current are generated by two separate current mirror circuits, hence, the pulse current amplitude for the turn-on transient ($i_{\text{cs1-on}}$) and the turn-off transient ($i_{\text{cs1-off}}$) are independent, which can be calculated by,

$$\begin{aligned} i_{\text{cs1-on}} &= \frac{V_{\text{on}} - V_{\text{BE}}}{R_1}, \\ i_{\text{cs1-off}} &= \frac{V_{\text{off}} - 2V_{\text{BE}}}{R_2}, \end{aligned} \tag{10}$$

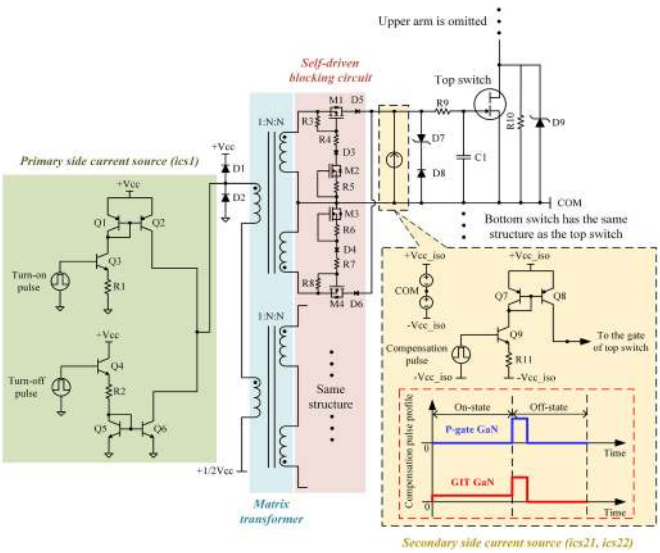

FIGURE 11. Circuit diagram of the proposed current source gate driver.

where V_{BE} is the base-to-emitter voltage drop for the BJT (around 0.7 V); V_{on} and V_{off} are the high-state values for the turn-on pulse and the turn-off pulse, respectively.

Meanwhile, two Schottky diodes (D_1 and D_2) are used to limit the output voltage of the primary current mirror circuit within $0\sim+V_{\text{cc}}$ to guarantee the BJTs ($Q_1\sim Q_6$) operate in the forward active region.

2) MATRIX TRANSFORMER

The matrix transformer with the split-winding structure is employed. The matrix transformer is defined as an array of elemental transformers interwired to form a single transformer [41]. In the proposed current source gate driver, the primary side of the element transformers are connected in series. With the identical structure for each channel, the parasitics (magnetizing inductance, leakage inductance, intra-winding and inter-winding capacitance) for different channels will be very consistent. Therefore, the induced currents for each channel will be almost the same as well, which is critical for maintaining the roughly synchronized switching timing for different channels. Meanwhile, the split-winding structure provides separate gate driving loops for the turn-on and turn-off transients. Moreover, a dc offset voltage (half of $+V_{\text{cc}}$) is applied on the primary side of the transformer to ensure that the output voltage of the primary current mirror circuit is always above zero, so the BJTs will operate in the forward active region. Moreover, the primary current mirror output voltage (transformer primary side voltage) is determined by the transformer secondary side voltage, so there is another restriction on the turns ratio of the transformer, which can be expressed as follows,

$$\frac{|V_{\text{gs(on)}}| + |V_{\text{gs(off)}}|}{N} \cdot m < +V_{\text{cc}}, \tag{11}$$

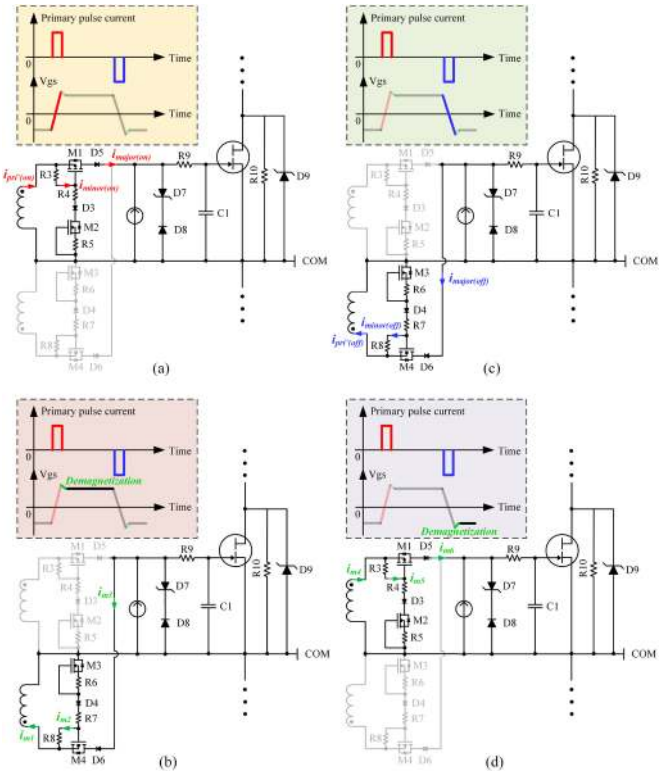

FIGURE 12. Operating principle of the self-driven blocking circuit. (a) Turn-on pulse current interval. (b) First demagnetization interval. (c) Turn-off pulse current interval. (d) Second demagnetization interval.

where $V_{gs(on)}$ and $V_{gs(off)}$ are the on-state and off-state gate-to-source voltage for the main switch; N is the turns ratio of the unit transformer and m is the number of unit transformers in the matrix transformer.

The detailed design considerations of the matrix transformer will be discussed later in this article.

3) SELF-DRIVEN BLOCKING CIRCUIT

A self-driven blocking circuit is implemented on the secondary side of the transformer. The function of this circuit is to transfer the primary side pulse current when the pulse current arises and block the discharging path for C_{gs} when the pulse current disappears in order to sustain the desired steady-state gate-to-source voltage. The operating principle of the self-driven blocking circuit is shown in Fig. 12 and the detailed operation during different intervals in one switching cycle is explained as follows.

As shown in Fig. 12(a), during this interval, the turn-on pulse current arises and the gate-to-source voltage starts to rise. The induced turn-on current ($i_{pri'(on)}$) will be split by two branches. The majority of the current ($i_{major(on)}$) will be utilized to charge C_{gs} of the main switch, while a small portion of the current ($i_{minor(on)}$) will be utilized to turn on the gate of the P-type MOSFET M_1. The magnitude of $i_{minor(on)}$ is limited by the depletion-mode MOSFET M_2, which can be calculated as,

$$i_{minor(on)} = I_{DSS} \cdot \left(1 - \frac{i_{minor(on)} \cdot R_5}{V_{th(D)}}\right)^2, \tag{12}$$

where I_{DSS} is the drain current at zero gate-to-source voltage and $V_{th(D)}$ is the threshold voltage of the depletion-mode MOSFET.

Meanwhile, the voltage drop on R_3 should be large enough to turn on the gate of M_1. Therefore, the following condition should be met,

$$i_{minor(on)} \cdot R_3 > |V_{th(P)}|, \tag{13}$$

where $V_{th(P)}$ is the threshold voltage for P-type MOSFET, which is negative.

The duration of turn-on pulse current should be long enough to ensure the gate-to-source voltage of the main switch reach the desired on-state voltage. Since there is no voltage source to clamp the gate-to-source voltage, the desired on-state voltage can be achieved by using the breakdown voltage of the Zener diode (for p-gate e-mode GaN) or using the natural forward voltage drop of the intrinsic diode between the gate and source (for GaN gate injection transistor (GIT)). This interval ends when the turn-on pulse current disappears. It should be mentioned that some margin should be reserved for the duration of the turn-on pulse in the practical design. For instance, if the rising time of the gate-to-source voltage is 50 ns, the duration of the turn-on pulse current can be set as 100 ns. After the gate-to-source voltage reaches the breakdown voltage of the Zener diode or the desired forward voltage of the intrinsic gate-to-source diode in GIT, the excessive current will flow into the Zener diode or the intrinsic gate-to-source diode, which will cause a little higher gate-to-source voltage than the desired value. During this process, the volt-second applied on the transformer is typically positive due to the extended turn-on pulse, so the magnetizing current will flow into the dot in the secondary upper winding, which will cause a little reduction of $i_{pri'(on)}$.

Once the turn-on pulse disappears, the transformer secondary upper winding will be disconnected from the main switch gate loop by the Schottky diode D_5. Due to the flux continuity, there will be a certain current continue to flow into the dot in the secondary lower winding of the transformer, as shown in Fig. 12(b). This is the so-called demagnetization process. The total demagnetizing current (i_{m1}) is the joint current of i_{m2} and i_{m3} in the two branches. The gate-to-source voltage can be discharged a little bit by i_{m3}. However, by designing the transformer with large magnetizing inductance, the magnitude of i_{m3} will be very insignificant. Meanwhile, the gate-to-source voltage is a little higher than the desired on-state value at the end of the last interval due to the extended turn-on pulse, so the gate-to-source voltage can still be very close to the desired value after the demagnetizing process. Next, the gate-to-source voltage will stay at the desired on-state value until the turn-off pulse emerges. It should be mentioned that the demagnetizing process is actually the volt-second balancing process for the transformer. During the

demagnetizing process, the negative volt-second will apply on the transformer to compensate the positive volt-second during the last interval. Once the volt-second is balanced, the demagnetizing current will disappear and the transformer winding will be disconnected from the main switch gate loop by the Schottky diode D_6. Therefore, the transformer will only be kicked in during the turn-on/turn-off transients and the following demagnetizing short intervals. The volt-second applied on the transformer will be very small, so the size of the transformer can be very tiny and the commercial pulse transformers can be utilized.

The circuit operation for the turn-off pulse current interval is very similar to the turn-on interval, as shown in Fig. 12(c). During this interval, the turn-off pulse current arises and the gate-to-source voltage starts to fall. The induced turn-off current ($i_{\mathrm{pri'(off)}}$) will be split by two branches. The majority of the current ($i_{\mathrm{major(off)}}$) will be utilized to discharge C_{gs} of the main switch, while a small portion of the current ($i_{\mathrm{minor(off)}}$) will be utilized to turn on the gate of the N-type MOSFET M_4. The magnitude of $i_{\mathrm{minor(off)}}$ is limited by the depletion-mode MOSFET M_3, which can be calculated as,

$$i_{\mathrm{minor(off)}} = I_{\mathrm{DSS}} \cdot \left(1 - \frac{i_{\mathrm{minor(off)}} \cdot R_6}{V_{\mathrm{th(D)}}}\right)^2, \tag{14}$$

where I_{DSS} is the drain current at zero gate-to-source voltage and $V_{\mathrm{th(D)}}$ is the threshold voltage of the depletion-mode MOSFET.

Meanwhile, the voltage drop on R_8 should be large enough to turn on the gate of M_4. Therefore, the following condition should be met,

$$i_{\mathrm{minor(off)}} \cdot R_8 > V_{\mathrm{th(N)}}, \tag{15}$$

where $V_{\mathrm{th(N)}}$ is the threshold voltage for N-type MOSFET, which is positive.

Similarly, the duration of turn-off pulse current should be long enough to ensure the gate-to-source voltage of the main switch reach the desired off-state voltage. Since there is no voltage source to clamp the gate-to-source voltage, the desired off-state voltage can be achieved by using the breakdown voltage of the Zener diode. This interval ends when the turn-off pulse current disappears. Again, some margin should be reserved for the duration of the turn-off pulse in the practical design. For instance, if the falling time of the gate-to-source voltage is 50 ns, the duration of the turn-off pulse current can be set as 100 ns. After the gate-to-source voltage reaches the breakdown voltage of the Zener diode, the excessive current will flow into the Zener diode, which will cause a little more negative turn-off voltage than the desired value. During this process, the volt-second applied on the transformer is typically negative due to the extended turn-off pulse, so the magnetizing current will flow out of the dot in the secondary lower winding, which will cause a little reduction of $i_{\mathrm{pri'(off)}}$.

Once the turn-off pulse disappears, the transformer secondary lower winding will be disconnected from the main switch gate loop by the Schottky diode D_6. Due to the flux continuity, there will be a certain current continue to flow out of the dot in the secondary upper winding, as shown in Fig. 12(d). The total demagnetization current (i_{m4}) is the joint current of i_{m5} and i_{m6} in the two branches. The negative gate-to-source voltage can be elevated a little bit by i_{m6}. However, by designing the transformer with large magnetizing inductance, the magnitude of i_{m6} will be very insignificant. Meanwhile, the gate-to-source voltage is a little more negative than the desired off-state value at the end of the last interval due to the extended turn-off pulse, so the gate-to-source voltage can still be close to the desired value after the demagnetization process. Next, the gate-to-source voltage will stay at the desired off-state value until the turn-on pulse in the next switching cycle occurs. Similarly, during the demagnetizing process, the positive volt-second will apply on the transformer to compensate the negative volt-second during the last interval. Once the volt-second is balanced, the demagnetizing current will disappear and the transformer winding will be disconnected from the main switch gate loop by the Schottky diode D_5.

4) SECONDARY SIDE CURRENT SOURCE

The current mirror circuits are employed as the secondary side current source as well. The compensation pulse amplitude can be calculated by,

$$i_{\mathrm{com}} = \frac{V_{\mathrm{com}} - V_{\mathrm{BE}}}{R_{11}}, \tag{16}$$

where V_{BE} is the base-to-emitter voltage drop for the BJT (around 0.7 V) and V_{com} is the amplitude of the compensation pulse voltage.

It should be mentioned that the isolated dc-dc power supplies should be employed for the secondary side current mirror circuits. Meanwhile, for GaN GIT, a constant small current (around 20 mA) should be supplied for the main switch during the entire on-state.

5) OTHER CIRCUIT ELEMENTS

The Zener diode D_7 is used to maintain the desired negative off-state gate-to-source voltage. The turn-off current pulse-width needs to be long enough to make the negative gate-to-source voltage exceed the breakdown voltage of D_7. The Schottky diode D_8 is employed for GaN GIT to prevent the forward biased of D_7. Since there is an intrinsic diode between the gate and source for GIT, it is not necessary to use another Zener diode to clamp the on-state voltage. The Schottky diode D_8 should be modified to a Zener diode for p-gate GaN to maintain the desired on-state gate-to-source voltage.

Meanwhile, the gate resistance R_9 can be utilized to damp the gate loop ringing. Since the gate current is no longer determined by the gate resistance value in the current source gate driver, the value of the gate resistance can be minimized. An external gate-to-source capacitor C_1 can be added to eliminate the effect of device input capacitance tolerance and slow down

the rising and falling of the gate-to-source voltage. A large resistor R_{10} (hundreds of kΩ) is used to maintain the initial voltage balancing for the series-connected GaN HEMTs. Moreover, a TVS diode D_9 is utilized to prevent the over-voltage breakdown of the main switch. The junction capacitance of the state-of-the-art 500∼600 V TVS diode can be as small as 10 pF, which has little impact on the switching speed of the main switch. It should be mentioned that the TVS diode D_9 is only for protection, not for voltage balancing. Hence, D_9 will only be kicked in when the device drain-to-source voltage exceeds the breakdown voltage of D_9.

B. PRACTICAL DESIGN CONSIDERATIONS OF THE PROPOSED CURRENT SOURCE GATE DRIVER

1) DESIGN CONSIDERATIONS OF CURRENT MIRROR CIRCUITS

First, the switching speed of the current mirrors should be fast enough to ensure the gate current for the main switch reach the desired value during most of time within its switching transients. The commercial state-of-the-art small signal transistors have the extremely small input and output capacitances. For example, for Diodes Incorporated 40 V/200 mA transistor pair (DMMT3904 W), the input capacitance and output capacitance are only 8 pF and 4 pF, respectively. Basically, based on the characteristics of the small signal transistors, they are able to provide very high slew rate pulse current. However, the slew rate of the pulse current is mainly restricted by the primary side leakage inductance of the transformer, which will be discussed later.

Second, the large current source can be constructed by paralleling several identical small current mirror circuits. For instance, if the output current of one small current mirror circuit is 200 mA, the 2 A pulse current can be obtained by paralleling ten identical current mirror circuits. This approach is employed in this study.

Last but not least, the power loss evaluation should be considered for the current mirror circuits. Basically, since the current mirror circuits only provide pulse current during the switching transients, the power loss is not high. If the desired turn-on and turn-off pulse current are both 2 A, the pulse duration is assumed to be 100 ns and the switching frequency is assumed to be 100 kHz, the conduction loss of the primary side current mirror circuits can be estimated as,

$$P_{\mathrm{con(cs1)}} = +V_{\mathrm{cc}} \cdot \left(i_{\mathrm{cs1-on}} \cdot \frac{t_{\mathrm{cs1-on}}}{T_{\mathrm{sw}}} + i_{\mathrm{cs1-off}} \cdot \frac{t_{\mathrm{cs1-off}}}{T_{\mathrm{sw}}} \right), \tag{17}$$

where $i_{\mathrm{cs1-on}}$, $i_{\mathrm{cs1-off}}$ are the pulse current amplitude; $t_{\mathrm{cs1-on}}$, $t_{\mathrm{cs1-off}}$ are the pulse current duration and T_{sw} is the switching cycle.

If the supplied voltage for the current mirror circuits is assumed to be +24 V, then the conduction loss for the primary side current mirror circuits is 0.96 W according to (17), which is normally very insignificant compared to the main switch power losses. Meanwhile, since the switching speed of the small signal transistors is very fast, the switching loss can be ignored for those low-voltage and low-current transistors.

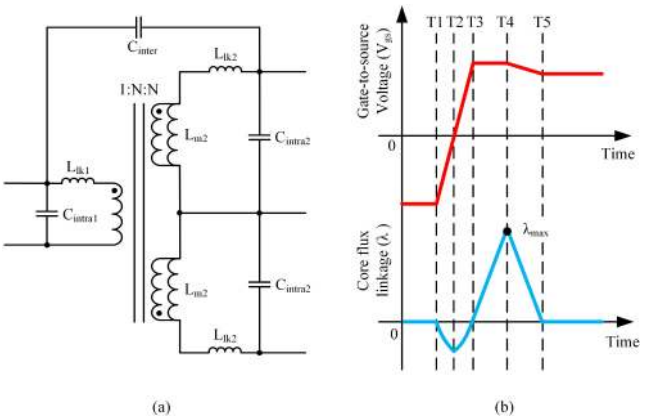

FIGURE 13. (a) Lumped model of the unit transformer. (b) Gate-to-source voltage and core flux linkage during the turn-on transient.

Moreover, for the secondary side current mirror circuits, since the pulse amplitude of the compensation current is much smaller than the primary side pulse current, the conduction loss of the secondary current mirror circuits is extremely low. It should be mentioned that for GaN GIT, the constant 20 mA gate current should be supplied for the main switch during the entire on-state, which will cause higher conduction loss for the secondary side current mirror circuits. However, the gate driving loss will be increased as well if the conventional voltage source gate driver is utilized to drive the GaN GIT. Therefore, the additional gate driving loss of the secondary side current mirrors is insignificant.

To sum, the power loss of the current mirror circuits is not a concern due to their discontinuous pulsed operation mode.

2) DESIGN CONSIDERATIONS OF MATRIX TRANSFORMER

The lumped model of the unit transformer is shown in Fig. 13(a).

First, the leakage inductance of the transformer should be minimized for the proposed current source gate driver, because it limits the slew rate of the primary current mirror output current, which can be explained by the following equation,

$$+V_{\mathrm{cc}} > L_{\mathrm{lk1}} \cdot \frac{di}{dt}, \tag{18}$$

where L_{lk1} is the primary side leakage inductance for the matrix transformer and $+V_{\mathrm{cc}}$ is the supplied voltage for the primary side current mirror circuits.

Since the voltage drop on the primary linkage inductance should not exceed the supplied voltage for the current mirror circuits, the di/dt of the pulse current is restricted. If the primary side leakage inductance of the transformer is assumed to be 100 nH and the supplied voltage for the primary current mirrors is +24 V, the di/dt will be limited to 240 mA/ns based on (18). If the desired transient turn-on/turn-off gate current is 2 A, it will take 8.3 ns to achieve the steady-state value. When

the leakage inductance becomes larger, the transient duration will be extended as well. To ensure the gate current equal its desired value during most of the time of the turn-on/turn-off transients, an external C_{gs} can be utilized to slow down the rising and falling of the gate-to-source voltage for the main switch.

For the leakage inductance on the secondary side of the transformer, as mentioned earlier, the values should be kept consistent for different channels in the stack. It can be achieved by the employment of the matrix transformer structure. In this study, the planar matrix transformer is utilized, which guarantees the consistent leakage inductances for different channels due to the fixed PCB winding structure.

Second, the magnetizing inductance of the transformer should be large enough to reduce the magnetizing current and demagnetizing current for the proposed current source gate driver. The gate-to-source voltage and the core flux linkage waveforms during the turn-on transient are shown in Fig. 13(b). The turn-off transient is very similar to the turn-on transient, so it is not shown in the figure. At T_1, the turn-on pulse current occurs and the device gate-to-source voltage starts to rise. At T_3, the device gate-to-source voltage reaches its peak value. Due to the margined turn-on pulse current, the pulse current will disappear at T_4. After T_4, the demagnetizing process starts and the process ends at T_5. The flux linkage in the core will reach its peak value at the end of the turn-on pulse (T_4). The maximum flux linkage in the core can be calculated by,

$$\lambda_{max} = (V_{gs(max)} + i_{g(on)} \cdot R_9 + V_{D5} + V_{ds(M1)}) \cdot T_{margin}, \tag{19}$$

where $V_{gs(max)}$ is the peak gate-to-source voltage; $i_{g(on)}$ is the turn-on gate current; T_{margin} is the margined pulse duration; R_9, D_5 and M_1 are the other components in the turn-on gate loop, which are shown in Fig. 11.

The magnetizing inductance should satisfy the following condition,

$$L_{m2} > \frac{\lambda_{max}}{i_{m(max)}}, \tag{20}$$

where L_{m2} is the magnetizing inductance of the secondary side and $i_{m(max)}$ is the desired maximum magnetizing current.

In this study, if the desired maximum magnetizing current is 1/10 of the turn-on pulse current; R_9 is selected to be 1 Ω; V_{D5} is around 0.5 V; $V_{ds(M1)}$ is around 0.4 V and the margined pulse duration is 50 ns, then the minimum magnetizing inductance is calculated to be only about 2 μH, which is very easy to obtain in the practical design.

Third, the intra-winding capacitance of the transformer should be minimized. The intra-winding capacitance is defined as the stray capacitance among different turns within each winding, which are shown as C_{intra1} and C_{intra2} in Fig. 13. The intra-winding capacitance can be regarded as the output capacitance for the current mirror circuits and it will draw some current during the switching transients. Meanwhile, the oscillations can occur between the intra-winding capacitance and the leakage inductance.

Fourth, the inter-winding capacitance of the transformer should be minimized as well. The inter-winding capacitance is defined as the stray capacitance between the primary winding and the secondary winding of the transformer, which is shown as C_{inter} in Fig. 13. It should be mentioned that C_{inter} represents the total inter-winding capacitance for the unit transformer in this figure. As mentioned earlier, the inter-winding capacitance can be regarded as part of the device gate-to-ground parasitic capacitances. The corresponding displacement currents can result in discrepancies in the gate currents for different channels. The discrepancies in the gate currents can be compensated by the proposed current source gate driver. Meanwhile, the displacement current flowing through the inter-winding capacitance can distort the control signal on the primary side, which may cause the mis-triggering.

Last but not least, the power loss should be considered for the transformer as well.

The core loss of the transformer can be calculated by the following equation,

$$P_{core} = K_{waveform} \cdot k \cdot f^{\alpha} \cdot {B_{max}}^{\beta} \cdot V_{core}, \tag{21}$$

where P_{core} is the core loss; B_{max} is the maximum flux density in the core; $K_{waveform}$ represents the core loss density under different excitation voltage waveforms [42]; k, α, β are Steinmetz parameters, which are provided by the manufacturer and V_{core} is the volume of the core.

The maximum flux density (B_{max}) can be calculated by the following equation,

$$B_{max} = \frac{\lambda_{max}}{A_c \cdot N}, \tag{22}$$

where A_c is the cross-section area of the core and N is the number of turns for the winding.

With the same parameters as selected earlier, if the winding only has one turn and the cross-section area is assumed to be only 5 mm×5 mm, the maximum flux density will be around 16 mT, which indicates very insignificant core loss. In the practical design, the maximum flux density can be even smaller if multiple turns are employed for the winding.

In terms of the transformer winding loss, it can be calculated by,

$$P_{winding} = \sum_{h=1}^{\infty} F_{ac(h)} \cdot {I_h}^2 \cdot R_{dc}, \tag{23}$$

where R_{dc} is the winding dc resistance value; I_h is the winding current for h^{th} harmonic component and $F_{ac(h)}$ is the winding ac factor for h^{th} harmonic component, which can be estimated by Dowell's model [43] or by FEA simulation.

Again, due to the pulsed winding current, the winding rms current is very low for the transformer. If the desired turn-on and turn-off pulse current are both 2 A, the pulse duration is assumed to be 100 ns and the switching frequency is assumed

to be 100 kHz, the winding current rms value will be only 0.28 A, which indicates very minimal winding loss.

To sum, due to the low volt-second and low rms current operating conditions for the transformer, the power loss of the transformer is not a concern for the proposed current source gate driver. Meanwhile, since the transformer only transfers pulse power, the size of the transformer can be very tiny as well.

In this study, the planar matrix transformer is employed. Due to the fixed PCB winding structure, the parasitic parameters for each unit transformer can be kept the same [44]. In terms of the insulation, the primary winding and secondary winding are placed in the two layers of the PCB, the interlayer insulation voltage level of the PCB is far beyond the voltage level for the test. However, sufficient creepage distance should be reserved between the winding and the core based on the corresponding insulation standard.

3) DESIGN CONSIDERATIONS OF THE SELF-DRIVEN BLOCKING CIRCUIT

The current rating and power loss should be considered for the auxiliary switches (M_1, M_2, M_3, M_4) in the self-driven blocking circuit (shown in Fig. 11). Since the major component of the pulse current will flow through M_1 and M_4, their current rating for these two auxiliary switches should be larger than the pulse current amplitude. Lower current rating devices can be selected for the other two auxiliary switches M_2 and M_3.

In terms of the power loss produced in the auxiliary switches, due to the very short pulse current, the loss is typically in the range of tens of mW. Therefore, the power loss generated in the self-driven blocking circuit is extremely insignificant.

4) DESIGN CONSIDERATIONS OF OTHER CIRCUIT ELEMENTS

It is found in the experiments that the device off-state voltage is not stabilized at the desired value if only the Zener diode (D_7 in Fig. 11) is employed. Without the constant reverse current flowing through the Zener diode, the breakdown voltage can not be maintained at the nominal value. To solve this issue, a low-voltage MOSFET can be connected between the gate and the negative rail of the secondary side power supply ($-V_{cc(iso)}$ in Fig. 11). After the gate-to-source voltage drops below the desired off-state voltage, the MOSFET should be turned on to clamp the gate-to-source voltage at the desired off-state value. The operating principle is similar to the active Miller clamping in the conventional voltage source gate driver [45]. The secondary side isolated power supply (voltage source) is only for clamping the gate voltage, which should be kicked in after the turn-off transient. The transient turn-off gate current is still supplied by the current source gate driver, so the dv/dt during the switching transients can be accurately regulated by adjusting the supplied gate current. This function will be implemented in the future prototype.

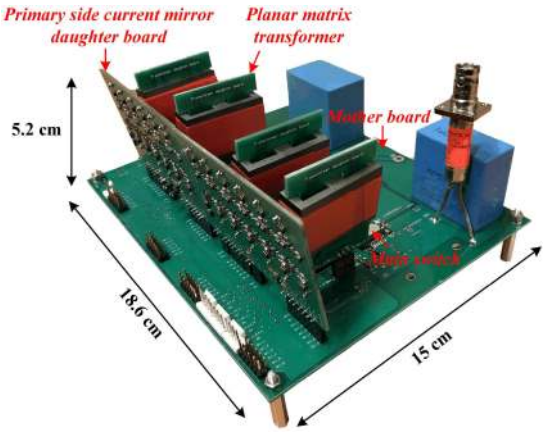

FIGURE 14. Prototype of a series-connected GaN-based multiple pulse tester with the proposed current source gate driver.

V. EXPERIMENTAL VERIFICATION

A. A SERIES-CONNECTED GAN-BASED MULTIPLE PULSE TESTER WITH THE PROPOSED CURRENT SOURCE GATE DRIVER

A series-connected GaN-based multiple pulse tester (MPT) with the proposed current source gate driver is designed and fabricated as shown in Fig. 14. The MPT is basically a half-bridge converter. A 300 μH air-core inductor is paralleled with the upper arm. Two series-connected GaN HEMTs are employed for both the upper arm and the lower arm of the MPT. The setup of the MPT is the same as the circuit shown in Fig. 2. The two upper arm switches are labeled as S_1 (top switch) and S_2 (bottom switch), while the two lower arm switches are labeled as S_3 (top switch) and S_4 (bottom switch). Although two switches are connected in series for the prototype, the proposed current source gate driver and voltage balancing strategies can be extended for more switches-in-series scenarios.

It should be mentioned that the modular design is chosen in this study, so the power density of the prototype is not optimized. Infineon 600 V/30 A e-mode GaN (IGOT60R070D1) devices (GIT) are employed in this prototype. The secondary side current mirrors and the self-driven blocking circuits are on the back of the mother board in the prototype. The selected components for the proposed current source gate driver are listed in Table 2. The labels of the components are consistent with the labels presented in Fig. 11. Multiple small current mirrors are paralleled to construct the large current source for the primary side. Meanwhile, R_1, R_2 and R_{11} can be adjusted based on the desired gate current value. Moreover, the planar matrix transformer is employed for this prototype. The critical parameters for each unit transformer is listed in Table 3.

The gate driving loss is normally a big concern for the current source gate driver. To evaluate the gate driving loss of the proposed current source gate driver. The turn-on and turn-off pulse currents for the primary current mirrors are selected to

TABLE 2. Selected Components for the Proposed Current Source Gate Driver

Components	Values
Main switch	Infineon IGOT60R070D1
Q_1, Q_2, Q_7, Q_8	Diode Incorporated DMMT3906W
Q_3, Q_4, Q_9	On Semiconductor FMB3904
Q_5, Q_6	Diode Incorporated DMMT3904W
M_1	ROHM RQ5H020SP
M_2, M_3	Infineon BSS159N
M_4	ROHM RSR030N06HZG
Schottky diode	STMicroelectronics STPS140Z
Zener diode	Central Semiconductor CMDZ5233B
R_3, R_8	30 Ω
R_4, R_7	0 Ω
R_5, R_6	1.3 Ω
R_9	1 Ω
R_{10}	330 kΩ

TABLE 3. Critical Parameters for the Unit Planar Transformer

Parameters	Values
Magnetic core material	Ferroxube 3F36
Cross-section area	194 mm^2
Number of turns	1:2:2
Winding width	100 mil (pri.); 50 mil (sec.)
Winding thickness	1 oz
Creepage distance (between winding and core)	150 mil
Magnetizing inductance	6.26 μH
Leakage inductance per line	188 nH
Total stray capacitance referred to primary side	189.6 pF

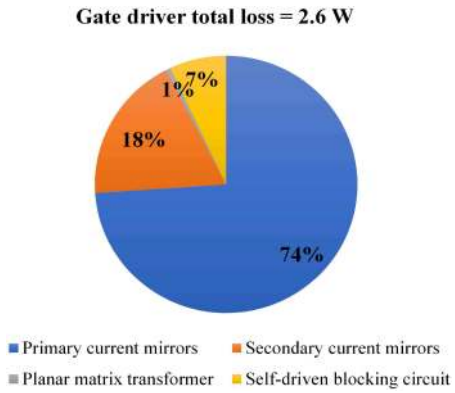

FIGURE 15. Power loss breakdown for the proposed current source gate driver.

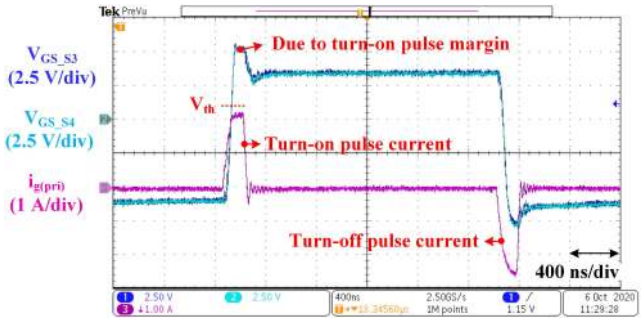

FIGURE 16. Gate-to-source voltages of the two lower arm switches (S_3, S_4) and the gate current of the transformer primary side.

be 2 A; the continuous on-state gate current for GaN GIT is 20 mA; the switching frequency is considered to be 100 kHz and the duty cycle is 0.5. Then the total power dissipation in the proposed current source gate driver for driving all four switches is around 2.6 W, which is insignificant compared with main switches power losses for most of the applications. The corresponding power loss breakdown for the proposed current source gate driver is shown in Fig. 15. It is clear that the power loss for the current mirrors is dominant in the total gate driving loss. It is understandable because the BJTs are in the active forward region in the current mirror circuits, which exhibit higher transistor voltage drop. However, due to the discontinuous pulsed operation of the current mirrors, the total loss of the proposed current source gate driving circuit is still acceptable.

Without the main power, the gate-to-source voltages of the lower arm switches and the gate current of the transformer primary side are shown in Fig. 16. The following conclusions can be obtained based on the waveforms. First, the synchronization of the gate-to-source voltages for different switches in the stack is pretty good. As mentioned earlier in the article, the structure of the proposed current source gate driver almost eliminates the discrepancies of the propagation delays and the gate loop parasitics. Second, the slew rate (di/dt) of the turn-on/turn-off pulse currents are restricted by the transformer leakage inductance. However, by designing the low leakage inductance transformer, the pulse currents can attain the desired values before the device gate-to-source voltage reaches the threshold. Last but not least, the overshoot in the gate-to-source voltage is due to the turn-on/turn-off pulse margin, which is essential to guarantee the safe turn-on/turn-off of the main switches.

B. VERIFICATION OF THE PROPOSED VOLTAGE BALANCING STRATEGY IN SOFT SWITCHING SCENARIO

1) CASE 1: DRAIN-TO-SOURCE DV/DT IS RESTRICTED BY THE GATE CURRENT

As mentioned earlier in the article, due to the concern of insulation or EMI issues, the maximum dv/dt is restricted by reducing the gate current in some practical applications. For the conventional voltage source gate driver, a large gate resistor is typically used to reduce the gate current. For the proposed current source gate driver, the primary side current mirror output can be directly decreased.

The waveforms for the lower arm switches (S_3, S_4) turn-off transient in the 600 Vdc and 25 A drain current condition are captured. As is shown in Fig. 17, without the active gate

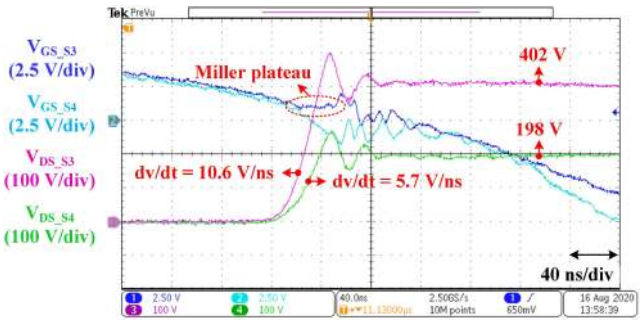

FIGURE 17. Gate-to-source voltages and drain-to-source voltages of the two lower arm switches (S_3, S_4) without active gate current control for soft switching case 1.

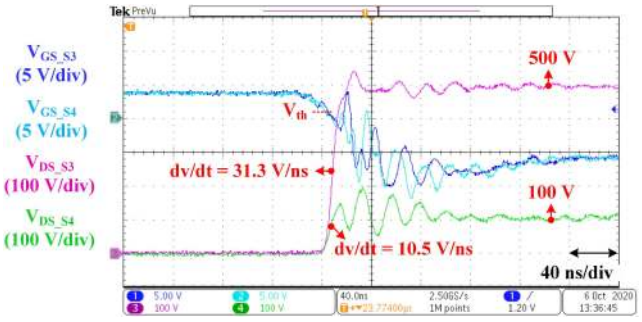

FIGURE 19. Gate-to-source voltages and drain-to-source voltages of the two lower arm switches (S_3, S_4) without active gate current control for soft switching case 2.

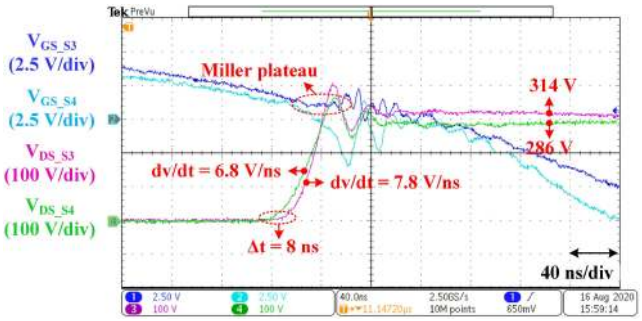

FIGURE 18. Gate-to-source voltages and drain-to-source voltages of the two lower arm switches (S_3, S_4) with active gate current control for soft switching case 1.

current control, the top switch S_3 exhibits higher dv/dt than the bottom switch S_4 does, which results in the 68% voltage difference compared with the desired average value (300 V). Although the gate current provided by the proposed current source gate driver is almost the same for both switches, the top switch has higher total gate current thanks to the contribution from the gate-to-ground displacement current (labeled as i_{p3} in Fig. 2).

With the implementation of the active gate current control, the total gate current for the top switch is reduced by increasing the compensation current on the secondary side of the gate driver, so the dv/dt of the top switch is reduced. Meanwhile, since the gate-to-source voltage of the top switch reaches its Miller plateau voltage a little bit later, the dv/dt starting timing of the top switch is delayed as well (delayed by 8 ns). The voltage difference of the two switches is cut down to 9.3% compared with the desired average value, as shown in Fig. 18. The experimental results successfully validate the theoretical analysis in Fig. 3.

2) CASE 2: DRAIN-TO-SOURCE DV/DT IS RESTRICTED BY THE DRAIN/LOAD CURRENT

As mentioned earlier in the article, if the turn-off gate current provided by the gate driver is sufficient, the dv/dt is typically limited by the drain/load current for GaN devices. With sufficient turn-off gate current, the device channel will be cut off very quickly, which is beneficial for reducing the device switching energy.

The waveforms for the lower arm switches (S_3, S_4) turn-off transient in the 600 Vdc and 25 A drain current condition are captured. As shown in Fig. 19, without the active gate current control, the top switch S_3 exhibits higher dv/dt than the bottom switch S_4 does, which results in the 133% voltage difference compared with the desired average value (300 V). It is clear that during most of the time in the dv/dt transient the gate-to-source voltages of the two switches already drop below the threshold. Therefore, the voltage sharing difference is caused by the variance in the drain current because of the contribution from the drain-to-ground displacement current (labeled as i_{p6} in Fig. 2).

With the implementation of the active gate current control, the total gate current for the top switch is reduced by increasing the compensation current on the secondary side of the gate driver, so the dv/dt starting timing of the top switch is delayed (delayed by 3.7 ns). Although the dv/dt of the top switch is still higher than the bottom switch, the two switches can reach the steady state value at the same time due to the starting timing difference. The voltage difference of the two switches is cut down to 10% compared with the desired average value, as shown in Fig. 20. The experimental results successfully validate the theoretical analysis in Fig. 4.

C. VERIFICATION OF THE PROPOSED VOLTAGE BALANCING STRATEGY IN HARD SWITCHING SCENARIO

When the lower arm switches (S_3, S_4) are 'hard' turned on, the drain-to-source voltages of the upper arm switches (S_1, S_2) are forced to be pulled up and the voltage imbalance occurs, as shown in Fig. 21. It is clear that the gate-to-source voltage of S_2 is far below the threshold when the dv/dt occurs, so the impedance of S_2 is very high during this transient. The existence of the device drain-to-ground capacitance will lead to the variance in the device drain currents, which results in the voltage imbalance. In the operating condition of 600 Vdc and 25 A drain current, the bottom switch S_2 exhibits higher

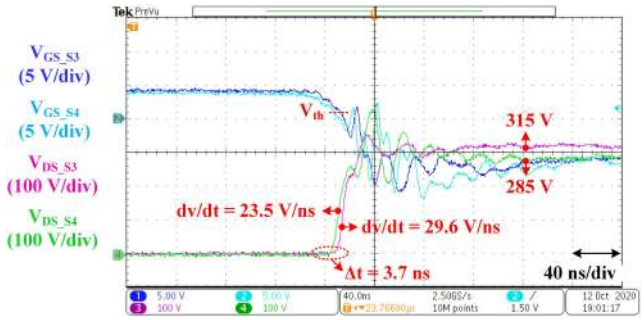

FIGURE 20. Gate-to-source voltages and drain-to-source voltages of the two lower arm switches (S_3, S_4) with active gate current control for soft switching case 2.

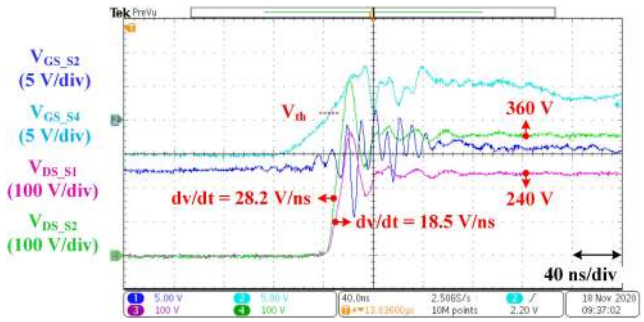

FIGURE 21. Gate-to-source voltages and drain-to-source voltages without active gate current control for hard switching scenario.

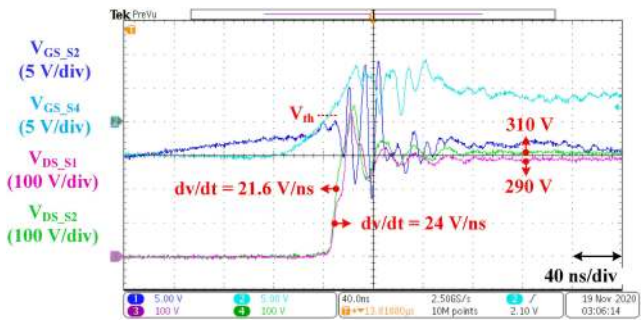

FIGURE 22. Gate-to-source voltages and drain-to-source voltages with active gate current control for hard switching scenario.

dv/dt than the top switch S_1 does. The voltage difference is 40% compared with the average value (300 V).

With the implementation of the active gate current control, the compensation current is injected into the gate of S_2 to elevate its gate-to-source voltage closer to the threshold voltage when the dv/dt occurs. The dv/dt of the bottom switch S_2 is decreased due to its reduced impedance. After the dv/dt transient is finished, the gate-to-source voltage of S_2 is pulled down again by a large turn-off current to maintain the safe turn-off of S_2. The voltage difference of the two switches is cut down to 6.7% compared with the desired average value,

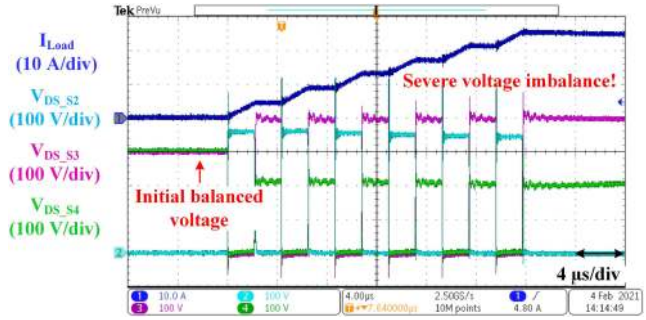

FIGURE 23. Drain-to-source voltages and load current in the multiple pulse test with only 300 pF/10 Ω RC snubber.

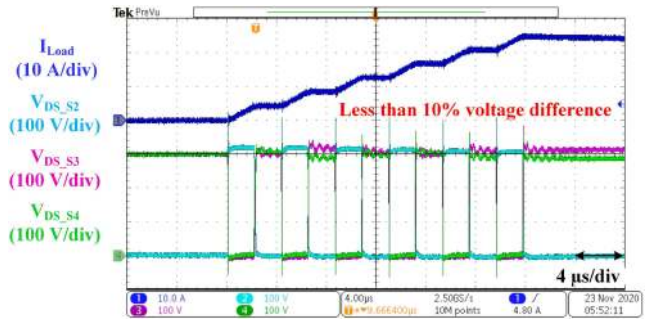

FIGURE 24. Drain-to-source voltages and load current in the multiple pulse test with 300 pF/10 Ω RC snubber (optional) and active gate current control.

as shown in Fig. 22. The experimental results successfully validate the theoretical analysis in Fig. 9 and Fig. 10.

D. VERIFICATION OF THE PROPOSED VOLTAGE BALANCING STRATEGY FOR DIFFERENT LOAD AND DIFFERENT SWITCHING SPEED CONDITIONS

To verify the voltage balancing function of the proposed current source gate driver in different load and different switching speed (dv/dt) conditions, the multiple pulse test at 600 Vdc and 0∼25 A load current is conducted. The desired amplitude and the pulse-width of the compensation current are tuned off-line for different load current conditions and directly programmed in the controller. Meanwhile, the gate current supplied by the gate driver is sufficient and the lower arm switches turn-off dv/dt is almost determined by the load current amplitude. A very small RC snubber circuit (300 pF/10 Ω) is utilized to damp the V_{ds} ringing for the switches. Such small snubber circuit will offer little help to the voltage balancing and the snubber circuit is totally optional. As is shown in Fig. 23, with only the small RC snubber (without active gate current control), the severe voltage imbalance among the series-connected switches is still observed. After implementing the proposed active gate current control, the voltage difference among the switches is suppressed below 10% compared with the average value (300 V) for the whole load current range, as shown in Fig. 24. It should be mentioned that since

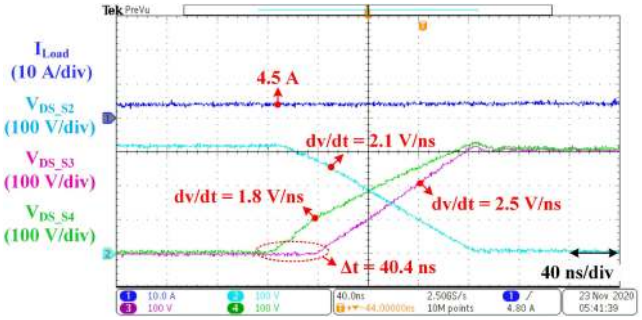

FIGURE 25. Lower arm switches turn-off at 4.5 A load current condition.

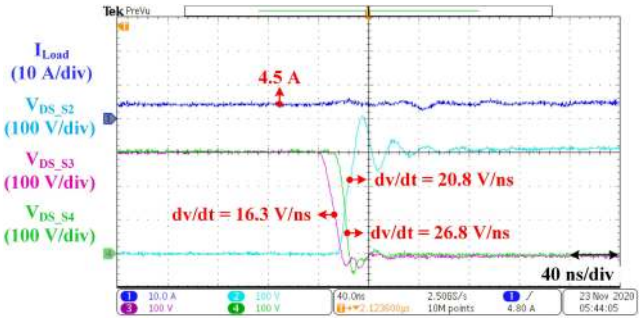

FIGURE 26. Lower arm switches turn-on at 4.5 A load current condition.

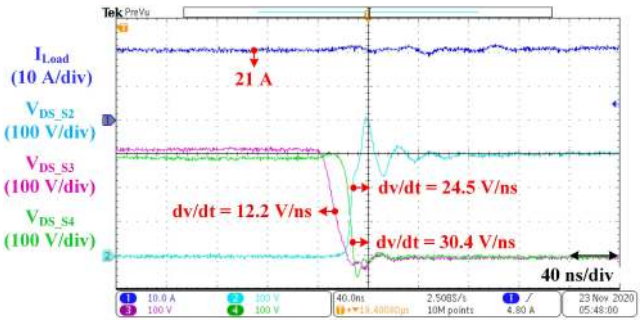

FIGURE 27. Lower arm switches turn-on at 21 A load current condition.

the off-state drain-to-source voltage of S_2 is very close to half of the dc link voltage, the off-state drain-to-source voltage of S_1 will be almost equalized to half of the dc link voltage as well. The oscilloscope used in the test only has four channels, so the drain-to-source voltage of S_1 is not presented in the experimental waveforms.

The zoomed-in switching waveforms for the light load condition are shown in Fig. 25 and Fig. 26, while the zoomed-in switching waveforms for the heavy load condition are shown in Fig. 27 and Fig. 28. Based on these waveforms, the following conclusions can be made.

First, for the lower arm switches turn-off transients (Fig. 25 and Fig. 28), the desired dv/dt starting timing difference is larger for the light load condition, which indicates larger compensation current amplitude or longer compensation current

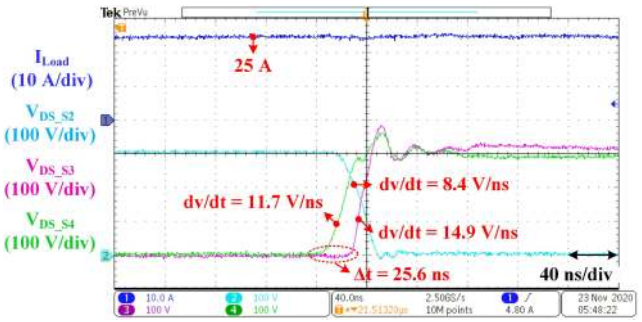

FIGURE 28. Lower arm switches turn-off at 25 A load current condition.

pulse-width should be implemented for lighter load condition. Second, for the lower arm switches turn-on transients (Fig. 26 and Fig. 27), the over-voltage is not observed for the lower arm switches, although their dv/dt is different. Actually, the proposed current source gate driver offers the capability of compensating the gate current difference during the turn-on transient as well, which can achieve similar dv/dt and switching energies for the series-connected switches during the turn-on transient. Since this study is aimed at achieving the drain-to-source voltage balancing of the series-connected switches, the turn-on transient gate current compensation is not implemented. It should be also mentioned that the dv/dt in the lower arm turn-off transient is decreased due to the existence of the small RC snubber circuit (300 pF/10 Ω). The proposed voltage balancing strategy is already validated in the high dv/dt condition without the snubber circuit (Fig. 19 and Fig. 20). Again, the employment of the snubber circuit is only for reducing the V_{ds} ringing for the series-connected switches and the snubber circuit is totally not required.

To sum, based on the experimental results, the voltage balancing function of the proposed current source gate driver works pretty well in different load current and different switching speed (dv/dt) conditions.

E. SWITCHING ENERGY EVALUATION FOR THE SERIES-CONNECTED GAN HEMTS WITH THE PROPOSED CURRENT SOURCE GATE DRIVER

To evaluate the switching energy for the series-connected switches, lower arm device current is measured by T&M Research SDN-414 current shunt (shown in Fig. 14). The captured turn-on and turn-off waveforms are presented in Fig. 29 and Fig. 30, respectively. The turn-on and turn-off energies of a single 1.2 kV/30 A SiC MOSFET (C3M0075120 J) under the same operating condition (Vdc, load current and similar dv/dt) are set as the benchmark, which are shown in Fig. 29 and Fig. 30 as well. Based on the experimental results, the following conclusions can be made.

First, the total turn-on energy of the series-connected GaN HEMTs is 65.1% less than the turn-on energy of a single SiC MOSFET under the same operating condition. Due to the lack of the body diode in GaN HEMTs, the turn-on energy is significantly reduced (no reverse recovery energy for the upper arm

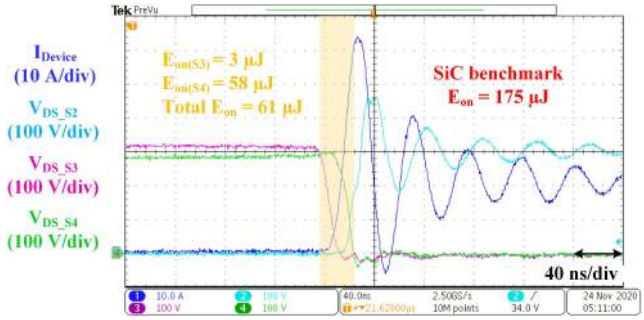

FIGURE 29. Lower arm switches turn-on energy at 21 A load current condition.

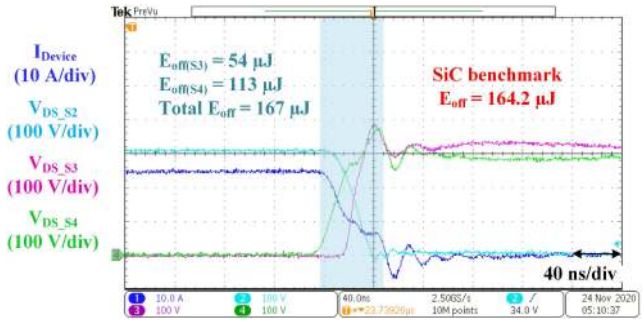

FIGURE 30. Lower arm switches turn-off energy at 25 A load current condition.

body diode). Even considering the small RC snubber circuit energy (300 pF/10 Ω), which is 27 μJ, the total turn-on energy (including the snubber energy) of the series-connected GaN solution is still 50% less than the turn-on energy of the single SiC solution. Moreover, as mentioned earlier in the article, the snubber circuit is totally not required for the proposed voltage balancing strategy.

Second, the total turn-off energy of the series-connected GaN HEMTs is almost the same as the turn-off energy of a single SiC MOSFET under the same operating condition. It is a fair comparison, because the switching speed (dv/dt) for the two solutions is kept nearly the same.

Last but not least, the switching energy distribution among the series-connected switches is not even for both turn-on and turn-off transients. For the turn-on transient, the bottom switch S_4 generates more switching energy than the top switch S_3 does, due to the difference in both the starting timing and the slew rate of the drain-to-source voltages for the two switches. The dv/dt starting timing difference of the two switches is caused by the Zener diode voltage clamping. As discussed earlier, the Zener diode clamping can not guarantee the consistent off-state gate-to-source voltage. The active clamping method will be used to solve this issue in the future prototype. For the slew-rate difference, the proposed current source gate driver offers the capability of regulating the turn-on gate currents for the switches in the stack. It is not hard to achieve more balanced turn-on energies for the series-connected switches, which will be investigated in the future study as well. It should be mentioned that the large ringing in the device current and drain-to-source voltage of S_2 (as shown in Fig. 29) is due to the increased power loop stray inductance introduced by the current shunt. If the current shunt is replaced by a short conductor, the ringing will be much smaller (as shown in Fig. 27). For the turn-off transient, similarly, the switching energy in the bottom switch S_4 is higher than the switching energy in the top switch S_3, due to the difference in both the starting timing and the slew rate of the drain-to-source voltages for the two switches. The proposed method actually utilizes the starting timing difference to compensate the dv/dt difference for achieving the balanced voltage sharing, so the uneven turn-off energy distribution in the series-connected switches is inevitable. This is a common drawback for the so-called active gate driving delay control method [14], [33]. However, the uneven turn-off energy distribution is significantly less pronounced for higher dv/dt operating conditions, because the dv/dt starting timing difference is much shorter. For the operating condition in Fig. 20, the turn-off energy difference between the two series-connected switches is only around 5%. In the practical applications, high dv/dt usually occurs at heavier load conditions. Therefore, for heavier load conditions, the uneven turn-off energy distribution among the series-connected switches will be less pronounced. Since the thermal design of the system is usually to fit the worst operating condition (heaviest load condition), the proposed current source gate driver and the voltage balancing strategy will have little impact on the thermal design in the practical power converter system. Moreover, to further tackle the issue of the thermal imbalance, the proposed strategy in hard switching scenario can be utilized in the soft switching scenario as well. When the lower arm switches are experiencing 'soft' turn-off, the gate-to-source voltage of device with higher dv/dt can be regulated around its threshold level. The reduction of the impedance for the device can counteract the effect from the drain-to-ground displacement current. In this way, the dv/dt of the series-connected switches can be well matched, as well as the thermal stress for the switches in the stack. This strategy is already validated for the hard switching scenario in this study (Fig. 21 and Fig. 22) and the same strategy will be investigated for the soft switching scenario in the future study.

To sum, the total switching energy for the series-connected GaN solution is 33.6% less than the total switching energy for the SiC solution under the same operating condition, so the series-connected GaN solution can improve the system efficiency significantly for the applications in which the switching loss is more dominant. Meanwhile, the uneven switching energy distribution among the series-connected switches is not pronounced for heavier load conditions, so it is not an issue for the thermal design in the practical power converter system.

VI. CONCLUSION

In this article, a novel current source gate driver is proposed, which addresses the voltage balancing issue for the series-connected GaN HEMTs. The large current source on

the primary side and the matrix transformer structure eliminate the discrepancies in the gate driving propagation delay and the gate driving loop parasitics for the series-connected switches in the stack. The small current sources on the secondary side compensate the voltage sharing difference caused by the displacement currents flowing through the device-to-ground parasitic capacitances. The current-mirror-based discontinuous pulsed current source introduces insignificant additional gate driving loss. Meanwhile, the voltage balancing strategies for both soft switching and hard switching scenarios are presented. A series-connected GaN-based multiple pulse tester is built to validate the proposed current source gate driver and the voltage balancing strategies. The experimental results coincide with the theoretical analysis pretty well for both soft switching and hard switching scenarios. With the implementation of the proposed voltage balancing strategy, the series-connected GaN HEMTs exhibit less than 10% voltage difference under different load and different switching speed conditions. Moreover, it is verified that the series-connected GaN solution saves 33.6% switching energy compared with the single SiC solution under the same operating condition. Therefore, the series-connected GaN solution can improve the system efficiency if the switching loss is dominant in the system. In the future, the closed-loop control will be implemented for the proposed current source gate driver to make the proposed approach more adaptive to various operating conditions.

REFERENCES

[1] J. Yu, R. Burgos, N. R. Mehrabadi, and D. Boroyevich, "Design of a sic-based modular multilevel converter for medium voltage DC distriution system," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 467–473.

[2] N. Doerry and K. Moniri, "Specifications and standards for the electric warship," in *Proc. IEEE Elect. Ship Technol. Symp.*, 2013, pp. 21–28.

[3] J. E. Huber and J. W. Kolar, "Optimum number of cascaded cells for high-power medium-voltage AC-DC converters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 213–232, Mar. 2017.

[4] L. Wang, Q. Zhu, W. Yu, and A. Q. Huang, "A medium-voltage medium-frequency isolated dc-dc converter based on 15-kv sic mosfets," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 100–109, Mar. 2017.

[5] M. Shojaie, N. Elsayad, H. Moradisizkoohi, and O. A. Mohammed, "Design and experimental verification of a high-voltage series-stacked gan ehemt module for electric vehicle applications," *IEEE Trans. Transport. Electrific.*, vol. 5, no. 1, pp. 31–47, Mar. 2019.

[6] Z. Zhang, L. M. Tolbert, D. Costinett, F. Wang, and B. J. Blalock, "A new hands-on course in characterization of wide-bandgap devices," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9392–9403, Oct. 2019.

[7] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial gan power devices and gan-based converter design challenges," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.

[8] S. Madhusoodhanan, K. Mainali, A. K. Tripathi, A. Kadavelugu, D. Patel, and S. Bhattacharya, "Power loss analysis of medium-voltage three-phase converters using 15-kv/40-a sic N-IGBT," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 902–917, Sep. 2016.

[9] K. Vechalapu, S. Bhattacharya, E. Van Brunt, S.-H. Ryu, D. Grider, and J. W. Palmour, "Comparative evaluation of 15-kv sic mosfet and 15-kv sic IGBT for medium-voltage converter under the same DV/DT conditions," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 469–489, Mar. 2017.

[10] H. Nie *et al.*, "1.5-kv and 2.2-m $\omega - \text{cm}^2$ vertical gan transistors on bulk-gan substrates," *IEEE Electron. Device Lett.*, vol. 35, no. 9, pp. 939–941, Sep. 2014.

[11] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[12] A. Hensler, S. Franz, D. Shapiro, and G. Bunin, "800v synchronous buck converter with series-connected GAN power transistors," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2018, pp. 1–7.

[13] A. Marzoughi, R. Burgos, and D. Boroyevich, "Active gate-driver with DV/DT controller for dynamic voltage balancing in series-connected sic mosfets," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2488–2498, Apr. 2019.

[14] T. Wang, H. Lin, and S. Liu, "An active voltage balancing control based on adjusting driving signal time delay for series-connected sic mosfets," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 454–464, Mar. 2020.

[15] N. Rouger, J.-C. Crébier, and S. Catellani, "High-efficiency and fully integrated self-powering technique for intelligent switch-based flyback converters," *IEEE Trans. Ind. Appl.*, vol. 44, no. 3, pp. 826–835, May–Jun. 2008.

[16] J. Roig *et al.*, "Series-connected gan transistors for ultra-fast high-voltage switch (>1 kv)," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 3043–3048.

[17] X. Huang, "High frequency gan characterization and design considerations," Ph.D. dissertation, Bradley Dept. Elect. Comput., Eng., Eng., Virginia Tech, 2016.

[18] M. Shojaie, N. Elsayad, S. Tabarestani, and O. Mohammed, "A bidirectional buck-boost converter using 1.3 kv series-stacked GAN e-HEMT modules for electric vehicle charging application," in *Proc. IEEE 6th Workshop Wide Bandgap Power Devices Appl.*, 2018, pp. 82–87.

[19] Y. Abe and K. Maruyama, "Multi-series connection of high-voltage IGBTS," *Fugi Electric J.*, vol. 75, no. 8, pp. 1–4, 2002.

[20] H. Zhang, J. Imaoka, M. Noah, Y. Ishikura, and M. Yamamoto, "Study on the imbalanced voltage of series-connected active power semiconductor devices in power conversion systems," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, 2019, pp. 1–4.

[21] S. Ji, T. Lu, Z. Zhao, H. Yu, and L. Yuan, "Series-connected HV-IGBTS using active voltage balancing control with status feedback circuit," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4165–4174, Aug. 2015.

[22] T. C. Lim, B. W. Williams, and S. J. Finney, "Active snubber energy recovery circuit for series-connected IGBTS," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1879–1889, Jul. 2011.

[23] J. WonDong-Wook BaekYoo, and Heung-GeunKim, "High-voltage switch using series-connected igbts with simple auxiliary circuit," *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 1832–1839, Nov./Dec. 2001.

[24] T. C. Lim, B. W. Williams, S. J. Finney, and P. R. Palmer, "Series-connected igbts using active voltage control technique," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4083–4103, Aug. 2013.

[25] F. Zhang, X. Yang, Y. Ren, L. Feng, W. Chen, and Y. Pei, "A hybrid active gate drive for switching loss reduction and voltage balancing of series-connected IGBTS," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7469–7481, Oct. 2017.

[26] R. Wang, L. Liang, Y. Chen, and Y. Kang, "A single voltage-balancing gate driver combined with limiting snubber circuits for series-connected sic mosfets," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 465–474, Mar. 2020.

[27] F. Zhang, X. Yang, W. Chen, and L. Wang, "Voltage balancing control of series-connected sic mosfets by using energy recovery snubber circuits," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10200-10212, Oct. 2020.

[28] Q. Lei, C. Liu, Y. Si, and Y. Liu, "A standard block of "series connected sic mosfet" for medium/high voltage converter," in *Proc. Int. Power Electron. Conf.*2018, pp. 3742–3748.

[29] L. Pang, T. Long, K. He, Y. Huang, and Q. Zhang, "A compact series-connected sic mosfets module and its application in high voltage nanosecond pulse generator," *IEEE Trans. Ind. Electron.*, vol. 66, no. 12, pp. 9238–9247, Dec. 2019.

[30] Y. Ren *et al.*, "A compact gate control and voltage-balancing circuit for series-connected sic mosfets and its application in a DC breaker," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8299–8309, Oct. 2017.

[31] Y. Ren, X. Yang, F. Zhang, F. Wang, L. M. Tolbert, and Y. Pei, "A single gate driver based solid-state circuit breaker using series connected sic mosfets," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2002–2006, Mar. 2019.

[32] R. Wang, L. Liang, Y. Chen, and Y. Kang, "A single voltage-balancing gate driver combined with limiting snubber circuits for series-connected sic mosfets," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 465–474, Mar. 2019.

[33] Z. Zhang *et al.*, "High precision gate signal timing control based active voltage balancing scheme for series-connected fast switching field-effect transistors," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 925–930.

[34] X. Lin, L. Ravi, Y. Zhang, R. Burgos, and D. Dong, "Analysis of voltage sharing of series-connected high voltage sic mosfets and body-diodes," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7612–7624, Jul. 2021.

[35] X. Chen, W. Chen, X. Yang, Y. Han, X. Hao, and T. Xiao, "Research on a 4000-v-ultrahigh-input-switched-mode power supply using series-connected mosfets," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5995–6011, Jul. 2018.

[36] T. Van Nguyen, P. Jeannin, E. Vagnon, D. Frey, and J. Crebier, "Series connection of IGBTS with self-powering technique and 3-D topology," *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1844–1852, Jul./Aug. 2011.

[37] L. F. S. Alves, P. Lefranc, P. Jeannin, B. Sarrazin, and J. Crebier, "Multi-step packaging concept for series-connected sic mosfets," in *Proc. 21st Eur. Conf. Power Electron. Appl.*, 2019, pp. P.1–P.10.

[38] Y. He and D. J. Perreault, "Diode evaluation and series diode balancing for high-voltage high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6301–6314, Jun. 2020.

[39] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched ALL-SI, SI-SIC, and ALL-SIC device combinations," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2393–2407, May 2014.

[40] M. J. Melfi, "Low-voltage PWM inverter-fed motor insulation issues," *IEEE Trans. Ind. Appl.*, vol. 42, no. 1, pp. 128–133, Jan./Feb. 2006.

[41] E. Herbert, "Design and Application Oi Matrix Transformers," FMTT, Incorporated, p. 162, 1990.

[42] W. A. Roshen, "A practical, accurate and very general core loss model for nonsinusoidal waveforms," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 30–40, Jan. 2007.

[43] P. L. Dowell, "Effects of eddy currents in transformer windings," *Proc. Elect. Eng., Inst.*, vol. 113, no. 8, pp. 1387–1394, Aug. 1966.

[44] Z. Zhang, C. Liu, M. Wang, Y. Si, Y. Liu, and Q. Lei, "High-efficiency high-power-density CLLC resonant converter with low-stray-capacitance and well-heat-dissipated planar transformer for EV on-board charger," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10831–10851, Oct. 2020.

[45] L. Dulau, S. Pontarollo, A. Boimond, J. Garnier, N. Giraudo, and O. Terrasse, "A new gate driver integrated circuit for IGBT devices with advanced protections," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 38–44, Jan. 2006.