A Novel Dimension Reduction Technique for the Capacitance Extraction of 3D VLSI Interconnects

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Abstract

In this paper, we present a new capacitance extraction method named Dimension Reduction Technique (DRT) for 3D VLSI interconnects. The DRT converts a complex 3D problem into a series of cascading simple 2D problems. Each 2D problem is solved separately, so we can choose the most efficient method according to the arrangement of conductors. More importantly, it is very easy to obtain the analytical solutions of 2D problem in many layers such as the pure dielectric layers and the layers with parallel signal lines. Therefore, the domain that has to be analyzed numerically is minimized. This leads to the drastic reduction of the computing time and memory needs. We have used the DRT to extract the capacitances of multilayered and multiconductor cross-overs, bends, via with signal lines and open-end. The results are in good agreement with those of Ansoft's SPICELINK and MIT's FastCap, But the computing time and memory size used by the DRT are several even tens times less than those used by SPICELINK and FastCap.

1 Introduction

With continuous increase in the clock rate of high speed VLSI system and decrease in the feature size of the interconnects and packages of VLSI circuit chips, the resultant signal delay, crosstalk, distortion and reflection may degrade the system performance. Analysis of these negative effects has become as important as the circuit design. This has increased the interest in the efficient methods for calculating electrical parameters of the interconnects and packages.

Many numerical methods have been applied to extract the electrical parameters of the interconnects and packages. These methods can be generally classified into two categories: integral equation methods and differential equation methods. The differential equation methods, such as Finite Element Method (FEM)[1] and Finite Difference Method (FDM)[2], divide an interconnect cell into meshes and lead to a large scale sparse matrix equation. Though the compressed storage technique and some efficient sparse matrix equation solvers may be applied, the solving process is still time-consuming and needs huge memory. The integral equation methods, such as the Method of Moments(MoM)[3, 4] and the Boundary Element Method (BEM)[5, 6], divides the surfaces of conductors and the interfaces of dielectric layers into meshes and lead to a comparatively smaller but full matrix. When the number of conductors and dielectric layers increase, the analysis procedure will also be too costly in terms of computing time and memory needs. Measured Equation of Invariance (MEI) [7] and its variety Geometry Independent MEI (GIMEI) [8, 9] combined the advantages of the above two classes of methods together and leads to a sparse matrix with small number of unknowns, however, when problem become very complex, the computation resources it used are still quite considerable.

Until now, several commercial and/or public domain tools such as TMA's Raphael (based on Finite Difference Method (FDM), Ansoft's SPICELINK (based on Finite Element Method (FEM) and MIT's FastCap (based on multipole accelerated Boundary Element Method (BEM) are available to calculate the capacitances of various interconnects. It is well known that most VLSI interconnects have stratified structures and every layer is homogeneous along the direction perpendicular to the interfaces of the layers (denoted as z-direction). However, it seems that the tools mentioned above have neglected this fact. In this paper, we present a new capacitance extraction method named Dimension Reduction Technique (DRT) to take full advantage of this fact. According to the method of separation of variables, the 3D Laplace equation defined in each layer can be reduced to a 2D Helmholtz equation defined on the cross section of the layer because the layer is homogeneous along the z-direction. Therefore, original 3D problem is converted into a series of cascading 2D prob-

lems. Each 2D problem can be solved separately, thus we can choose the most efficient method for each problem according to the arrangement of the conductors. More importantly, it is very easy to obtain the analytical solutions of 2D problems in many layers such as the pure dielectric layers and the layers with parallel signal lines. Therefore, the domain that has to be analyzed numerically is reduced dramatically. This leads to the dramatic reduction of the computing time and memory needs. We have used the DRT to extract the capacitances of multilayered and multiconductor cross-overs, bends, via with signal lines and open-end. The results are in good agreement with those of SPICELINK and FastCap, but the computing time and memory size used by DRT are several even tens times less than those used by SPICELINK and FastCap. In addition, these examples show that the DRT has following attractive features: 1)The computing time and memory needs are unrelated to the ratio between the thickness of dielectric layers, which means we need not to pay additional efforts for an interconnect with both very thin and very thick layers. But it will be very costly to use FDM and FEM to extract the capacitances of this kind of interconnects: 2)Since the 2D problems in some layers can be solved analytically, the computing time and memory needs only increase slightly when the sizes of conductors increase. However, the computing time and memory used by BEM will increase greatly if the same thing happens; 3)The tedious task of 3D mesh generation is avoided, only 2D mesh generation is necessary if the 2D problems in some layers have to be solved numerically.

2 Principle of DRT

Up to now, the effective frequency range of the signal in VLSI system is still within 10 GHz. Therefore, the quasi-TEM assumption is valid. A simple example of interconnect layout is shown in Fig. 1. According to quasi-TEM assumption, the planes, which are far enough from the discontinuities in Fig. 1 and normal or parallel to the axis of the signal lines, can be replaced by magnetic walls (M.W.). Therefore, we can decompose the whole interconnect system into a lot of simple cells with magnetic walls and analyze each cell separately. These cells can be classified into a limited number of typical structures, such as those shown in Fig. 2.

We will use a typical 3D multilayer and multiconductor interconnect structure as shown in Fig. 3 to illustrate the principle of the DRT. Along the interfaces of dielectric layers, the whole structure is cut into slices. In the ith slice, the potential function ϕ^i satisfies the 3D Laplace equation

$$\frac{\partial^2 \phi^i}{\partial x^2} + \frac{\partial^2 \phi^i}{\partial y^2} + \frac{\partial^2 \phi^i}{\partial z^2} = 0 \qquad (1)$$

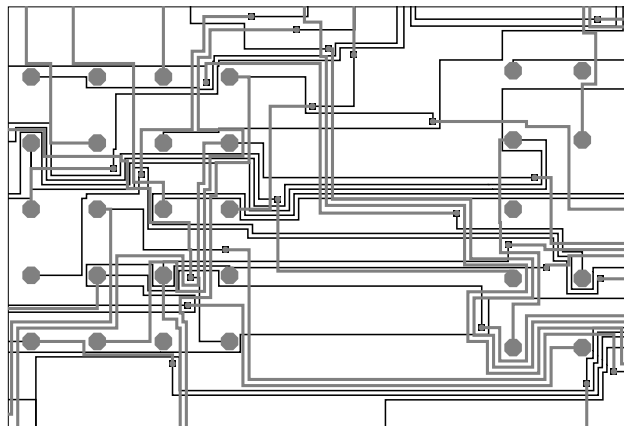From Fig. 3 it is obviously that each slice is homoge-
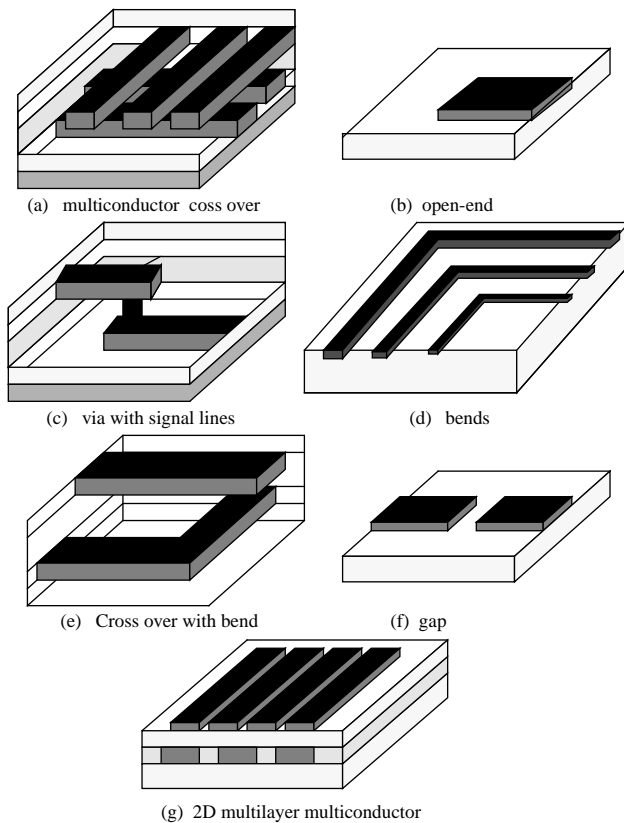

Figure 1: An example of layout

(a) multiconductor coss over

(b) open-end

(c) via with signal lines

(d) bends

(e) Cross over with bend

(f) gap

(g) 2D multilayer multiconductor
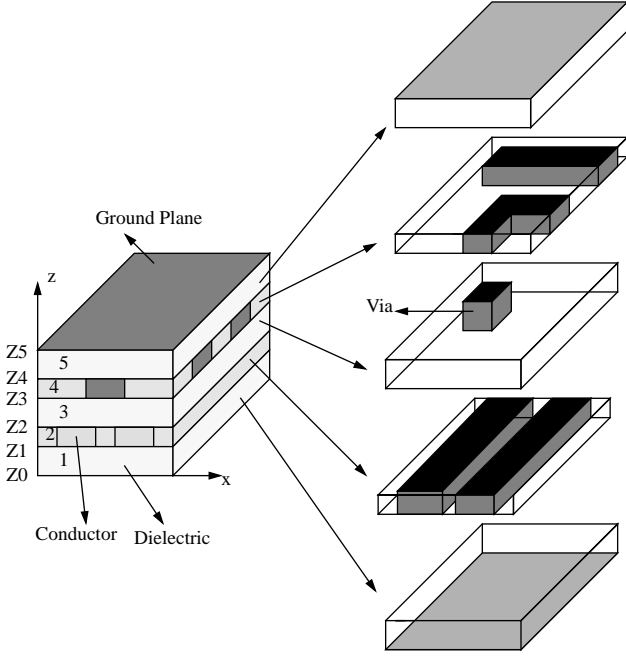
Figure 2: Some typical interconnect structures

Figure 3: A 3D interconnect and its slices

neous along z-direction. It should be noted that every slice is surrounded by magnetic walls. Thus the boundary conditions can be expressed as the following forms

$$\phi^i(x,y,z) = V_c^j \quad Z_{i-1} \le z \le Z_i, \quad (x,y) \in \Gamma_c^j \qquad (2)$$

$$\frac{\partial \phi^i(x,y,z)}{\partial n} = 0 \quad Z_{i-1} \le z \le Z_i, \quad (x,y) \in \Gamma_M \qquad (3)$$

$$\begin{cases} \phi^i = \phi^{i+1} \\ \varepsilon_i \frac{\partial \phi^i}{\partial z} = \varepsilon_{i+1} \frac{\partial \phi^{i+1}}{\partial z} \end{cases} \quad z = Z_i \qquad (4)$$

$$\phi^1(x,y,Z_0) = 0, \quad \phi^5(x,y,Z_5) = 0 \qquad (5)$$

where V_c^j refers to the voltage on the jth conductor, and n is the unit vector normal to the magnetic walls. Γ_c^j refers to the sides of the jth conductor, Γ_M refers to the magnetic walls. Eq. 2 will be invalid if the slice is a pure dielectric layer. Denote $W^i(x,y,V_c^j)$ as a linear function of x,y and V_c^j, let

$$\phi^i = \psi^i + W^i(x,y,V_c^j) \qquad (6)$$

If there exists such a function $W^i(x,y,V_c^j)$ to let function $\psi^i(x,y,z)$ satisfies

$$\psi^i(x,y,z) = 0 \quad Z_{i-1} \le z \le Z_i, \quad (x,y) \in \Gamma_c^j \qquad (7)$$

$$\frac{\partial \psi^i(x,y,z)}{\partial n} = 0 \quad Z_{i-1} \le z \le Z_i, \quad (x,y) \in \Gamma_M \qquad (8)$$

and Laplace equation 1, then from the method of separation of variables, the general solution of $\psi(x,y,z)$ is

$$\psi^i = \sum_{m=1} T_m^i(x,y)L_m^i(z) \qquad (9)$$

where $T_M^i(x,y)$ and $L_m^i(z)$ satisfy the following equations respectively

$$\frac{\partial^2 T_m^i}{\partial x^2} + \frac{\partial^2 T_m^i}{\partial y^2} + (\alpha_m^i)^2 T_m^i = 0 \qquad (10)$$

$$\begin{cases} \frac{\partial T_m^i}{\partial n} = 0 & (x,y) \in \Gamma_m \\ T_m^i = 0 & (x,y) \in \Gamma_c^j \end{cases} \qquad (11)$$

$$\frac{\partial^2 L_m^i}{\partial z^2} - (\alpha_m^i)^2 L_m^i = 0 \qquad (12)$$

The solution of Eq. 10 and 11 is called mode functions. The general solution of Eq. 12 is

$$L_m^i(z) = \begin{cases} A_m^i ch(\alpha_m^i z) + B_m^i sh(\alpha_m^i z) & \alpha_m^i \ne 0 \\ A_0^i z + B_0^i & \alpha_m^i = 0 \end{cases} \qquad (13)$$

where A_m^i and B_m^i are the undetermined coefficients. Substituting the mode functions, 6, 9 and 13 into 4 and 5, and making the inner product of each side of Eq. 4 with the mode functions, we can obtain a system of linear equation about A_m^i and B_m^i by utilizing the orthogonal property of mode functions. The potential functions in every slice and then the capacitance matrix can be readily retrieved from the solutions of these equations.

Therefore, the crux of the whole problem has become how to efficiently solve Helmholtz equation 10 with boundary conditions 11. In pure dielectric layer, such as the first and the fifth layer in Fig. 3, the mode functions and eigenvalues have the analytical expressions as

$$T_m^i(x,y) = cos\frac{(p-1)\pi x}{a}cos\frac{(q-1)\pi y}{b}, \quad i = 1,\ldots,5 \qquad (14)$$

$$\alpha_m^i = \pi \sqrt{(\frac{p-1}{a})^2 + (\frac{q-1}{b})^2} \qquad (15)$$

where $p = 1,2,\ldots,NM_x, q = 1,2,\ldots,NM_y, m = p + (q-1)*NM_x$, NM_x and NM_y are the truncated numbers of the mode functions along x and y direction, a and b are the distance between the magnetic walls along x and y direction, respectively. For the slice with irregular conductors (such as the fourth layer in Fig. 3), we will choose suitable numerical methods, such as the FD methods, to solve Eq. 10 and 11. The discretized form of Eq. 10 can be reduced to the following eigenvalue equation

$$[S]\bar{T} = \lambda\bar{T} \qquad (16)$$

where $\lambda = (\alpha_m^i)^2$ is the eigenvalue, $\bar{T}$ is the eigenvector consisting of the potential value at each mesh node, and $[S]$ is a sparse matrix resulted from the FD equations at each mesh node. This equation can be solved by some standard subroutines, such as Lanczos method. And the general solution of potential functions can be expressed as Eq. 9. The field matching process is almost the same as that of continuous mode functions.

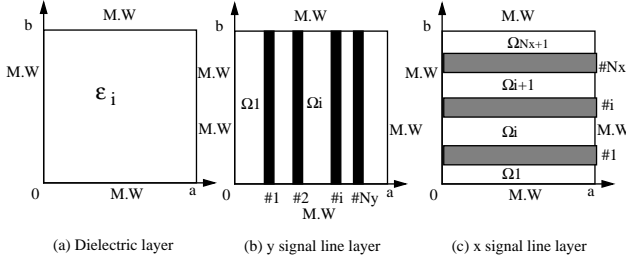In summary, the DRT consists of four steps: 1)Partitioning the complex interconnects into simple cells with

Figure 4: Cross section of typical layers of cross-overs

magnetic walls; 2)Along the interfaces of the dielectric layers, cutting the stratified structure of each cell into slices; 3)Finding the function $W^i(x, y, V_c^j)$ in Eq. 6, following the well-known method of separation of the variables, reducing the 3D Laplace equation (1) into 2D Helmholtz equation (6) and solving the Helmholtz equation in the cross section of every slice separately; 4)Matching the potential of each slice at the interfaces and solve the linear matrix equation about the unknown coefficients. The field matching process is the same as that of the mode matching technique [10], so we will omit the details of this step. The first and the second step are fixed and can be easily implemented for all kinds of structures, while the third and fourth step may need some more explanations. In the next section we will present further details about them.

3   Application of DRT

In this section, we will use the DRT to analyze several typical interconnect structures shown in Fig. 2. Since these structures are surrounded by magnetic walls, we only need to perform the second, the third and the fourth step mentioned in section 2. All relevant programs were run on a Sun Sparc 20 workstation.

A. Multiconductor crossover in multilayered dielectric media

   The structure of the multiconductor crossover is shown in Fig. 2(a). Based upon the DRT concept, the structure is cut into slices. There are three kinds of slices: pure dielectric layers, layer with x direction signal lines and layer with y direction signal lines. Their cross sections are shown in Fig. 4, where Nx and Ny are the number of the signal lines along x and y direction respectively.

   The function $W^i(x, y, V_c^j)$ in Eq. 6 can be easily obtained. For the layer with x direction signal lines, it is

$$W^i(y, V_x^j) = \begin{cases} V_x^1 & \Omega_1 \\ \frac{y - y_{j,2}}{SX_j}(V_x^j - V_x^{j-1}) + V_x^{j-1} & \Omega_j \\ V_x^{N_x} & \Omega_{N_x+1} \end{cases} \tag{17}$$

where V_x^j is the voltage on the jth signal line, SX_j is the

distance between jth and $(j-1)$th line. For the layer with y direction signal lines, $W^i(x, y, V_c^j)$ takes the similar form.

   The mode functions and eigenvalues in every layer can then be expressed analytically. For the pure dielectric layers, they are Eq. 14. For the layer with x direction signal lines, they are

$$T_m^{k,i}(x, y) = cos(\frac{(p-1)\pi x}{a})g_p^i(y) \quad i = 1, \ldots, N_x + 1 \tag{18}$$

$$g_q^i(y) = \begin{cases} cos\frac{(q-0.5)\pi y}{y_{1,1}} & i = 1 \\ sin\frac{q\pi(y-y_{i-1,2})}{SX_i} & 2 \le i \le N_x \\ cos\frac{(q-0.5)\pi(y-b)}{b-y_{N_x,2}} & i = N_x + 1 \end{cases} \tag{19}$$

$$\alpha_m^{k,i} = \begin{cases} \pi\sqrt{(\frac{p-1}{a})^2 + (\frac{q-0.5}{y_{1,1}})^2} & i = 1 \\ \pi\sqrt{(\frac{p-1}{a})^2 + (\frac{q}{SX_i})^2} & 2 \le i \le N_x \\ \pi\sqrt{(\frac{p-1}{a})^2 + (\frac{q-0.5}{b-y_{N_x,2}})^2} & i = N_x + 1 \end{cases} \tag{20}$$

where $p = 1, 2, \ldots, NM_x, q = 1, 2, \ldots, NM_y^i, m = p + (q-1)*NM_x + \sum_{j=1}^{i-1} NM_x NM_y^i$, NM_x and NM_y are the truncated numbers of the mode functions along x and y direction in the domain Ω_1 shown in Fig. 4(c), k is the sequence number of the layer with x direction signal lines. Exchanging x and y, a and b, we can obtain the mode functions and eigenvalues in the layer with the y direction signal lines. Substituting the mode functions of every layer into Eq. 9 and matching the potential at the interfaces, we can obtain the capacitance matrix.

   The algorithm can be used to analyze crossover with arbitrary number of lines embedded in arbitrary number of dielectric layers. The crossover chosen for analysis is modeled as: the number of x and y direction lines are 2, the width, thickness and the length of each line are $1\mu m$, $1\mu m$ and $8\mu m$ respectively, the number of dielectric layers is 5, the relative dielectric constant and thickness of each layer is 3.9 and $1\mu m$, respectively, the crossover is separated from the top and bottom planes by $1\mu m$. The truncated number of mode functions in every layer is 21×21. The capacitance matrix in $fF(10^{-15}F)$ is

$$[C] = \begin{bmatrix} 1.536 & -0.407 & -0.173 & -0.173 \\ -0.407 & 1.535 & -0.173 & -0.173 \\ -0.173 & -0.173 & 1.535 & -0.407 \\ -0.173 & -0.173 & -0.407 & 1.535 \end{bmatrix} \tag{21}$$

The computing time is 87 seconds and memory need is 2MB while Ansoft SPICELINK's results are (in fF)

$$[C] = \begin{bmatrix} 1.53 & -0.398 & -0.188 & -0.196 \\ -0.398 & 1.52 & -0.187 & -0.195 \\ -0.188 & -0.187 & 1.47 & -0.373 \\ -0.196 & -0.195 & -0.373 & 1.51 \end{bmatrix} \tag{22}$$

with 881 seconds CPU time and 58.551MB memory needs.

B. Via with signal lines in multilayered dielectric media

(a) top signal line   (b) bottom signal line   (c) via
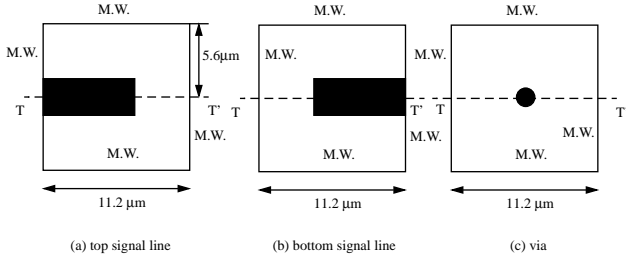
Figure 5: Cross section of typical layers of a via

M1	M2	M3	Cap. in fF	Time in sec.	Memory in MB
40	40	49	1.094	50	0.707
45	45	49	1.095	51	0.711
50	50	49	1.070	53	0.715

Table 1: Results of via structure

The structure of a via with signal lines is shown in Fig. 2(c). The cross sections of three consecutive slices with conductor are shown in Fig. 5.

For these three slices, the function in Eq. 6 is also Eq. 23, so the DRT can be applicable to every slice of the whole structure. Using Eq. 14 for pure dielectric layer and numerically-solved mode function of slices in Fig. 5, after the field matching step, the capacitance value can be obtained. The algorithm can be used for the rectangular via as well as the cases that the signal lines take other shapes (such as a straight line with pad on the top of the via).

We will use the via in Fig. 2(c) as the numerical example. The whole structure can be cut into five slices and is symmetric to the plane T-T' shown in Fig. 5, so we only have to analyze half of the structure. The top and bottom ground planes are separated from the via by the dielectric layer whose thickness and relative dielectric constant are $2\mu m$ and 3.9. The length, width and thickness of the two signal lines are $6.4\mu m$, $1.6\mu m$ and $1\mu m$ respectively. The radius and height of the via is $0.2\mu m$ and $3\mu m$ respectively. The distance between the center of the via and the edge of the signal lines is $0.8\mu m$. The relative dielectric constant of other three layers is 2.45. The capacitance, computing time and memory size are shown in Table 1, where M1, M2 and M3 refer to the truncated number of mode functions in the slices with top and bottom signal line, the slice with the via and the pure dielectric slices respectively.

The capacitance calculated by Ansoft's SPICELINK is $1.124fF$, the computing time is 405 seconds, the memory needs is 48.197MB.

C. Openend in multilayered dielectric media

The structure of an open-end is shown in Fig. 2(b). The cross section of the slice with the conductor is shown in Fig. 6(a). Since it is symmetrical to the plane T-T', we
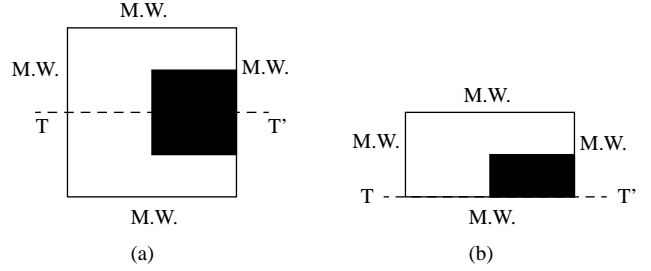

(a)   (b)

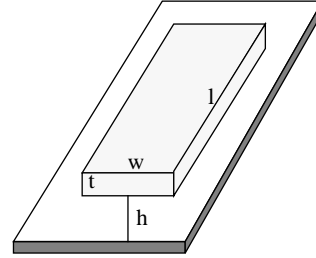Figure 6: Cross section of the conductor layer of openend

Figure 7: A conductor over a ground plane

can replace the plane with a magnetic wall and analyze half of the structure.

For the slice with the conductor, the function in Eq. 6 is

$$W^i(x, y, V_c^j) = 1 \qquad (23)$$

Eq. 10 is defined on an irregular L-shape domain in Fig. 6(b), so we use the numerical method, such as FD method, to obtain the discrete mode functions. The mode functions of the pure dielectric slices are still Eq. 14. Substituting the mode functions of every slice and Eq. 13 into 9 and taking the fourth step mentioned in section 2, we can obtain the capacitance.

To test the algorithm, we have used it to analyze a simple structure shown in Fig. 7. The width and thickness of the conductor are $1\mu m$ and the length is regarded as variable. The thickness and the relative dielectric constant of the dielectric layer above the ground plane is $1\mu m$ and 3.9 respectively. The structure has two symmetric planes, we only need to analyze a quarter of it which is exactly the same as that shown in Fig. 6(b), thus the algorithm mentioned above can be used directly. The capacitance of the structure in Fig. 7 is four times of the capacitance of the structure in Fig. 6(b). The computed results, CPU time and memory needs are listed in Table 2. The table shows that the DRT is several times faster than the FastCap but uses much less memory.

We have also adopted DRT to multiconductor bends in Fig. 2(d) and some other combined structures. Numerical results are in good agreement with Ansoft's and FastCap's data with orders of magnitude reduction of CPU time and memory usage. Using similar procedures as shown above,

Conductor length in μm	DRT in $10^{-3}pF$	FastCap in $10^{-3}pF$	Closed-form formulae [11] in $10^{-3}pF$	DRT CPU time in sec.	FastCap time in sec.	DRT memory in MB	FastCap memory in MB
2	0.415	0.422	0.414	0.8	3.53	0.45	4
4	0.650	0.674	0.659	0.8	11.08	0.45	4.7
6	0.873	0.925	0.904	0.8	7.69	0.45	2.8
8	1.110	1.170	1.149	1.2	8.24	0.47	7.13
10	1.357	1.412	1.195	1.2	7.64	0.47	7
12	1.568	1.654	1.640	1.2	29.45	0.47	11.7

Table 2: Comparison of capacitance, CPU time, and memory usage

analyzing other structures such as the rest in Fig. 2 is straightforward.

4   Conclusions and Discussions

In this paper, we present a new method named dimension reduction technique (DRT) to extract the capacitance matrix of the 3D interconnects in VLSI circuits. The method is very versatile and efficient. Based upon the basic idea of DRT, we can set up an accurate and fast field solver library for the typical interconnect structures. By using this library, accurate closed-form formulae or data base of the electrical parameter of these typical interconnect structures can be easily obtained.

The most fundamental assumption in the present paper is that the method of separate of variables are valid. This requires that the interfaces of each layer is parallel to each other and the surfaces of conductors are either parallel or orthogonal to those interfaces. Unfortunately, some kinds of packages and bonds do not meet these requirements. Therefore, the DRT needs some improvement to analyze these structures. One obvious solution is using straight segments that parallel or orthogonal to the interfaces to approximate the original structure. This of course will introduce some errors. More research work is being done on this aspect.

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