A novel double-trench LVTSCR used in the ESD protection of a RFIC*

Li Li(李立)† and Liu Hongxia(刘红侠)

Key Laboratory of the Ministry of Education for Wide Band Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an 710071, China

Abstract: A low-voltage triggering silicon-controlled rectifier (LVTSCR), for its high efficiency and low parasitic parameters, has many advantages in ESD protection, especially in ultra-deep sub-micron (UDSM) IC and high frequency applications. In this paper, the impact factors of the snapback characteristics of a LVTSCR and the configuring modes are analyzed and evaluated in detail. These parameters include anode series resistance, gate voltage, structure and size of devices. In addition, a double-trench LVTSCR is presented that can increase the hold-on voltage effectively and offers easy adjustment. Also, its snapback characteristics can obey the ESD design window rule very well. The strategy of ESD protection in a RFIC using a LVTSCR is discussed at the end of the paper.

Key words: UDSM; LVTSCR; RFIC; ESD design window
DOI: 10.1088/1674-4926/32/10/104005 **EEACC:** 2570

1. Introduction

With continuous scaling down of feature sizes, decreasing gate oxide thickness in ICs, and increasing work frequency, the performance of ESD protection and compatibility issues becomes more and more prominent. When ESD happens, the main discharging devices carry much current and occupy a large chip area, which increases the cost of the chip and causes the deterioration of high-frequency parameters[1]. Because of its high discharging capability per unit area and easy adjustment of switch parameters, the LVTSCR is playing a very important role in ESD protection circuits.

As the turn-on resistance (R_{on}) of a LVTSCR is low and the power dissipation is small, it has good ESD robustness and high discharging efficiency. Therefore, an LVTSCR has good advantages in UDSM and high frequency applications. Figure 1 shows a cross-section of a LVTSCR. Different from BJT or ggNMOS, an LVTSCR is a double-injected device that has two highly-doped emitters, an anode and a cathode. After being turned on, the N well-P substrate junction can be considered as a recombination center, and the holes and electrons are injected from the two-side emitters and are recombined. Because of the positive feedback of NPN and PNP, the collector current of each transistor becomes the base input of the other transistors. Thus, the LVTSCR has a better turn-on mechanism than ggNMOS of single inject mode, and its R_{on} is small[2].

Snapback in a LVTSCR is due to positive feedback triggered by the substrate current of the NMOS[3, 9]. For an effective ESD protection structure, the turn-on voltage (V_T) must be lower than the breakdown voltage of the gate oxide of CMOS, and the hold-on voltage (V_H) must be higher than the normal operating voltage of the circuit, which is called the ESD design window. There are many different triggering mechanisms for ESD protection structures, including the displacement current caused by significant variation dV/dt and the substantial fluctuation in incoming current signal dI/dt, which may be coupled into ESD devices through the parasitic capacitor and inductor, leading to undesired early turn-on of ESD protection structures. Such accidental triggering is highly likely in super-GHz RF applications considering the fact that the ESD pulse rise time t_r is about 10 ns in HBM mode and $t_r \leqslant 200$ ps in CDM mode. There are two solutions to avoid the LVTSCR being accidentally triggered by the noise pulses when the circuit is in the normal operating condition: one is to increase the trigger current and the other is to increase the hold-on voltage[4].

2. Impact of anode series resistance (R_s) on snapback

By adding anode series resistance in the LVTSCR, the voltage drop across R_s will be caused by ESD current, which can increase the hold-on voltage between the terminals of ESD protection after being turned on[5]. R_s can cause increased power dissipation and decreased ESD robustness. In order to

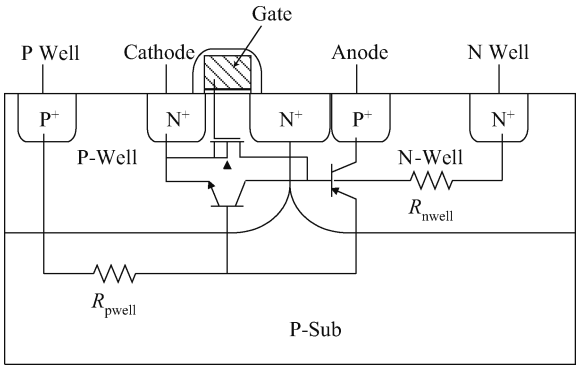

Fig. 1. Cross-section of an LVTSCR.

* Project supported by the National Natural Science Foundation of China (Nos. 60976068, 61076097) and the National Defense Foundation of China (No. 413080401).
† Corresponding author. Email: 332808552@qq.com
Received 8 April 2011, revised manuscript received 19 May 2011

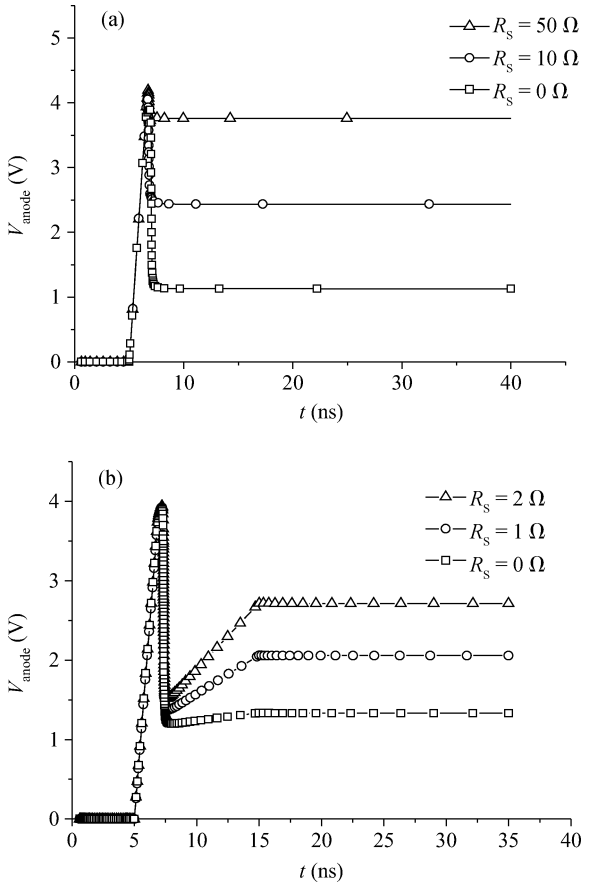

Fig. 2. Transient characteristics of the LVTSCR (with R_S) under different TLP stresses. (a) Low intensity. (b) High intensity.

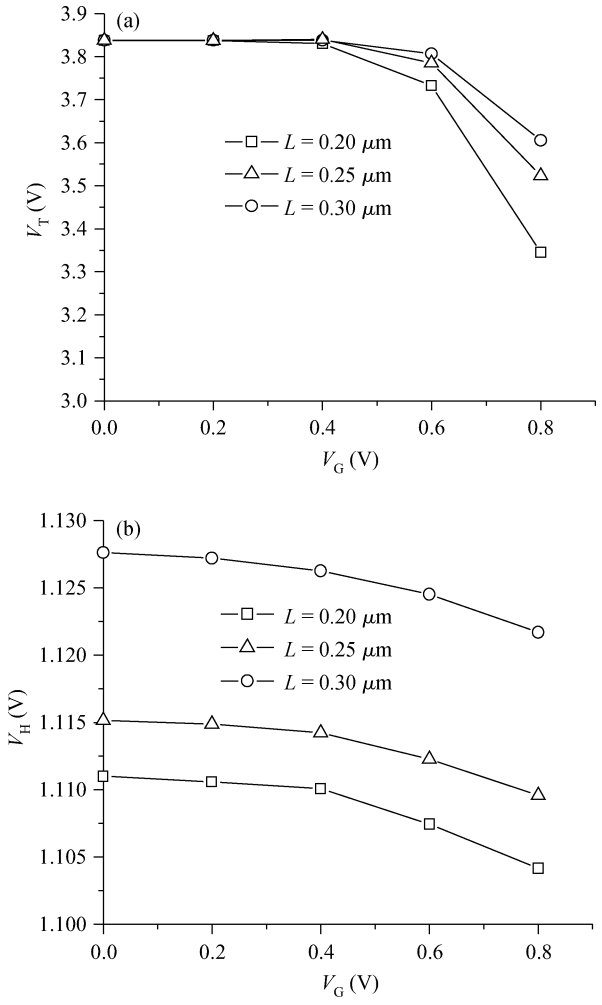

Fig. 3. (a) V_T–V_G and (b) V_H–V_G relations of the LVTSCR for different channel lengths.

solve this problem, R_s can be designed to be large, such as by using a large sectional area and controlling the value by adjusting its length. It can improve the heat dissipation conditions effectively. The controlled capability of R_s to V_H will be discussed in the following sections.

In this paper, the numeric simulation software SILVACO is used. For the LVTSCR of a 90 nm process with a channel length $L = 0.2$ μm, and channel width $W = 100$ μm, TLP testing is performed. For a pulse with a certain rise time, the greater the intensity, the greater the ESD current and the voltage across R_s. Large R_s can cause the hold-on voltage V_H to be greater than the turn-on voltage V_T, and the protection circuit cannot work. Small R_s can cause a small voltage drop, and V_H is less than the circuit's normal operating voltage VDD. It does not obey the ESD design window. Figure 2 shows the transient characteristics of the LVTSCR under different TLP stresses.

In order to increase V_H, large R_s is required. However, in order to make the protection valid ($V_H < V_T$), small R_s is needed. Anyway, the effect of increasing V_H by adjusting R_s is limited, especially for high level protection (> 4 kV). The clamp voltage of the LVTSCR with anode series resistance is strongly dependent on the intensity of the ESD stress, the value of resistance should be precise and the range is narrow. However, this configuration is simple, and the parasitic parameters are less, which is suitable for input/output protection of the RFIC.

3. Impact of gate voltage (V_G) on snapback

For a LVTSCR structure, the channel doping of parasitic NMOS is low, around 10^{17} cm^{-3}, and the resistivity of this region is high, and it can be taken to increase the voltage drop across the LVTSCR by increasing the channel length L. V_T can be adjusted by V_G. Now we analyze the structure with the LVTSCR, $L = 0.20$, 0.25 and 0.30 μm, $V_G = 0$, 0.2, 0.4, 0.6 and 0.8 V.

Figures 3 and 4 show the relationships of V_T–V_G and V_H–V_G of the LVTSCR for different channel lengths, respectively. For high V_G, V_T is obviously different with increasing L. The greater L, the higher V_T. This means that the adjusting ability of V_G is small. V_H increases slightly with increasing L. When $V_G = 0$ V, L increases from 0.20 to 0.30 μm, and V_H only increases from 1.111 to 1.128 V. V_H decreases with increasing V_G. Increasing V_H by increasing the channel length of the LVTSCR is very limited.

4. Impact of structure and size of the LVTSCR on snapback

Increasing the distance from the anode to the border of the N-well–P-substrate means prolonging the path of the turn-on

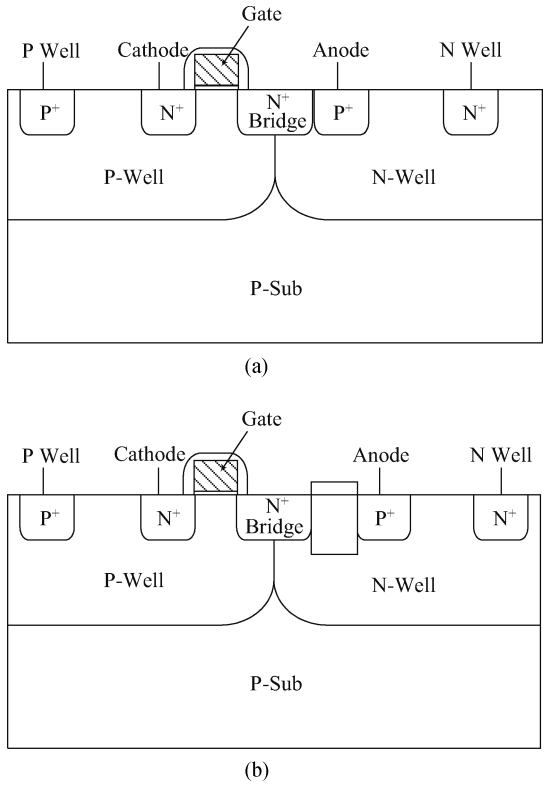

Fig. 4. Different LVTSCR structures. (a) Normal LVTSCR structure. (b) A LVTSCR with a single trench.

current, and it can increase turn-on resistance R_{on} and hold-on voltage V_H. V_T is the sum of the reverse breakdown voltage of the N-well–P-substrate (V_{BR}) and the build-in potential of the two emitter junctions. The N-well–P-substrate of the LVTSCR is highly doped at one-side, and avalanche is the dominant mechanism of breakdown, as shown here,

$$V_{BR} = \frac{\varepsilon_0 \varepsilon_{Si} E_C}{2q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right), \quad (1)$$

where V_{BR} is the reverse breakdown voltage of the PN junction, N_A and N_D are the impurity concentration for accepters and donors, and E_C is the critical electric field. For medially-doped silicon, E_C is around 4×10^5 V/cm[6, 10]. This equation shows that the breakdown voltage of a one-side step junction is determined by the impurity concentration of the lightly doped side, and it is in inverse proportion to the concentration. Therefore, increasing the distance from the anode to the border of the N well-P substrate does not influence V_T.

However, the effect of increasing V_H only by increasing the distance from the anode to the border of the N-well–P-substrate is limited, and it occupies a large chip area. In fact, increasing V_H is current-limitation. If an isolation trench was made between the anode and the N^+ bridge region, the effect would be better than increasing the distance. It does not occupy large area. In this paper, both the width and the depth of the trench are 0.2 μm, as shown in Fig. 4.

Figure 5 shows the snapback characteristics of the LVTSCR with and without trench between the anode and the N^+ bridge. V_T is almost the same after adding an isolation trench, while V_H increases from 1.126 to 1.270 V. However,

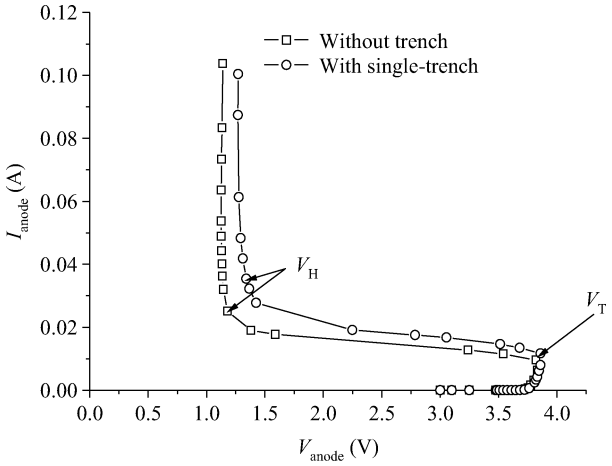

Fig. 5. Snapback characteristics of the LVTSCR with and without a trench between the anode and the N^+ bridge.

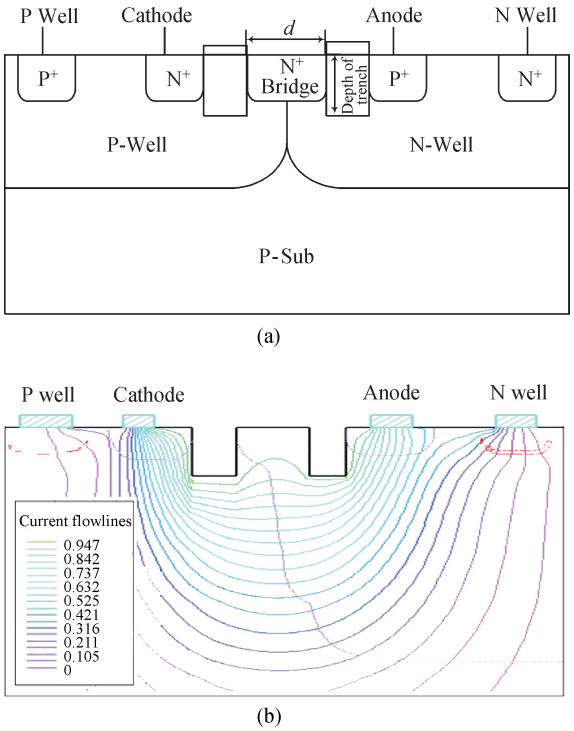

Fig. 6. (a) LVTSCR with double trenches. (b) Current distribution after turn-on.

the effect of current-limitation with a single trench is poor, and the regulation of V_H is still difficult to fit the acquirements. Since the structure has a low turn-on voltage, which can also be changed by impurity concentration, so we give up adjusting V_T by changing the gate voltage and replace the gate with another isolation trench to restrict the current. The size of the trench is 0.20×0.20 μm^2, as shown in Fig. 6(a).

For a LVTSCR with double trenches, most current still goes through the highly-doped N^+ bridge region after being turned on, as shown in Fig. 6(b). While the corners of the trench can restrict the current effectively and increase V_H from 1.126 to 1.420 V, the trigger current I_T increases slightly and the turn-on voltage V_T is almost the same (3.877, 3.884, 3.867 V), as shown in Fig. 7. Thus, the effect of increasing the hold-on volt-

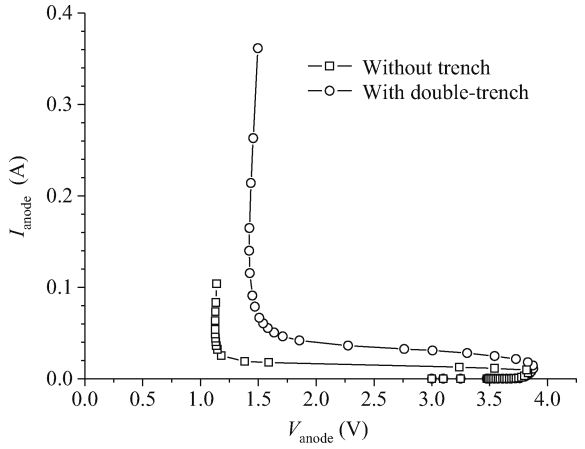

Fig. 7. Snapback characteristics of the LVTSCR with and without double trenches.

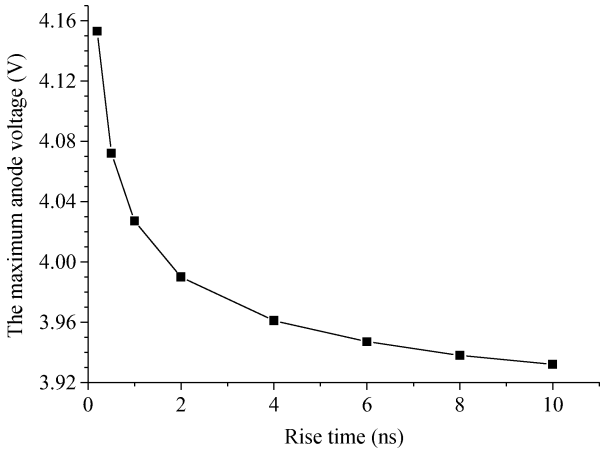

Fig. 9. Relationship between the TLP rise time and the maximum anode voltage.

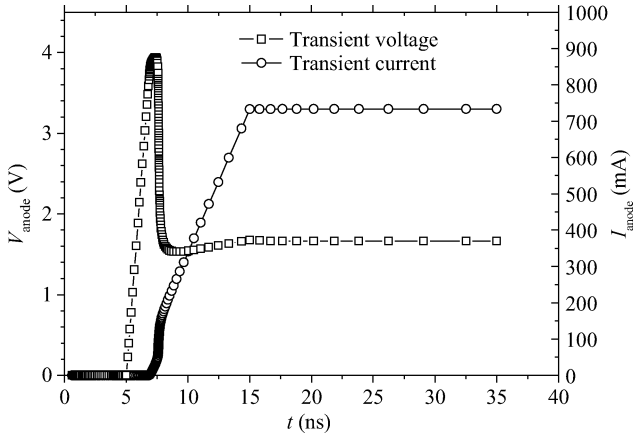

Fig. 8. Transient characteristics of the LVTSCR with double trenches under TLP stress.

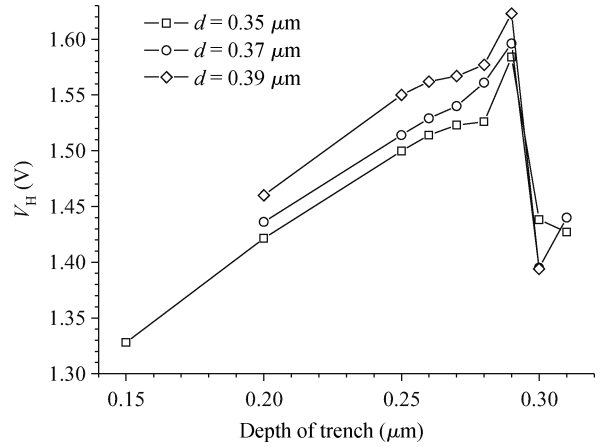

Fig. 10. Impact of the depth of trench and the width of the N^+ bridge (d) on V_H of the LVTSCR with double trenches.

age of a double trench structure is obvious, and we can get a proper V_H by adjusting the depths of the two trenches.

Figure 8 shows the transient characteristics of the LVTSCR with double trenches under TLP stress. When the rise time is 10ns, the voltage of 3.932 V is built up at the anode for the current level of 733 mA. Thus, the maximum anode voltage not only depends on the turn-on voltage of the LVTSCR but it also depends on the rise time of the ESD signal.

Generally speaking, the set-up time of the ESD is about 0.2–20 ns. Considering the impact of the TLP rise time on the maximum anode voltage, we set the rise time of the signal as 0.2–10 ns. Figure 9 shows the relationship between the TLP rise time and the maximum anode voltage. For the same pulse amplitude, the maximum anode voltage increases with decreasing rise time. It is 3.932 V when the rise time is 10 ns. It increases to 4.153 V when the rise time is 0.2 ns. It is caused by the delay effect of the N-well–P-substrate junction capacitance. The shorter the TLP rise time, the more significant the delay effect becomes. The delay effect causes charge accumulation near the junction. The maximum anode voltage increases with decreasing rise time.

The depth of trench impacts the hold-on voltage greatly, because the vertical size will significantly affect the path of carriers, while the horizontal size affects the path much less. When carriers pass through the N^+ bridge region, they will be restricted around the corners due to the existence of double trenches, and they will go through a path of low resistance. When the depth of trench is shallow, carriers may choose the path through the highly-doped N^+ bridge region, and the isolation trench increases the paths that are lightly-doped before and after the N^+ bridge. However, if the trench is very deep, the highly-doped N^+ bridge will be far away from the bottom of the trench, and the carriers will choose the path through the lightly-doped region directly because of the total resistance is low. So there is a critical value of trench depth that influences the hold-on voltage greatly. When the depth of trench is greater than the critical value, the turn-on resistance R_{on} will not increase with increasing depth, the effect of current-limitation is restrained, and the hold-on voltage will not continue to increase and begin to fall. Figure 9 shows the relation between the depth of trench and the hold-on voltage for different N^+ bridge widths d. When d is 0.35 μm and the depth of trench is 0.29 μm, V_H reaches its maximum value of 1.584 V.

In addition, the width of the N^+ bridge region d will influence the hold-on voltage significantly. Figure 10 shows that the hold-on voltage increases with increasing d, and the maxi-

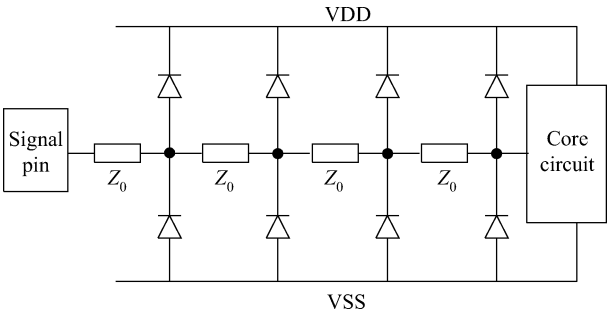

Fig. 11. The distributed ESD protection design with diodes.

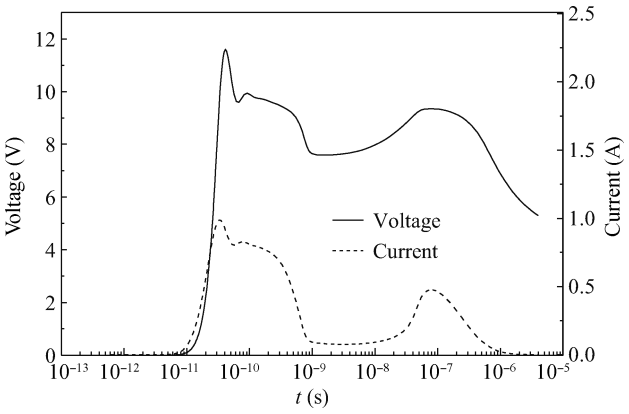

Fig. 12. HBM simulation results of two-stage LVTSCR protection.

mum values of V_H are 1.584, 1.596 and 1.623 V for $d = 0.35$, 0.37 and 0.39 μm.

5. ESD protection based on the LVTSCR in the RFIC

The basic principle for incorporating suitable on-chip ESD protection in a given circuit requires that the added ESD protection circuitry dose not degrade the performance of the circuit. In digital circuits, ESD protection commonly consists of large clamping devices (> 100 μm), e.g. diodes or ggNMOS structures, and it often has a current-limitation series resistor[7]. However, in RF designs, such a large device presents a big parasitic input capacitance and can severely degrade input matching. Thus, simultaneously achieving the RF performance and ESD robustness in state-of-the-art CMOS technologies is an issue.

In the RFIC, the input and output port are very sensitive to the changes in structure, e.g. an ESD protection circuit being induced. To achieve a well matching, low noise figure and high ESD protection level, distributed ESD protection is used[8], which includes the equally distributed structure and the unequally distributed structure, as shown in Fig. 11. The LVTSCR has a similar capacitance with the STI diode in equal size, and its performance is much better than the latter. STI diodes used to protect the input and output ports of the RFIC can be instead by LVTSCRs. Based on the two-stage LVTSCR protection, a human-body model simulation is implemented, the results of which are shown in Fig. 12. This shows that there is a fluctuation in the discharging voltage/current wave due to an inductor effect of the distributed protection structure, which is different from a single discharging device. Anyway, it does not have apparent influence on the protection level.

6. Conclusion

The LVTSCR was reported for on-chip ESD protection in CMOS IC over ten years ago. Such devices can be triggered by the overshooting or undershooting of noise pulses, which cause a latch-up danger when ICs are operated under normal conditions. In this work, several kinds of structure for LVTSCRs in ESD protection have been analyzed and evaluated, and their characteristics and application conditions have also been summarized. Based on a 90 nm process, a novel LVTSCR structure with double trenches was presented, which has a relatively high and easily adjustable hold-on voltage without changing other snapback parameters obviously. It can be used instead of STI diodes in input and output ports of the RFIC for ESD protection, which has relatively low parasitic capacitance and higher protection efficiency. Based on the LVTSCR, the protection strategy in high frequency applications was discussed.

References

[1] Wang A Z, Feng H G, Zhan R Y, et al. ESD protection design for RF integrated circuits: new challenges. IEEE Custom Integrated Circuits Conference, 2002, 22(1): 1

[2] Concannon A, Vashchenko V A, Beek M T, et al. A device level negative feedback in the emitter line of SCR structures as a method to realize latch-up free ESD protection. IEEE 41st Annual International Reliability Physics Symposium, 2003: 105

[3] Zhou P, Hajjar J J, Righter A W, et al. Modeling snapback of LVTSCR devices for ESD circuit simulation using advanced BJT and MOS models. EOS/ESD Symposium, 2007, 3A(3): 175

[4] Ker M D, Chang H H. How to safely apply the LVTSCR for CMOS whole-chip ESD protection without being accidentally triggered on. Electrical Overstress/Electrostatic Discharge Symposium Proceedings, 1998: 72

[5] Mergens M P J, Russ C C, Verhaege K G, et al. Speed optimized diode-triggered SCR (DTSCR) for RF ESD protection of ultra-sensitive IC nodes in advanced technologies. IEEE Trans Device Mater Reliab, 2005, 5(3): 532

[6] Arora N. MOSFET models for VLSI circuit simulation: theory and practice. New York: Springer-Verlag, Wien, 1993: 54

[7] Wang A Z H, Feng H G, Zhan R Y, et al. A review on RF ESD protection design. IEEE Trans Electron Devices, 2005, 52(7): 1304

[8] Ker M D, Kuo B J. ESD protection design for broadband RF circuits with decreasing-size distributed protection scheme. IEEE Radio Frequency Integrated Circuits Symposium, 2004: 383

[9] Wang X, Fan S Q, Zhao H, et al. Whole-chip ESD protection design for RF and AMS ICs. Tsinghua Science and Technology, 2010, 15(3): 265

[10] Brennan C J, Chang S, Woo M, et al. Implementation of diode and bipolar triggered SCRs for CDM robust ESD protection in 90 nm CMOS ASICs. Microelectron Reliab, 2007, 47: 1030