

Article

# A Novel Dry Selective Isotropic Atomic Layer Etching of SiGe for Manufacturing Vertical Nanowire Array with Diameter Less than 20 nm

Junjie Li <sup>1,2,\*</sup>, Yongliang Li <sup>1</sup> , Na Zhou <sup>1</sup>, Guilei Wang <sup>1,2,\*</sup> , Qingzhu Zhang <sup>1,3</sup>, Anyan Du <sup>1</sup>, Yongkui Zhang <sup>1</sup>, Jianfeng Gao <sup>1</sup>, Zhenzhen Kong <sup>1</sup>, Hongxiao Lin <sup>1</sup>, Jinjuan Xiang <sup>1</sup>, Chen Li <sup>1,2</sup>, Xiaogen Yin <sup>1,2</sup>, Yangyang Li <sup>1,2</sup>, Xiaolei Wang <sup>1</sup>, Hong Yang <sup>1</sup> , Xueli Ma <sup>1</sup>, Jianghao Han <sup>1</sup>, Jing Zhang <sup>4</sup>, Tairan Hu <sup>4</sup>, Tao Yang <sup>1</sup>, Junfeng Li <sup>1</sup>, Huaxiang Yin <sup>1,2</sup>, Huilong Zhu <sup>1,2</sup>, Wenwu Wang <sup>1,2,\*</sup> and Henry H. Radamson <sup>1,2,5</sup>

- <sup>1</sup> Key Laboratory of Microelectronics Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China; liyongliang@ime.ac.cn (Y.L.); zhouna@ime.ac.cn (N.Z.); zhangqingzhu@ime.ac.cn (Q.Z.); duanyan@ime.ac.cn (A.D.); zhangyongkui@ime.ac.cn (Y.Z.); gaojianfeng@ime.ac.cn (J.G.); kongzhenzhen@ime.ac.cn (Z.K.); linhongxiao@ime.ac.cn (H.L.); xiangjinjuan@ime.ac.cn (J.X.); lichen2017@ime.ac.cn (C.L.); yinxiaogen@ime.ac.cn (X.Y.); liyangyang@ime.ac.cn (Y.L.); wangxiaolei@ime.ac.cn (X.W.); yanghong@ime.ac.cn (H.Y.); maxueli@ime.ac.cn (X.M.); hanjianghao@ime.ac.cn (J.H.); tyang@ime.ac.cn (T.Y.); lijunfeng@ime.ac.cn (J.L.); yinhuaxiang@ime.ac.cn (H.Y.); zhuhuilong@ime.ac.cn (H.Z.); rad@ime.ac.cn (H.H.R.)
- <sup>2</sup> Microelectronics Institute, University of Chinese Academy of Sciences, Beijing 100049, China
- <sup>3</sup> State Key Laboratory of Advanced Materials for Smart Sensing, General Research Institute for Nonferrous Metals, Beijing 100088, China
- <sup>4</sup> College of Electronic and Information Engineering, North China University of Technology, Beijing 100144, China; zhangj@ncut.edu.cn (J.Z.); tairanhu1@gmail.com (T.H.)
- <sup>5</sup> Department of Electronics Design, Mid Sweden University, Holmgatan 10, 85170 Sundsvall, Sweden
- \* Correspondence: lijunjie@ime.ac.cn (J.L.); wangwenwu@ime.ac.cn (W.W.); wangguilei@ime.ac.cn (G.W.); Tel.: +86-010-8299-5508 (W.W.)

Received: 16 January 2020; Accepted: 3 February 2020; Published: 7 February 2020



**Abstract:** Semiconductor nanowires have great application prospects in field effect transistors and sensors. In this study, the process and challenges of manufacturing vertical SiGe/Si nanowire array by using the conventional lithography and novel dry atomic layer etching technology. The final results demonstrate that vertical nanowires with a diameter less than 20 nm can be obtained. The diameter of nanowires is adjustable with an accuracy error less than 0.3 nm. This technology provides a new way for advanced 3D transistors and sensors.

**Keywords:** vertical nanopillar; atomic layer etching; SiGe; field effect transistor; nano device; sensor material

## 1. Introduction

It has taken few decades to search for materials and device designs for different types of sensors and field-effect transistors. Until now, nanowires (NWs) have offered an excellent platform for gas and bio sensing due to their nano-scale size compatibility to molecule size [1,2]. One issue for this application is how to functionalize the surface of NWs to detect a specific gas molecule with good selectivity. In such case, NW transistors could be designed where the carrier transport through the channel is affected and signaled in response to “absorption of” or “interaction with” the gas molecules. For simplicity, these NW sensors are laterally formed on the oxide [3–7]. In these NW transistors,

a good Ohmic contacts with low contact resistance, high signal-to-noise, and a good isolation of NW contacts are the main issues.

For many sensor applications, Si-based materials have been widely used but recently different 2D crystals have also been demonstrated. In contrary to Si, SiGe alloys offer a better carrier transport property in presence of compressive strain [8–11].

For field-effect transistors, in order to reduce the short channel effect (SCE) and power consumption caused by device size shrinkage, lateral and vertical gate-all-around (GAA) field-effect transistors have become a trend to replace FinFet [12–14]. Therefore, the manufacturing of precise and controllable size nanowires or nanosheets has become an important technology. In addition, in order to obtain a larger drive current, the channel mobility should be improved. It is also a development trend to use higher mobility SiGe and Ge materials instead of silicon [15,16]. The diameter of nanowires or pillars significantly affects the performance of the device. For sensors, a small size diameter will raise sensitivity because of the higher surface-to-volume ratio [17,18]. For GAA transistors, a small channel diameter will improve gate control and reduce device leakage and power consumption [19,20]. In the conventional bottom-up vertical nanowire preparation method, the diameter of the nanowires is mainly controlled by advanced lithography technology [14,21]. Isotropic selective etching of SiGe is a top-down method to obtain nanowires or nanopillars, and its diameter is controlled by etching and does not depend entirely on photolithography [22]. However, how to accurately control the diameter of nanowires or pillars has become a challenging subject. The commonly used methods for the selective etching of SiGe include wet etching of a mixed solution of oxidant and acid [23–25], HCl gaseous reaction [26–28], and  $\text{CF}_4$  base gas remote plasma etching [29,30], but the control accuracy is not high enough. The recently reported method of alternating cycles of  $\text{O}_2$  and  $\text{NF}_3/\text{NH}_3/\text{O}_2$ , because the self-limitation in each cycle cannot be achieved, and the etching amount per cycle is close to 20 nm, so the etching accuracy is still not high enough [31].

In our previous work, the new  $\text{CF}_4/\text{O}_2/\text{He}$  reaction system without bias power plasma etching technology was studied, but its etching accuracy still needs to be improved because of its continuous etching characteristics [32]. Then, the method of  $\text{H}_2\text{O}_2$  and BOE alternate cycle self-selective etching of SiGe was studied, and the etching accuracy was remarkably improved. However, the surface tension of the wet solution and the capillary effect determine that its application in 3D high aspect ratio devices will be a big limitation in the future [22].

In this article, a novel SiGe vertical NW in Si/SiGe/Si structure has been proposed as a sensor structure and the work presents how to apply a dry atomic layer etching (ALE) method to form such structures. The alternating circulation based on  $\text{O}_2$  plasma self-limited oxidation and  $\text{CF}_4/\text{C}_4\text{F}_8$  self-limited selective etching was studied systematically. The profile of nanowires and nanopillars, the relationship between the diameter of nanowires/sheets, and the amount of etching and the number of self-limiting etching cycles were also studied by different types of characterizations. The microstructure after etching was studied by HRSEM (high-resolution scanning electron microscope), HRTEM (High-resolution transmission electron microscope) and EDS (energy dispersive spectrometer) as well as high-resolution x-ray diffraction (HRXRD) [33,34].

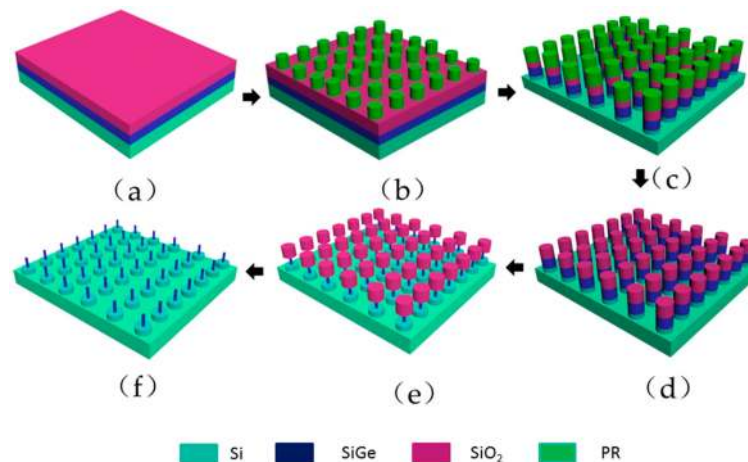
## 2. Materials and Methods

All the materials were performed on 8-inch (100) silicon wafers. The flow of nanopillar manufacture is shown in Figure 1.

Step 1: The film of 60 nm  $\text{Si}_{0.72}\text{Ge}_{0.28}$  was grown by using reduced pressure chemical vapor deposition (RPCVD) technique [35–37], and then a 60 nm-thick  $\text{SiO}_2$  is grown on the silicon-germanium by plasma enhanced chemical vapor deposition (PECVD).

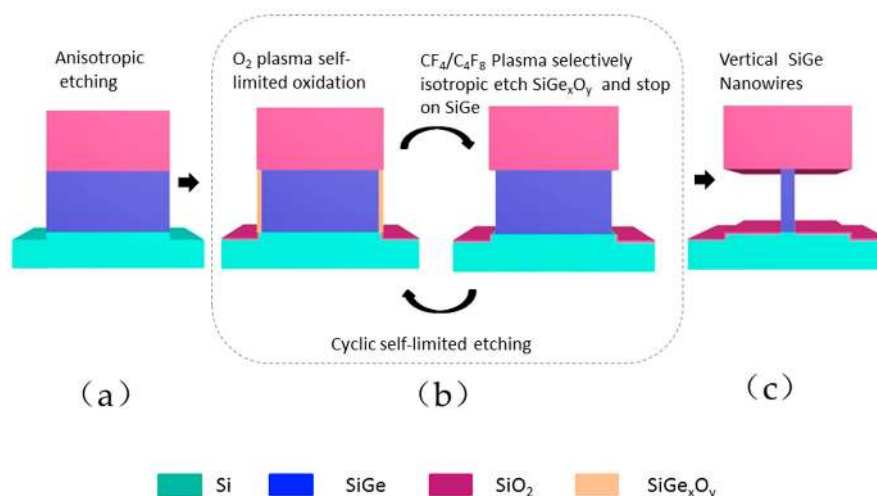
Step 2: Photoresist lattices with a diameter of 90 nm and a pitch of 500 nm were fabricated on the wafer surface by 248 nm DUV lithography.

- Step 3: An 8-inch CCP etcher was used to trim the PR lattice diameter from 90 nm to 70 nm with the gas of  $\text{CF}_4/\text{O}_2/\text{Ar}$  and opening the  $\text{SiO}_2$  hard mask with the gas of  $\text{CF}_4/\text{CHF}_3/\text{Ar}$ . Then, SiGe layer and 40 nm Si substrate were anisotropic etched by 8-inch ICP etcher with  $\text{HBr}/\text{O}_2/\text{He}$  gas.
- Step 4: PR was removed by a 8-inch ash chamber and wet clean with 100:1 diluted hydrofluoric acid (DHF).
- Step 5: An 8-inch ICP etcher with switch process function was used to atomic precisely and selectively isotropic etch SiGe. Then SiGe vertical nanowires were manufactured.
- Step 6: 10:1 DHF was used to remove the  $\text{SiO}_2$  hard mask, and the nano-pillar array was prepared.



**Figure 1.** Nano pillar manufacture flow: (a) SiGe and  $\text{SiO}_2$  film growth; (b) Lithograph obtain PR mask pattern array; (c) PR trimming,  $\text{SiO}_2$  hard mask open etching by RIE ether and SiGe/Si anisotropic etching by ICP etcher; (d) PR removed by  $\text{O}_2$  plasma; (e) SiGe vertical nanowires formed by atomic layer etching; (f)  $\text{SiO}_2$  selectively removed by DHF.

The above 5-step etching is a cyclic etching process as show in Figure 2, which is mainly two self-limiting processes: (1)  $\text{O}_2$  plasma self-limiting oxidation: 150 sccm  $\text{O}_2$ , 500 W source RF/0 W bias power, treatment can reach oxidation saturation; (2)  $\text{SiGe}_x\text{O}_y$  selective etching: 200 sccm  $\text{CF}_4/x$  sccm  $\text{C}_4\text{F}_8/500$  W source RF power/0 W bias power for selective etching of  $\text{SiGe}_x\text{O}_y$  and self-limitation stops on the SiGe surface. Repeat steps (1) and (2) until the diameter of the SiGe nanowire reaches the expected value.



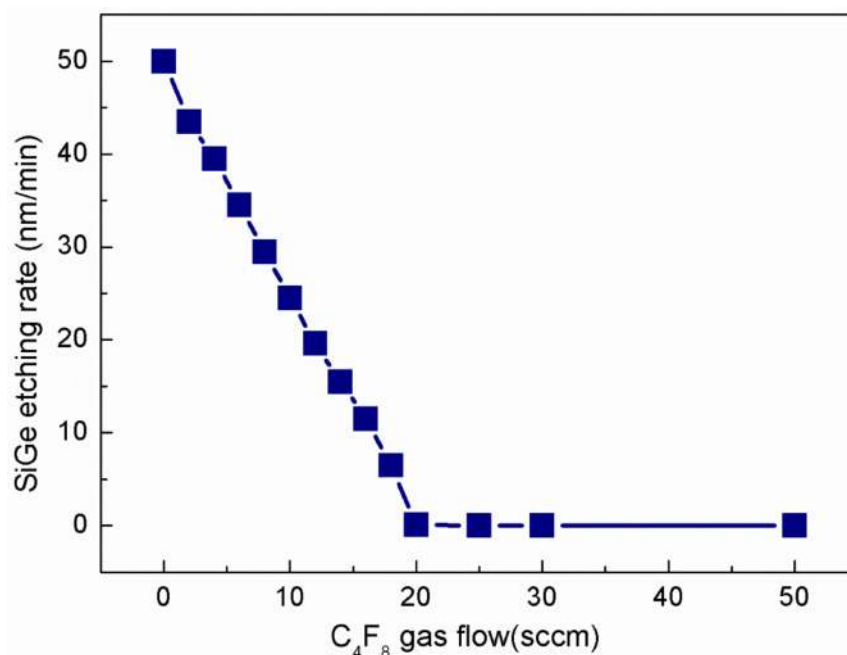
**Figure 2.** Etching process of vertical nanowires: (a) vertical etching with  $\text{HBr}/\text{O}_2/\text{He}$  ICP etcher; (b) atomic layer etching: cyclic self-limited oxidation and selective etching of SiGe oxides achieve atomic layer etching accuracy; (c) vertical SiGe nanowires with nanometer diameter formed by multiple cycle etching.

The top-view and cross-section of the sample after etching were analyzed by using high-resolution scanning electron microscope (HRSEM) to check its quality and profile of etching. The defect density in the Si layers after the SiGe release was also analyzed by using high-resolution transmission electron microscope (HRTEM). Energy dispersive spectroscopy (EDS) was employed to determine the element materials of etched layers. The strain relaxation and layer quality were examined by high-resolution x-ray diffraction (HRXRD).

### 3. Results

#### 3.1. Study of Atomic Layer Etching SiGe

It is well known that self-limiting sequential reactions are the primary feature of atomic layer etching [38]. According to previous studies, the oxidation of SiGe is self-limiting under certain conditions [39]. Therefore, the focus of this study is how to achieve self-limiting removal of  $\text{SiGe}_x\text{O}_y$  (see Figure 2) and automatically stops on the SiGe layer. We know that SiGe can be oxidized to  $\text{SiGe}_x\text{O}_y$  under  $\text{O}_2$  plasma, and Si can be oxidized to  $\text{SiO}_2$ , but before forming these, the oxide needs to open the original covalent bond. The Si–Si bond energy (2.31 eV) > Si–Ge bond energy (2.12 eV), so SiGe alloys are more susceptible to bond oxidation than pure Si [28]. The Si–O bond energy (9.0 eV) is greater than Ge–O bond energy (5.0 eV), the value of the Si–O–Ge bond energy is between the two [40], so using CF-based gas to etch the oxide will form volatile  $\text{SiF}_x$  and  $\text{GeF}_x$  and CO or  $\text{CO}_2$ . Hence, increasing the C/F ratio is expected to inhibit the etching on the surface of SiGe, because the absence of O in SiGe cannot make the rich C produce volatile CO or  $\text{CO}_2$ . It can be seen from Figure 3 that when the  $\text{CF}_4$  flow rate is fixed at 200 sccm, and the  $\text{C}_4\text{F}_8$  ratio exceeds 20 sccm, SiGe etching has been completely suppressed. Thus, the self-limiting effect of the  $\text{SiGe}_x\text{O}_y$  layer selective etching is achieved.



**Figure 3.** Etching rate of  $\text{Si}_{0.72}\text{Ge}_{0.28}$  with different gas flow of  $\text{C}_4\text{F}_8$  and  $\text{CF}_4$  gas flow fixed at 200 sccm.

Further experimental data are shown in Figure 4. At 60 mT process pressure and 500 W source RF power, the saturation or self-limiting time of oxidation and selective etching is 6 s and 5 s, respectively.

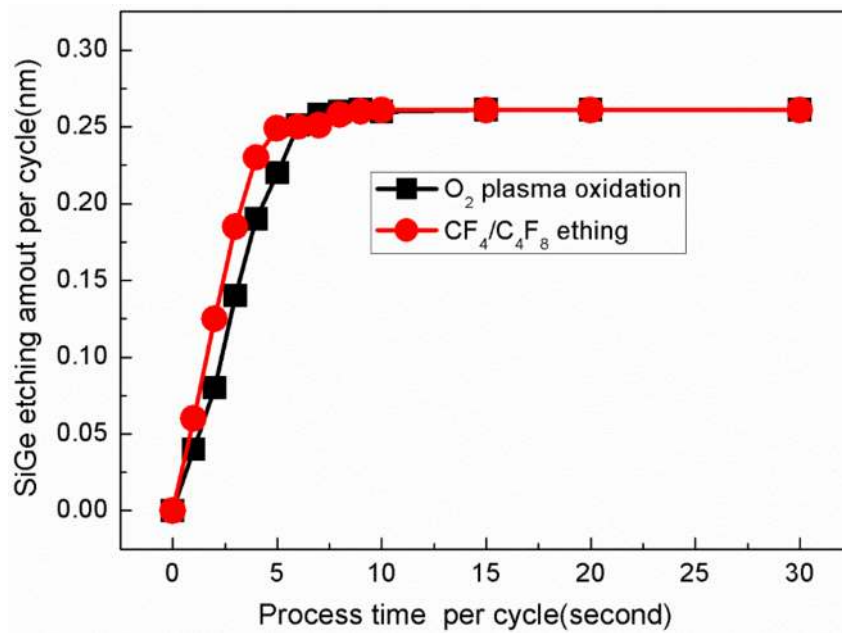


Figure 4. Si<sub>0.72</sub>Ge<sub>0.28</sub> etching amount of different process time per cycle.

### 3.2. Study of Nanowire Size and Profile Control

In order to examine the process performance of ALE, the etching conditions of different etching cycles were designed, and then the dimensional and profile characterization of the samples were performed.

Firstly, the SiGe nanowire diameter and lateral etching amount of different etching cycles are measured and compared. As shown in Figure 5, the lateral etching amount increases linearly as the number of etching cycles grows, and so do the corresponding SiGe nanometers. The diameter of the wire also decreases linearly as the number of etching cycles reduces. Through 110 cycles of ALE etching, the nanowire diameter can be controlled to less than 20 nm, and the etching amount per cycle is about 0.23 nm, so the control accuracy is very high.

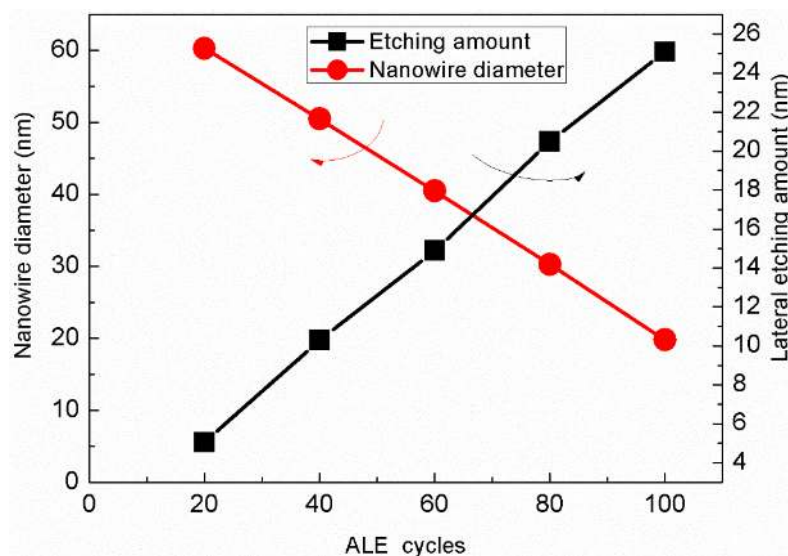
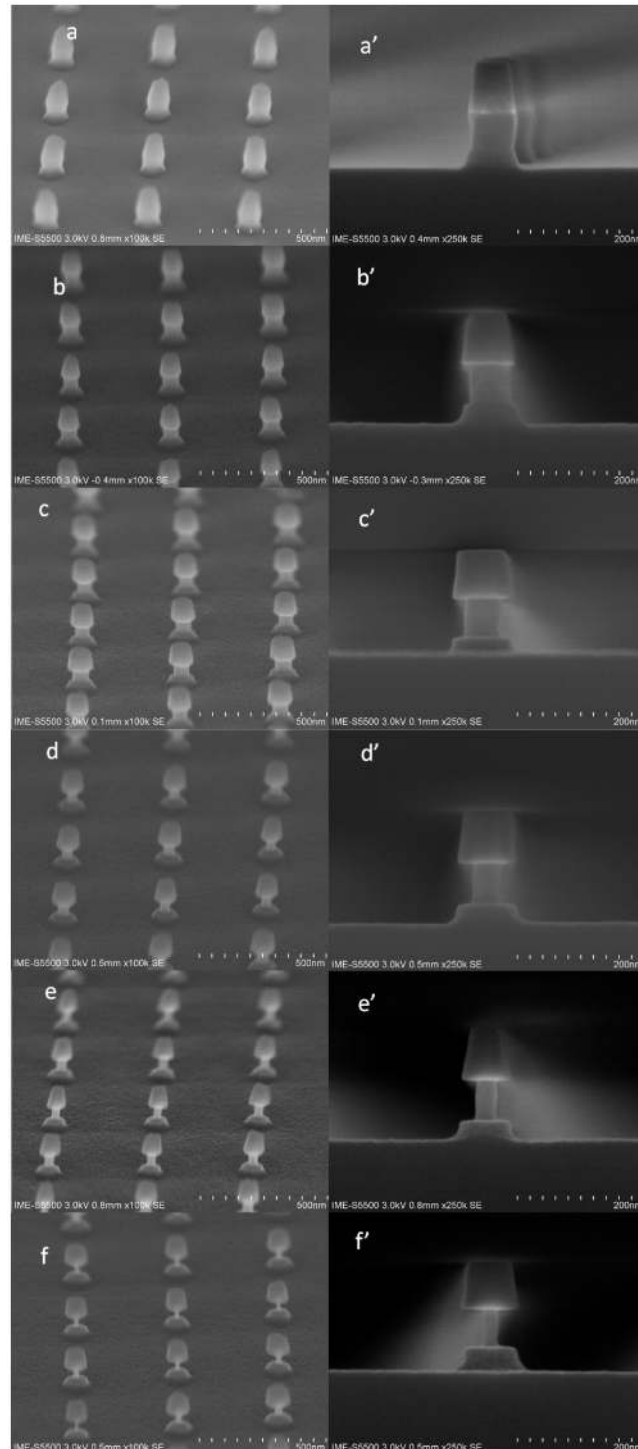


Figure 5. Etching amount and nanowire diameter after different cycles ALE etching.

Secondly, the morphology of etching was characterized. The SEM results are shown in Figure 6: the dot pattern is relatively uniform (see Figure 6a), the anisotropically etched SiGe part is relatively

vertical and the underlying silicon substrate is slightly tilted (see Figure 6a'). This is because the etching of SiGe and Si is a one-step etching. The same etching recipe is used without fine-tuning for different materials. After different cycles of etching, the lattice remains intact (Figure 6b–f), but the diameter of the SiGe part is continuously shrinking, and the shape is still steep and conformal (Figure 6b'–f')

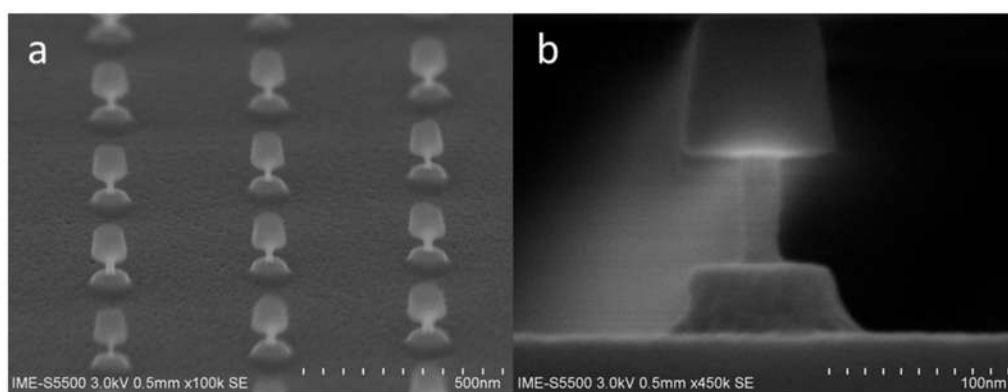


**Figure 6.** 45° top review SEM of profile: (a) after anisotropic etching without isotropic ALE etching; (b) ALE etching 20 cycles; (c) ALE etching 40 cycles; (d) ALE etching 60 cycles; (e) ALE etching 80 cycles; (f) ALE etching 100 cycles; and the cross section SEM images of different samples (a'–f'), corresponding the sample (a–f).

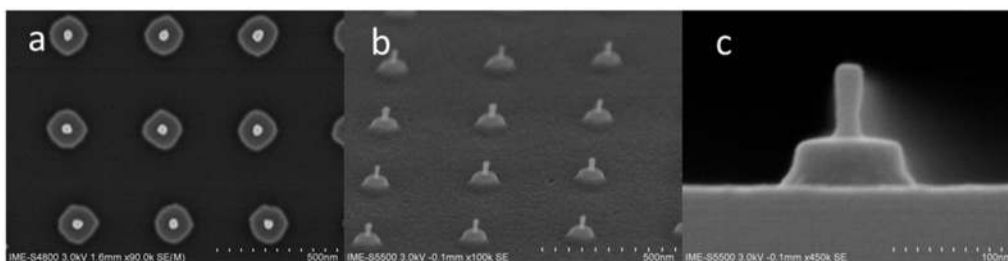
In general, through ALE etching, the diameter of the nanowires can be flexibly and accurately controlled, and the relatively steep SiGe nanowire morphology can be preserved.

### 3.3. Study Morphology of Nanowire and Nanopillar

From previous studies, it has been shown that nanowires can be flexibly prepared by using ALE technology without relying on advanced lithography technology. Next, the morphology of nanowires with a diameter of less than 20 nm is mainly studied in terms of SiO<sub>2</sub> hard mask retention and removal. The result of maintaining the SiO<sub>2</sub> hard mask is shown in Figure 7. The top view shows that all the lattices in the field of view are intact, and the multiple nanowires have good consistency at low magnifications, and the nanowires have good morphology at high magnifications. 10:1 DHF was used to remove the SiO<sub>2</sub> hard mask to obtain an independent nano-pillar. The morphological results are shown in Figure 8, which shows that the nano-pillar cross sections are uniform.



**Figure 7.** Morphology of nanowires less than 20 nm diameter after 110 cycles etching by ALE: (a) 45° top review SEM of profile; (b) cross section SEM images.

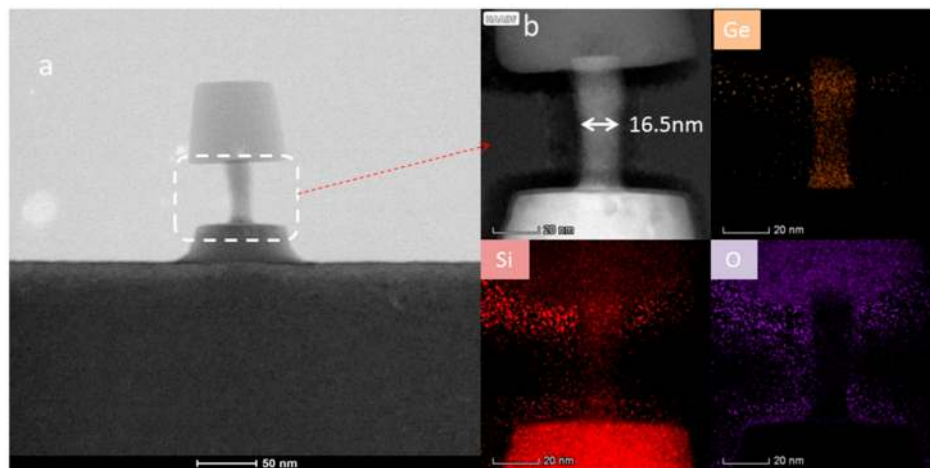


**Figure 8.** Morphology of nanowires less than 20 nm diameter after 100 cycles ALE and SiO<sub>2</sub> hard mask remove: (a) bird's-eye top review SEM of profile; (b) 45° top review SEM of profile; (c) cross section SEM images.

### 3.4. Material Quality and Interface Analysis

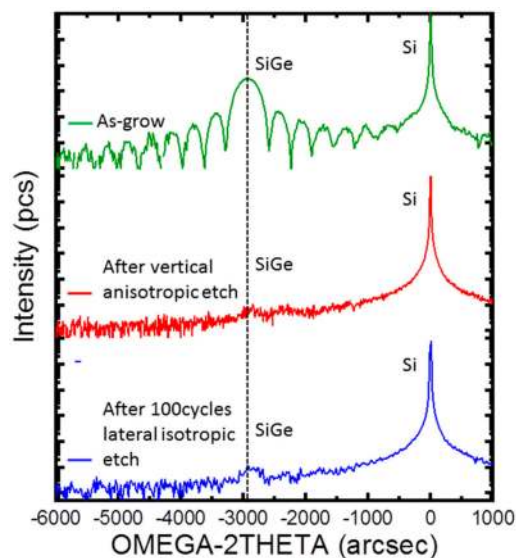
The layer quality and more detailed information about the parts of the hard mask/SiGe/Si materials have been performed by using HRTEM.

Figure 9 displays the cross-section TEM micrograph of sample in Figure 7b. It is also shown that the nanowires are slightly distorted due to the TEM sample preparation. Figure 9b HRTEM results show that SiGe remains basically perfect in crystal structure and diameter about 16.5 nm. EDS mapping shows that Ge element is mainly in vertical nanowires, Si element is distributed in SiO<sub>2</sub>, SiGe, and Si substrates, O is mainly extant in SiO<sub>2</sub> hard mask and loading filling material, and the interface of SiGe is also very thin.



**Figure 9.** TEM and EDX mapping: (a) TEM picture of all structure; (b) HRTEM and EDS mapping of near isotropic etching region.

Finally, the integrity of strain in SiGe during etch process has also been studied. It is expected that the strain has impact on the device performance, therefore, strain relaxation has to be studied. In order to obtain a more accurate measurement of strain, reciprocal lattice maps around (113) reflection were performed. Unfortunately, no SiGe peak could be observed due to small size of SiGe layer after etching. Therefore, rocking curves (RCs) measurements were carried out where the x-ray beam has high intensity. Figure 10 shows these RCs measurements. The intensity of SiGe after etching has been remarkably reduced due to removal of large volume of the layer. In these curves, the position of the SiGe has not varied showing the initial strain has been preserved.



**Figure 10.** Rocking curves of sample at different steps of processing.

The processed vertical SiGe NWs can be later functionalized by e.g., metal oxide to form gate all around (GAA) transistor for future gas sensor.

#### 4. Conclusions

With ALE etching, an innovative method for manufacturing nanowires was obtained. The results show that the diameter of the nanowires can be flexibly adjusted from 60 nm to 16.5 nm, and the morphology is under precise control, the microstructure is complete, and there is also no obvious etching residue contamination on the interface. The ALE method could be co-used with advanced



lithography (such as initial line width control to <45 nm), and it will be expected to obtain much smaller nanowires with high density in the future. This technique will have very wide and promising applications in sensors.

**Author Contributions:** Conceptualization, J.L. (Junjie Li), G.W., H.H.R.; methodology, J.L. (Junjie Li), N.Z., Q.Z., A.D., Y.Z., J.G., Z.K., H.L., J.X., C.L., X.Y., Y.L. (Yangyang Li), X.W., H.Y. (Hong Yang), X.M., J.Z., T.H., T.Y., J.L. (Junfeng Li), H.Y. (Huaxiang Yin), H.Z.; data curation, J.L. (Junjie Li) and J.H.; writing—original draft preparation, J.L. (Junjie Li); writing—review and editing, J.L. (Junjie Li), G.W. and H.H.R.; supervision, W.W. and Y.L. (Yongliang Li); project administration, W.W.; funding acquisition, W.W. All authors have read and agreed to the published version of the manuscript.

**Funding:** This work was financially supported by the science and technology planning project of Beijing (Grant No. Z191100010618005), the National Key Project of Science and Technology of China (Grant No. 2017ZX02315001-002) and the National Key Research and Development Program of China (Grant No. 2016YFA0301701).

**Conflicts of Interest:** The authors declare no conflict of interest.

## References

- Dey, A. Semiconductor metal oxide gas sensors: A review. *Mater. Sci. Eng. B Adv.* **2018**, *229*, 206–217. [[CrossRef](#)]
- Xu, Y.; Hu, X.; Kundu, S.; Nag, A.; Afsarimanesh, N.; Sapra, S.; Han, T. Silicon-Based Sensors for Biomedical Applications: A Review. *Sens. Basel* **2019**, *19*, 2908. [[CrossRef](#)] [[PubMed](#)]
- Hsu, H.F.; Chen, C.A.; Liu, S.W.; Tang, C.K. Fabrication and Gas-Sensing Properties of Ni-Silicide/Si Nanowires. *Nanoscale Res. Lett.* **2017**, *12*, 1–8. [[CrossRef](#)] [[PubMed](#)]
- Jang, B.; Kim, M.H.; Baek, J.; Kim, W.; Lee, W. Highly Sensitive Hydrogen Sensors: Pd-coated Si Nanowire Arrays for Detection of Dissolved Hydrogen in Oil. *Sens. Actuators, B* **2018**, *273*, 809–814. [[CrossRef](#)]
- Mirzaei, A.; Kang, S.Y.; Choi, S.W.; Kwon, Y.J.; Choi, M.S.; Bang, J.H.; Kim, H.W. Fabrication and gas sensing properties of vertically aligned Si nanowires. *Appl. Surf. Sci.* **2018**, *427*, 215–226. [[CrossRef](#)]
- Nuzaihan, M.; Hashim, U.; Arshad, M.M.; Kasjoo, S.R.; Rahman, S.F.A.; Ruslinda, A.R.; Shahimin, M.M. Electrical Detection of Dengue Virus (DENV) DNA Oligomer using Silicon Nanowire Biosensor with Novel Molecular Gate Control. *Biosens. Bioelectron.* **2016**, *83*, 106–114. [[CrossRef](#)]
- Tran, D.P.; Pham, T.T.T.; Wolfrum, B.; Offenhäusser, A.; Thierry, B. CMOS-Compatible Silicon Nanowire Field-Effect Transistor Biosensor: Technology Development toward Commercialization. *Materials* **2018**, *11*, 785. [[CrossRef](#)]
- Zhang, N.; Zhang, Z.; Zhang, Q.; Wei, Q.; Zhang, J.; Tang, S.; Yan, J. O<sub>2</sub> plasma treated biosensor for enhancing detection sensitivity of sulfadiazine in a high-k HfO<sub>2</sub> coated silicon nanowire array. *Sens. Actuators B* **2020**, *306*, 127464. [[CrossRef](#)]
- Ebrahim, S.; Raoof, M.; Ramadan, W.; Soliman, M. New self assembly monolayer onto SiGe as a selective biosensor for single-strand DNA. *Microelectron. Eng.* **2016**, *160*, 87–93. [[CrossRef](#)]
- Chen, Y.M.; Chang, T.Y.; Lai, C.H.; Chang, K.M.; Chen, C.F.; Lai, Y.L.; Hsu, T.R. Investigation of Defect Free SiGe Nanowire Biosensor Modified by Dual Plasma Technology. *J. Nanosci. Nanotechnol.* **2016**, *16*, 1454–1459. [[CrossRef](#)]
- Singh, A.; Amin, S.I.; Anand, S. Label Free Detection of Biomolecules Using SiGe doped Dual Electrode Doping-Less Dielectrically Modulated Tunnel FET. *Silicon* **2020**, 1–8. [[CrossRef](#)]
- Ferain, I.; Colinge, C.A.; Colinge, J.P. Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors. *Nature* **2011**, *479*, 310–316. [[CrossRef](#)] [[PubMed](#)]
- Loubet, N.; Hook, T.; Montanini, P. Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET. Available online: <http://gen.lib.rus.ec/scimag/10.23919%2FVLSIT.2017.7998183> (accessed on 20 August 2017).
- Veloso, A.; Eneman, G.; Huynh-Bao, T. Vertical Nanowire and Nanosheet FETs: Device Features, Novel Schemes for Improved Process Control and Enhanced Mobility, Potential for Faster & More Energy Efficient Circuits. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019.
- Zhao, Z.; Li, Y.; Wang, G.; Du, A.; Li, Y.; Zhang, Q.; Wang, W. Process optimization of the Si<sub>0.7</sub>Ge<sub>0.3</sub> Fin Formation for the STI first scheme. *Semicond. Sci. Technol.* **2019**, *34*, 125008. [[CrossRef](#)]

16. Van Dal, M.J.H.; Vellianitis, G.; Doornbos, G.; Duriez, B.; Holland, M.C.; Vasen, T.; Shen, T.M. Ge CMOS gate stack and contact development for Vertically Stacked Lateral Nanowire FETs. In Proceedings of the IEEE 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018.
17. Zheng, G.; Patolsky, F.; Cui, Y.; Wang, W.U.; Lieber, C.M. Multiplexed Electrical Detection of Cancer Markers with Nanowire Sensor Arrays. *Nat. Biotechnol.* **2005**, *23*, 1294–1301. [[CrossRef](#)]
18. Puppo, F.; Doucey, M.A.; Delaloye, J.F.; Moh, T.S.; Pandraud, G.; Sarro, P.M.; Carrara, S. SiNW-FET in-Air Biosensors for High Sensitive and Specific Detection in Breast Tumor Extract. *IEEE Sens. J.* **2015**, *16*, 3374–3381. [[CrossRef](#)]
19. Zhuge, J.; Wang, R.; Huang, R.; Zou, J.; Huang, X.; Kim, D.W.; Wang, Y. Experimental Investigation and Design Optimization Guidelines of Characteristic Variability in Silicon Nanowire CMOS Technology. In Proceedings of the IEEE 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, USA, 7–9 December 2009.
20. Mastari, M.; Charlesa, M.; Bogumilowicza, Y. SiGe nano-heteroepitaxy on Si and SiGe nano-pillars. *Nanotechnology* **2018**, *29*, 1–32. [[CrossRef](#)]
21. Yirka, B. New nanowire transistors may help keep Moore's Law alive. *Nanoscale* **2013**, *5*, 2437–2441.
22. Yin, X.; Zhang, Y.; Zhu, H.; Wang, G.L.; Li, J.J.; Du, A.Y.; Xie, L. Vertical Sandwich Gate-All-Around Field-Effect Transistors with Self-Aligned High-k Metal Gates and Small Effective-Gate-Length Variation. *IEEE Electr. Device L.* **2020**, *41*, 8–11. [[CrossRef](#)]
23. Holländer, B.; Buca, D.; Mantl, S.; Hartmann, J.M. Wet Chemical Etching of Si, Si<sub>1-x</sub>Ge<sub>x</sub>, and Ge in HF:H<sub>2</sub>O<sub>2</sub>:CH<sub>3</sub>COOH. *J. Electrochem. Soc.* **2010**, *157*, 643–646.
24. Johnson, F.S.; Miles, D.S.; Grider, D.T.; Wortman, J.J. Selective Chemical Etching of Polycrystalline SiGe Alloys with Respect to Si and SiO<sub>2</sub>. *J. Electron. Mater.* **1992**, *21*, 805–810. [[CrossRef](#)]
25. Kil, Y.H.; Yang, J.H.; Kang, S.; Jeong, T.S.; Kim, T.S.; Shim, K.H. Selective Chemical Wet Etching of Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si Multilayer. *J. Semicond. Tech. Sci.* **2013**, *13*, 668–673. [[CrossRef](#)]
26. Loubet, N.; Kormann, T.; Chabanne, G.; Denorme, S.; Dutartre, D. Selective etching of Si<sub>1-x</sub>Ge<sub>x</sub> versus Si with gaseous HCl for the formation of advanced CMOS devices. *Thin Solid Films* **2008**, *517*, 93–97. [[CrossRef](#)]
27. Bogumilowicz, Y.; Hartmann, J.M.; Truche, R.; Campidelli, Y.; Rolland, G.; Billon, T. Chemical vapour etching of Si, SiGe and Ge with HCl; applications to the formation of thin relaxed SiGe buffers and to the revelation of threading dislocations. *Semicond. Sci. Technol.* **2005**, *20*, 127–134. [[CrossRef](#)]
28. Hartmann, J.M.; Destefanis, V.; Rabill', G. HCl selective etching of SiGe versus Si in stacks grown on (1 1 0). *Semicond. Sci. Technol.* **2010**, *25*, 105009. [[CrossRef](#)]
29. Borel, S.; Arvet, C.; Bilde, J. Isotropic etching of SiGe alloys with high selectivity to similar materials. *Microelectron. Eng.* **2004**, *73*, 301–305. [[CrossRef](#)]
30. Caubet, V.; Beylier, C.; Borel, S. Mechanisms of isotropic and selective etching between SiGe and Si. *J. Vac. Sci. Technol. B* **2006**, *24*, 2748–2754. [[CrossRef](#)]
31. Pargon, E.; Petit-Etienne, C.; Youssef, L.; Thomachot, G.; David, S. New route for selective etching in remote plasma source: Application to the fabrication of horizontal stacked Si nanowires for gate all around devices. *J. Vac. Sci. Technol. A* **2019**, *37*, 040601. [[CrossRef](#)]
32. Li, J.; Wang, W.; Li, Y.; Zhou, N.; Wang, G.; Kong, Z.; Yang, H. Study of selective isotropic etching Si<sub>1-x</sub>Ge<sub>x</sub> in process of nanowire transistors. *J. Mater. Sci. Mater. Electron.* **2019**, 1–10.
33. Radamson, H.; Simoen, E.; Luo, J.; Zhao, C. *Past, Present and Future of CMOS*; Woodhead Publishing: Cambridge, UK, 2018.
34. Radamson, H.H.; Thylen, L. *Monolithic Nanoscale Photonics-Electronics Integration in Silicon and Other Group IV Elements*; Elsevier: San Diego, CA, USA, 2014.
35. Zhang, Q.; Tu, H.; Gu, S.; Zhang, Z.; Wang, G.; Wei, F.; Fan, Y. Influence of Rapid Thermal Annealing on Ge-Si Interdiffusion in Epitaxial Multilayer Ge<sub>0.3</sub>Si<sub>0.7</sub>/Si Superlattices with Various GeSi Thicknesses. *ECS J. Solid State Sci. Technol.* **2018**, *7*, 671–676. [[CrossRef](#)]
36. Wang, G.; Abedin, A.; Moeen, M.; Kolahdouz, M.; Luo, J.; Guo, Y.; Zhao, C. MoeenMahdi. Integration of highly-strained SiGe materials in 14 nm and beyond nodes FinFET technology. *Solid State Electron.* **2018**, *103*, 222–228. [[CrossRef](#)]
37. Wang, G.; Luo, J.; Qin, C.; Liang, R.; Xu, Y.; Liu, J.; Xu, J. Integration of Highly Strained SiGe in Source and Drain with HK and MG for 22 nm Bulk PMOS Transistors. *Nanoscale Res. Lett.* **2017**, *12*, 1–7. [[CrossRef](#)] [[PubMed](#)]

38. Kanarik, K.J.; Lill, T.; Hudson, E.A.; Sriraman, S.; Tan, S.; Marks, J.; Gottscho, R.A. Overview of atomic layer etching in the semiconductor industry. *J. Vac. Sci. Technol. A* **2015**, *33*, 020802. [[CrossRef](#)]
39. Rozé, F.; Gergaud, P.; Jaouen, N. SiGe Oxidation Kinetics and Oxide Density Measured by Resonant Soft X-ray Reflectivity. In Proceedings of the 2017 IEEE 12th Nanotechnology Materials and Devices Conference, Singapore, Singapore, 2–4 October 2017.
40. Fischer, B.; Pollak, R.A.; DiStefano, T.H. Electronic structure of  $\text{SiO}_2$ ,  $\text{Si}_x\text{Ge}_{1-x}\text{O}_2$ , and  $\text{GeO}_2$  from photoemission spectroscopy. *Phys. Rev. B* **1977**, *15*, 3193–3199. [[CrossRef](#)]



© 2020 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).