Briefs

A Novel Hetero-Material Gate (HMG) MOSFET for Deep-Submicron ULSI Technology

Xing Zhou and Wei Long

***Abstract*— A novel hetero-material gate MOSFET intended for integration into the existing deep-submicron silicon technology is proposed and simulated. It is shown that by adding a layer of material with a larger workfunction to the source side of the gate, short-channel effects can be greatly suppressed without degrading the driving ability. The threshold voltage roll-off can be compensated and tuned by controlling the length of this second gate. The new structure has great potential in breaking the barrier of deep-submicron MOSFET's scaling beyond 0.1-μm technologies.**

***Index Terms*— Asymmetric MOSFET, asymmetric spacer, deep-submicron technology, gate-material engineering, hetero-material gate MOSFET, MOSFET scaling.**

I. Introduction

A MOSFET, by its own geometric nature, is a symmetrical device in the sense that the source and drain are interchangeable—they are identified by the operating bias rather than the structure. However, as the gate length becomes increasingly small, the device operation is asymmetrical even at very low drain bias, resulting in short-channel effects (SCE) such as threshold voltage roll-off and DIBL as well as hot-carrier effects that limit the transistor scaling. As the conventional scaling limit is approached, new structures employing asymmetric architectures become inevitable. The asymmetric channel profile engineering [1] has demonstrated enhanced transconductance due to enhanced carrier velocity in the channel region. However, for ULSI integration, it cannot be expected that all the transistors have the same orientation to get the desired channel profile with a tilted implant. The recently proposed dual-material gate field-effect transistor (DMGFET) [2], based on the ideas of dual-gate [3] and split-gate [4] transistors, is intrinsically an asymmetric device, and it has shown a simultaneous transconductance enhancement and suppression of short-channel effects. This "DMG effect" has been demonstrated with a 1-μm HFET, and it was predicted that more benefits could be obtained for devices with ultra-small dimensions. It is of vital importance, however, such novel devices can be eventually integrated into the current ULSI technology.

In this brief, we present theoretical analysis of a novel hetero-material gate (HMG) MOSFET, based on the concept of the DMGFET [2], intended for integration with the current deep-submicron MOS technology. The scaling characteristics of the HMG-MOSFET are compared with those of a conventional single-material gate (SMG) MOSFET based on a practical 0.25-μm CMOS technology, which demonstrate superior SCE suppression without sacrificing the driving ability. It is predicted that the impact would be revolutionary if a breakthrough in manufacturing technology for realizing the proposed novel structure could be unleashed.

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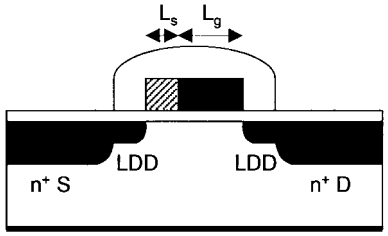


Fig. 1. Structure of the HMG-MOSFET.

II. HMG-MOSFET Structure and Simulation Models

A conventional SMG-MOSFET for a 0.25-μm technology is modeled by the two-dimensional (2-D) device simulator MEDICI with the following parameters: gate oxide thickness $t_{ox} = 50$ Å; Gaussian channel doping profile with peak concentration $N_{sub} = 4 \times 10^{17}$ cm^{-3} and characteristic length of 0.25 μm; LDD junction depth $x_j = 70$ nm; S/D junction depth of 150 nm; oxide spacer thickness of 125 nm; n$^+$ poly-Si gate workfunction $W_g = 4.17$ eV; fixed oxide charge density $N_{ss} = 3 \times 10^{10}$ cm^{-2}; gate (or drawn channel) length L_g $(= L_c)$, which is a variable for studying the scaling characteristics. The physical model used is the drift-diffusion model with concentration, perpendicular- and parallel-field dependent mobility models. Poly depletion is not included. No attempt is made to evaluate the physical models since the focus here is on qualitative and *relative* comparisons.

The proposed HMG-MOSFET is shown schematically in Fig. 1, which comprises a poly-Si gate of length L_g (same as SMG) and a larger workfunction material of length L_s to the source side of, and in contact with, the gate, which we call it "source-gate" (or "S-gate"). For compatibility with the current MOS technology, we assume that the S-gate could be formed by an "asymmetric spacer process" (similar to oxide spacer for LDD) with precise and uniform thickness control, while the minimum feature size is still defined by the poly-Si line (L_g) of the conventional technology. According to [2], the S-gate would be the main gate to control carrier acceleration while the poly-gate would serve as a "screening gate." In this work, we have used tungsten for the "S"-gate with a workfunction $W_s = 4.63$ eV. The *channel length* of the HMG-MOSFET is then given by $L_c = L_g + L_s$. All other device parameters used for the HMG simulations are equivalent to the SMG parameters unless otherwise stated.

III. Computer Experiments and Discussions

Our first computer experiment is for the scaling characteristics of the HMG-MOSFET, in which the length of the S-gate is fixed at $L_s = 0.1$ μm and the poly-Si gate length is varied for $L_g = 0.1, 0.15, 0.2, 0.3, 0.4$, and 0.9 μm, and compared to those of the SMG-MOSFET with $L_g = 0.2, 0.25, 0.3, 0.4, 0.5$, and 1 μm. This is to simulate a process in which the HMG-MOSFET would be formed by adding a "tungsten spacer" of thickness L_s to the source side of the gate of an existing process. There are two scenarios for the comparison: For I–V characteristics, it is fair to compare the same channel length ($L_c = L_g + L_s$ for HMG, $L_c = L_g$ for SMG). For technology, the same gate length (L_g) should be used, assuming that

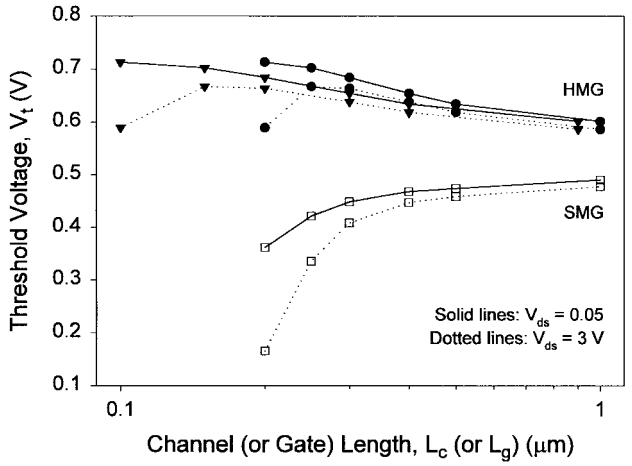


Fig. 2. Comparison of the linear (solid lines) and saturation (dotted lines) threshold voltages against channel length (circles) or gate length (triangles).

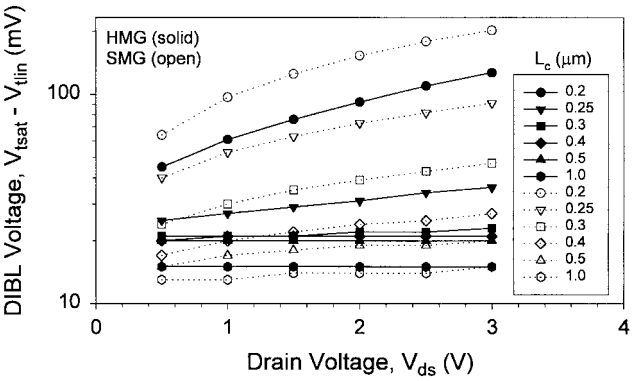


Fig. 3. Comparison of the DIBL voltages as a function of the drain bias for each channel length.

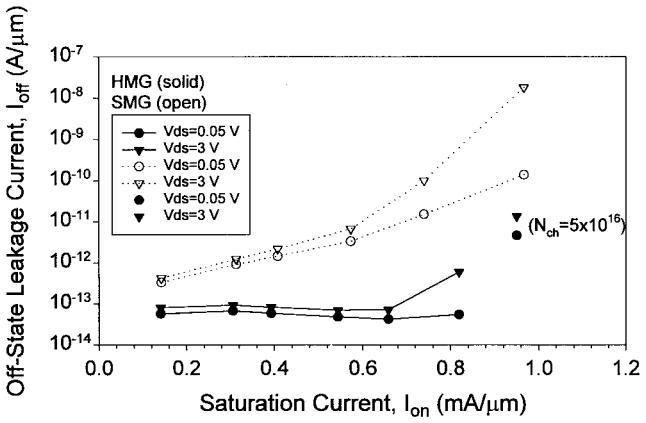
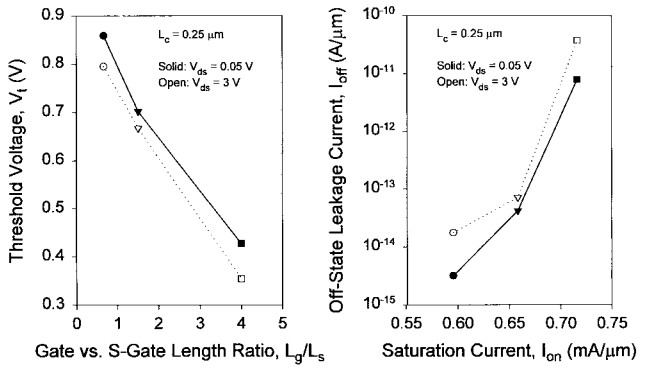


Fig. 4. Leakage currents (at $V_{ds} = 0.05$ or 3 V) against the saturation current (each pair corresponds to a different channel length). One pair of $I_{\rm on}/I_{\rm off}$ for the HMG-MOSFET with $L_g/L_s = 0.15/0.1$ and channel doping $N_{ch} = 5 \times 10^{16}$ cm^{-3} is also shown as a comparison.



(a) (b)

Fig. 5. (a) Threshold voltages as a function of the L_g/L_s ratio and (b) the corresponding leakage current versus saturation current.

the S-gate of the HMG could be formed by a spacer process rather than by another lithographic definition.

The device performance parameters are extracted from the calculated I_{ds}–V_{gs}characteristics for the two types of MOSFET's. The linear threshold (V_{tlin}) is based on the peak-transconductance method at $V_{ds} = 0.05$ V and the saturation threshold (V_{tsat}) is based on the constant-current method at $V_{ds} = 3$ V where the current is defined as the drain current when $V_{gs} = V_{tlin}$ and $V_{ds} = 0.05$ V. The saturation current ($I_{\rm on}$) and leakage current ($I_{\rm off}$) are defined as the drain current at $V_{gs} = V_{ds} = 3$ V and at $V_{gs} = 0$ and $V_{ds} = 0.05$ V (or $V_{ds} = 3$ V as stated), respectively. The extracted threshold voltage is shown in Fig. 2. It can be seen that, contrary to the normal V_t roll-off, the HMG-MOSFET's V_t increases as the channel (or gate) length is decreased. This is a very important new feature of the HMG-MOSFET (to be discussed below). For relative comparisons, the DIBL voltage ($V_{tsat} - V_{tlin}$) for the two transistors is shown in Fig. 3. It is observed that the DIBL effect is reduced more at smaller channel length—up to 40% at $L_c = 0.2$ μm, or an order of magnitude if the same $L_g = 0.2$ μm is compared. The off-state leakage current is found to be significantly reduced with comparable saturation current which, of course, is partially due to the elevated V_t of the HMG-MOSFET. The $I_{\rm on}/I_{\rm off}$ relationship for the two devices is plotted in Fig. 4, which shows the superior $I_{\rm on}/I_{\rm off}$ tradeoff of the HMG-MOSFET.

To investigate the special feature of V_t roll-up at decreasing L_g, we further study the effect of L_g/L_s ratio at a fixed $L_c = 0.25$ μm for the HMG-MOSFET. The result is plotted in Fig. 5 with $L_g/L_s =$ $0.1/0.15$, $0.15/0.1$, and 0.2/0.05. As the L_g/L_s ratio is decreased, V_t increases since the portion of the larger workfunction material is increased. This explains the reason for the V_t roll-up at decreasing L_g with fixed L_s (Fig. 2), which compensates the normal V_t roll-off. This unique feature adds another design freedom to tune the V_t roll-up/roll-off with different "tungsten spacer thickness" (L_s). It is also observed from Fig. 5 that there exists an optimum L_g/L_s ratio for each fixed L_c where the DIBL voltage is minimized and the $I_{\rm on}/I_{\rm off}$ has an optimum tradeoff. This is determined by the location of the workfunction step where the channel potential is discontinuous, causing the electron velocity to have an optimum distribution in the channel [2].

Finally, since the simulated V_t of the HMG-MOSFET is much larger than that of the SMG-MOSFET, more design choices are available to boost the driving ability by reducing either the channel doping or oxide thickness. For the $L_g/L_s = 0.15/0.1$ HMG-MOSFET, when the peak channel doping is reduced to 5×10^{16} cm^{-3} to obtain a comparable $V_t = 0.5$ V, $I_{\rm on}$ is increased by 30% (g_m is increased by 22%) while $I_{\rm off}$ is still much lower (below 5×10^{-12} A/μm). The $I_{\rm on}/I_{\rm off}$ data is shown in Fig. 4 as a comparison.

In addition to the superior $I_{\rm on}/I_{\rm off}$ characteristics and SCE suppression of the HMG-MOSFET, this novel device opens the door for an array of new design options. Besides the L_g/L_s ratio for tuning V_t, different workfunction difference ($W_s - W_g$) also adds another freedom of choice, which could be made with a variety of materials for the gate and the S-gate, e.g., by using different

types of silicides [5] or metal [6], and variable workfunction using poly-(Si, Ge) [7]. Moreover, if the proposed "spacer process" for the S-gate could be realized, the same can be done on the drain side of the gate with a lower workfunction (W_d) material of length L_d, called the "drain-gate" (or "D-gate"), to be used for controlling the channel resistivity on the drain side. (This is why we have chosen the acronym "HMG" different from the "DMG" in [2].) Then, in principle, the performance of the HMG-MOSFET (which is still compatible with the conventional MOS technology) could be optimized with a proper choice of $L_s/L_g/L_d$ and $W_s/W_g/W_d$ by "engineering" the gate material and, hence, the potential, field, and carrier velocity distributions along the channel.

IV. Conclusion

In conclusion, based on the original idea of the DMGFET, a novel hetero-material gate MOSFET is proposed and its performance has been simulated with a 2-D numerical model. The new device has shown superior and simultaneous performance enhancement for both the "on" and "off" states as compared with the conventional single-material gate MOSFET. It could potentially be integrated into the existing deep-submicron MOS technology. Moreover, it opens brand new ways of engineering and optimizing the performance of ultra-small devices with many degrees of freedom. A technology breakthrough in realizing the proposed device would have tremendous impact on the ULSI technology.

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A High-Performance Polycrystalline Silicon Thin Film Transistor with a Silicon Nitride Gate Insulator

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***Abstract*— We have fabricated a high performance polycrystalline silicon (poly-Si) thin film transistor (TFT) with a silicon-nitride (SiN_X) gate insulator using three stacked layers: very thin layer of hydrogenated amorphous silicon (a-Si : H), SiN_X and laser annealed poly-Si. After patterning thin a-Si : H/SiN_X layers, gate, and source/drain regions were ion-doped and then Ni layer were deposited. Such structure was annealed at 250°C to form NiSi silicide phase. The low resistive NiSi silicides were introduced as gate/source/drain electrodes in order to reduce the process steps. The poly-Si with a grain size of 250 nm and low resistance n^+ poly-Si for ohmic contact were introduced to have a high performance TFT. The fabricated poly-Si TFT exhibited a field effect mobility of 262 cm^2/Vs and a threshold voltage of 1 V.**

I. Introduction

Polycrystalline silicon (poly-Si) thin film transistors (TFT's) are currently attracting much attention for use in active matrix liquid crystal displays (AMLCD's) [1]. The peripheral circuits using complementary metal oxide semiconductor (CMOS) process and the TFT for switching devices can be fabricated on the same glass substrate [2]. The excimer laser crystallization is a promising method to obtain low temperature, high performance poly-Si for TFT's [3], [4].

Sera *et al.* [3] have obtained a normal staggered poly-Si TFT with a high field effect mobility of $\sim$120 cm^2/Vs in the peripheral area. Sameshima *et al.* [5] utilized a multistep XeCl annealing in order to dehydrogenate and to melt hydrogenated amorphous silicon (a-Si : H) by controlling the laser energy density. Yuki *et al.* [6] deposited a-Si : H films with low hydrogen concentration and irradiated an Ar^+ laser on the whole substrate area to fabricate a poly-Si TFT-LCD panel. The highest carrier mobility for the poly-Si TFT reported so far was 640 cm^2/Vs using a SiO_2 deposited by remote plasma chemical vapor deposition [7].

In our previous work, we have fabricated a novel self-aligned poly-Si TFT using silicide layers [8]. To simplify the fabrication process of the poly-Si TFT and to decrease the contact resistance, we used the Ni silicide as ohmic contact layers of the source/drain electrodes. Recently, an ion shower doping technique using a broad ion beam without mass separation and beam scanner has been utilized to fabricate both a-Si : H TFT and poly-Si TFT [9]. In the present work, we have fabricated a high-performance poly-Si TFT with Ni silicide source/drain/gate electrodes in which a large grain poly-Si and low resistance ion doped n^+ poly-Si were utilized. The fabricated poly-Si TFT's exhibited a field effect mobility of $\sim$262 cm^2/Vs and a threshold voltage of $\sim$1 V. It is noted that a high performance poly-Si TFT can be obtained by using only two mask steps. This is possible by utilizing a triple layer of thin a-Si : H/SiN_X/poly-Si and simultaneous silicide formation of the source, drain, and gate contacts.

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