A novel high CMRR Trans-Impedance Instrumentation Amplifier for biomedical applications

R. Nagulapalli, K. Hayatleh, S. Barker, S. Zourob, N. Yassine, S. Raparthy and A. A. Tammam

A compact high gain current mode instrumentation amplifier (IA) has been proposed for biomedical imaging applications. Conventional IAs rely on several matching resistors which occupies a lot of silicon area, the input and output common mode voltages are exactly same and the maximum applied signal amplitude is limited by internal node voltage swings. The present proposal eliminates the need for matching resistors by processing signals in the current mode. Hence input amplitudes are no longer limited by the voltage headroom and input and output common-mode voltages can be independent. An amplifier with a differential gain greater than 52dB and a common mode rejection ratio (CMRR) greater than 120dB has been implemented in 65nm CMOS Technology and Post layout simulations were presented. The total circuit occupies 4500um^2 silicon area and circuit consumes ~260µA from 1.8V power supply.

Keywords: CMRR, Low Power, CMOS, Trans-impedance.

***1. Introduction*:** In recent days, Instrumentation amplifiers have become essential in all Bio-medical sensing and imaging fields due to the diversified needs for Quality healthcare technologies and physiological measurement systems, which can efficiently monitor biological signals such as ECG, EEG and blood pressure [1]. Fig. 1 shows the block diagram of the biomedical imaging analog frontend that includes the electrodes, instrumentation amplifier (IA), Variable Gain amplifier (VGA), Low pass filter and analog to digital converter (ADC). The key element in the measurement front end is the instrumentation amplifier (IA) that determines the sensitivity of the system which can amplify the weak signals without adding significant noise. Amplifying biological signals possess stringent challenges compared to actuator sensor output signals due to them naturally having low frequencies. Fig. 2 describes all signal amplitude and frequency varies from the uV to tens of mV's.

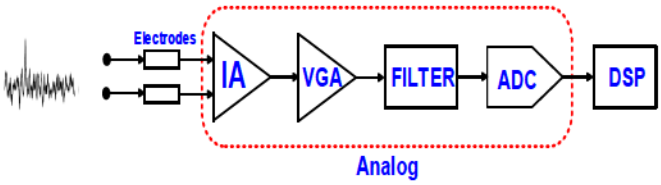

Fig. 1 Biomedical imaging Front-end

This paper is divided into several sections. Section 2 describes the traditional IA and challenges, section 3 describes the proposed compact IA, section 4 describes the op-amp design specific to the IA and finally, section 5 describes the prototype simulation results IA and summarizes the paper.

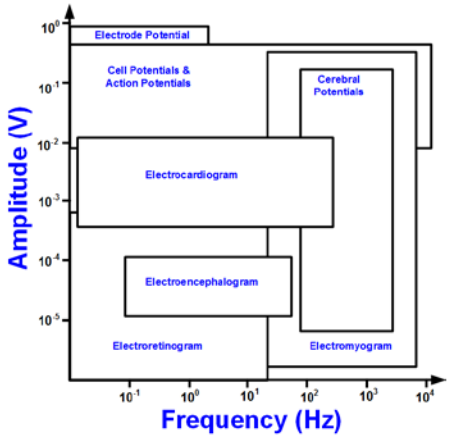

Fig. 2 Biomedical signal Frequency and amplitudes.

2. Traditional IA: To amplify weak and noisy signals with lot of common mode noise (coupling among the electrodes or power supply) the IA needs to have stable gain, ultra-low noise, high CMRR and high impedance [2]. There are two basic ways to implement IA: with the voltage feedback through resistors or with current feedback through trans-conductors (g_m-cells). Fig. 3 shows the conventional resistive feedback of three op-amps instrumentation amplifiers, which consist of two stages. The first is a gain stage which consists of Op_1, Op_2, R_1 and R_g, whose proposal is to amplify the differential mode of the input signal and pass common signals with unity gain. The second stage is the difference amplifier, which consists of Op_3, R_2 and R_3, should cancel the common mode. The difference amplifier will amplify the differential mode while cancelling the common mode, (Assuming resistors are well matched) hence the overall CMRR would be very high [3]. This amplifier presents a very high input impedance so that the signal attenuation because of the electrode impedance is minimal.

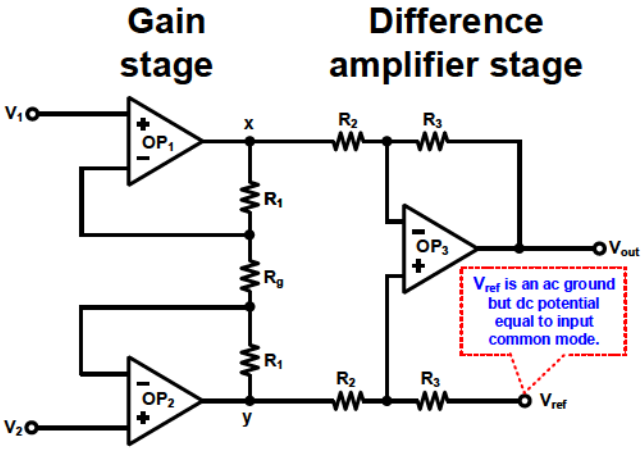

Fig. 3 Conventional three Op-amp IA

The differential and common mode gain of the amplifier given in equations (1) and (2) respectively:

$$\frac{V_{out}}{V_1 - V_2} = \frac{R_3}{R_2}\left(1 + \frac{2R_1}{R_g}\right) \quad (1)$$

$$\frac{V_{out}}{V_{cm}} = \frac{1}{2}\frac{R_2 + R_3}{R_2 - R_3} \quad (2)$$

This Conventional three Op-amp IA is very popular design due to:

1. High input impedance and both input signals feeding the non-inverting terminals, hence there is no asymmetry in the impedance from the electrode side.
2. A simple way to control the gain is by varying the R_g, without needing to alter any other performance parameter significantly.

Despite the above mentioned advantages, the Conventional three Op-amp generally exhibit some drawbacks and limitation. Considering the integrated option rather than the discrete components.

1. Resistors occupy 70% of the silicon chip area, compared to the IC amplifiers. The second stage CMRR relies on resistors matching. Thus, to achieve high CMRR, the resistors must be accurate enough to reduce the common mode gain, usually by increasing the resistor area [4]. Detailed analysis of the CMRR is given in Appendix-I.
2. A typical op-amp has an offset voltage of ~1mV but an applied signal to the IA are in the order of 10uV. In that case the signal may be buried under the offset voltage and hence it could be irrelevant to total offset voltage of IA. The effect of the Op-amp offsets at the IA output can be expressed as follows:

$$V_{out} = \frac{R_3}{R_2}\left(1 + \frac{2R_2}{R_g}\right)(V_{OSP1} - V_{OSP2}) \pm \left(1 + \frac{R_3}{R_2}\right)V_{OSP3} \quad (3)$$

   where V_{OSP} is the offset of each Op-amp.

3. The Conventional three Op-amp IA with several large resistors in the signal path exhibits a relatively high noise. Additionally, it requires a moderately high dynamic range, which requires dynamic element matching (DEM) techniques.
4. The modern sub-micron technology requires a low power supply voltage (V_{dd} of 1.5V max). Given that the first stage has a high gain nodes x and y which could reach the supply rails and hence limit the maximum signal applied to the signal noise ratio (SNR). This may not be the problem for sensor applications, where the input common mode is closer to the mid-rails, but there is no guarantee of mid-rail

common-mode voltage due to the electrode offset and impedance uncertainty in the present application.

5. The circuit output common-mode is same as input common-mode voltage; this is not acceptable in many applications. In order to shift the output common-mode voltage relative to input common mode, splitting the resistor R_g (Fig. 1) into two parts and DC bias with a separate resistor would work but increases the flicker noise of the amplifier due to the DC current through the resistors.

There have been several attempts to improve the performance of the conventional three Op-amp IA in recent publications, which has helped to overcome some of the limitation mentioned above. An indirect current feedback-based IA has been proposed, which uses only 3 resistors [4]. The indirect current feedback architecture demands high power consumption due to the wideband requirement of the gm cells. This has additional stability issues with global negative feedback and noise. [5] Proposed chopper stabilization based low offset IA, requires a very low cut-off frequency filter, which occupies a lot of area. [6][7] [12] presented several low-voltage architectures but they haven't addressed the input and output common-mode problem described above. None of the proposed IA's addressed the tight resistor-matching requirement and low voltage requirement.

3. Proposed Instrumentation Amplifier: The motivation for the proposed architecture is to minimise the voltage swing at node x and y. In the conventional IA circuit input the voltage signal is amplified at those nodes so that they will be closer to the supply. Therefore; converting the input voltage into current, through a V2I converter, would lead to minimizing the dynamic range limitation [9] [10]. The converted current is amplified through the current mirror, as well as through the trans-impedance amplifier to convert the amplified current into voltage, to drive the circuit by the IA.

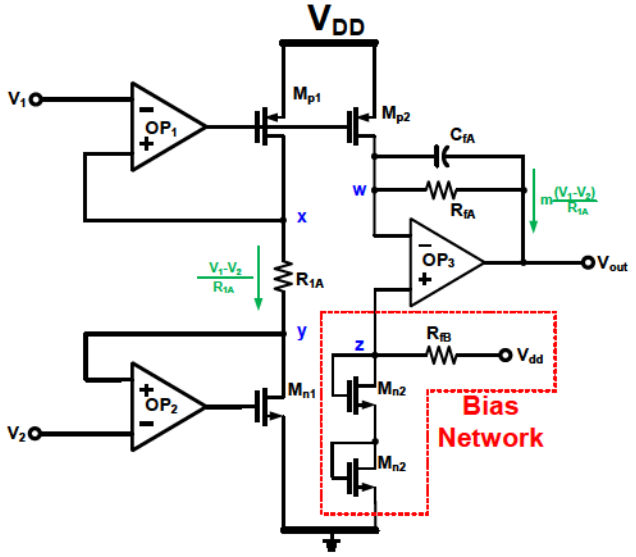

Fig. 4 Proposed trans-impedance IA

Fig. 4 shows the proposed current-mode amplifier with Op_1 and M_{p1} acting as V2I converters and produce a current proportional to the input voltage. In a similar way O_{p2} and M_{n1} act as V2I converters and produce a current proportional to the input voltage. In the process of V2I conversion, x and y potentials do not swing more, compared to the conventional IA. Instead they will swing the same as the input swing, hence there would be no dynamic range limited gain. O_{p3} and R_{fA} forms a trans-impedance amplifier (TIA) to convert M_{p2} current into voltage. As a design trade off, one could use some amplification in the current mirror formed by the M_{p2} and M_{p1} so that R_{fa} value can be reduced to relax the TIA open loop-gain, hence stability. The output voltage can be expressed as:

$$V_{out} = -m\frac{R_{fA}}{R_{1A}}(V_1 - V_2) \tag{4}$$

where m is the size ratio of M_{p2} and M_{p1}.

The output common mode is decided by the dc potential of the non-inverting terminal (node-z). In this current proposal, we use a simple bias circuit, which consists of M_{n2} and R_{fb}. The potential of Node Z is kept closely to the mid rail as shown in Fig. 4. However, the role of the bias circuit is to provide appropriate common mode voltage to OP_3, so any other bias circuit works properly as long as it provides required common mode and present proposal works with any bias circuit. There is no conflict between the input and output common mode in the new architecture design which is a significant improvement. Hence, the output common-mode voltage of this circuit is independent of the input common-mode voltage. In the conventional IA, the difference amplifier loop-gain will be $(A_{OP3})(R_2/(R_3+R_2))$, where A_{OP3} is the DC gain of the op-amp OP3. Given the DC accuracy requirement is typically 0.01%, a specific loop-gain is necessary so that OP_3 would need to be designed for higher DC gain and bandwidth. Whereas, in the proposed IA, the final stage loop-gain is simply defined by the op-amp gain, since it is a trans-impedance amplifier. Assuming r_0 of M_{p2} is very high compared to R_{fA} (**typical case**), the op-amp gain requirement is far less than that of the current mode IA; a typical value would be of a minimum 6dB. In case of traditional IA, the first stage has an unity common-mode gain, whereas in the proposed new design IA, it is very low because common mode voltage influence will be suppressed due to V2I conversion (means M_{p1} current will be independent of the input common mode voltage).

Input refereed noise of the circuit is very critical while processing the very weak signals. Spectral density of the thermal noise and flicker noise of the transistor current can be expressed as follows:

$$I^2_{Thermal} = 4KTY g_m \tag{5}$$

$$I^2_{Flicker} = \frac{Kg^2_m}{WLC_{ox}}\frac{1}{f} \tag{6}$$

The major noise contributors in the proposed circuits are OP_1, M_{p1}, M_{p2} and R_{fA}, whereas the OP_3 noise contribution is minimal because of the higher forward gain in the chain. The noise contributed by M_{p2} at the output is given by:

$$V^2_{mp1} = \frac{4KTY g_{mp1}}{(1+A_{op1}g_{mp1}R_{1A})^2}(m g_{mp2}R_{fa})^2 \tag{7}$$

The noise contributed by Mp2 at the output is given by:

$$V^2_{mp2} = 4KT g_{mp2}R^2_{fa} \tag{8}$$

The noise contribution of R_{fa} is given by:

$$V^2_{Rfa} = 4KTR_{fa} \tag{9}$$

The total input referred noise can be expressed as:

$$V^2_{inp} = \frac{V^2_{mp1}+V^2_{mp2}+V^2_{Rfa}}{\left(m\frac{R_{fa}}{R_{1a}}\right)^2} \tag{10}$$

Input refereed offset of the IA is dominated by the front-end buffer amplifiers Op_1 and Op_2, thus the only way to improve it is by building the op-amps with inherently low noise.

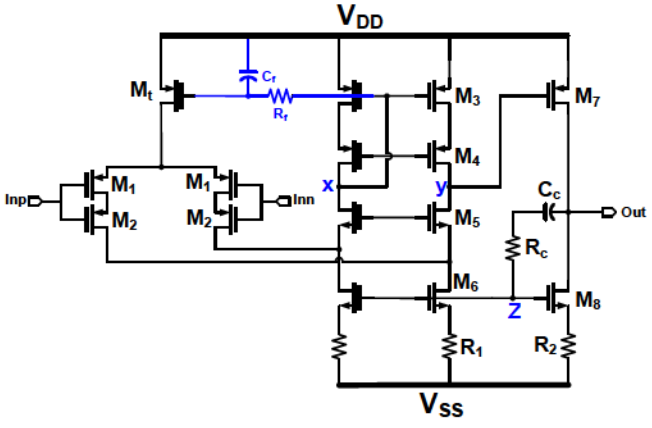

Fig. 5 Self-Bias opamp (Op1/2) Schematic used in IA

4. Op-amp design: To meet typical 0.01% accuracy requirement at the output, the minimum op-amp DC gain requirement is 80dB. Nevertheless, by including the non-idealities parameters such as bandwidth limitation and component mismatching, thus, the practical gain requirement is ~82dB. We have chosen two stage op-amps with the first stage as the folded Cascode op-amp for rail to rail input operation and common source amplifier as second stage. The op-amp schematic circuit is shown in Fig.5. To reduce the input referred noise, a self cascode input stage is introduced, where M_1 forms the differential pair with M_2 as a degeneration resistor since it is in the triode region. The folding cascode transistor M_6 would generate more noise due to the high current flow, so used a resistive degeneration R_1 to minimize the it's noise contribution to overall IA. To avoid the bandgap requirement and to minimise the offset drift with temperature, op-amp tail current source and cascode loads have been biased through the self-bias feedback loop [11]. When the op-amp configured in the feedback (fig. 5), the first-stage output and mirror node-x will settle to an appropriate bias voltage depends on the current requirement, so used this node to bias the tail current source hence systematic offset voltage will be minimized significantly.

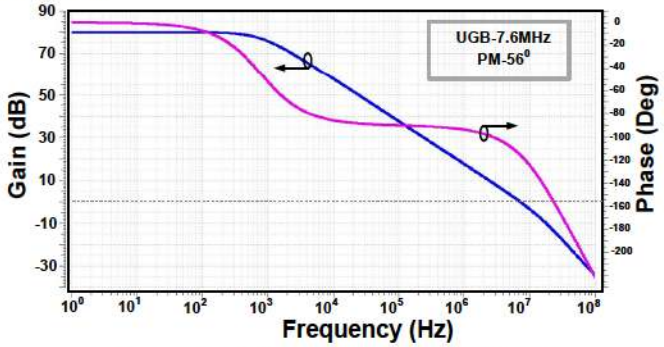

Fig. 6 Simulated frequency response of the OP_1-Loop

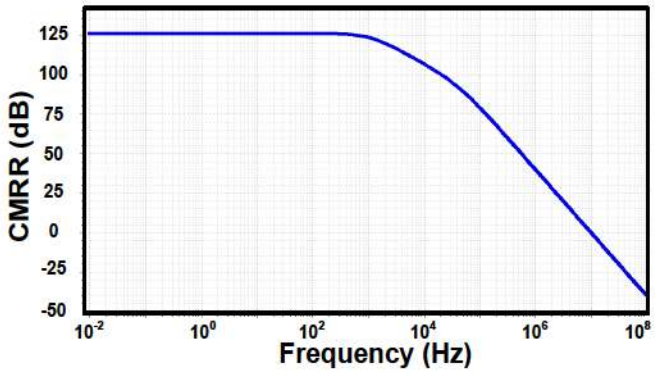

Fig. 7 Simulated CMRR of the IA

Self-bias works when the external feedback loop is rapidly faster than the self-bias. This is achieved by using RC low pass filters, formed by R_f and C_f, to slow down the bias loop. A start-up circuit is required to push the opamp out of zero current operating point, hence a standard circuit has been used [11]. For the well-behaved transient response, adopted Miller compensation with RH zero cancellation resistor (R_c). gm/id methodology has been used to fix the device sizes, gm/id ratio of 18 for the differential pair and gm/id ratio of 7, for the cascode current mirrors, to minimize the input referred offset. When the op-amp is connected in the IA architectural configuration (as shown in Fig. 4), the feedback loop is equivalent to three stage op-amp loops, thus, the compensation is very challenging [8]. Therefore, a nested Miller style of compensation technique is introduced. One compensation capacitor connected across the 2nd stage with the right half zero (RHZ) cancellation resistor and another compensation capacitor is connected between the amplifier first stage output node z and IA node x (as shown in Fig. 4) [13]. Fig. 6 shows the simulated frequency response of the Op-amp, which illustrate a 56^0 phase-margin and 7.6MHz unity gain frequency. OP_3 is a Miller-compensated two stage simple amplifier with NMOS input differential pair. Since OP_3 noise and offset are reduced by the first stage amplifier OP_1, its contribution to the overall amplifier is less than ~3.5% (from the noise contribution analysis). The overall loop has 60^0 phase margin. To achieve this phase margin (over-damped loop dynamics), a small compensation capacitor C_{fa} across the feedback resistor is introduced, which basically creates a zero in the loop-gain transfer function and helps for the stability.

5. Results: The proposed IA has been implemented in 65nm CMOS technology. The new proposal has a high CMRR of (greater than 120dB), thus a substantial improvement in the CMRR has been achieved. Fig. 7 shows the simulation of the CMRR vs. frequency characteristic for the new proposed design. To evaluate the IA performance under a small differential mode signal and a large common mode signal, a 0.2mV typical ECG signal with a 100Hz, 50mv common signal has been applied as shown in the Fig. 8. The top trace shows that the input signal and the output is an 80mV signal and there are no traces of the 50Hz common mode. Fast Fourier Transform (FFT) of the output confirms that the CMRR of the proposed amplifier.

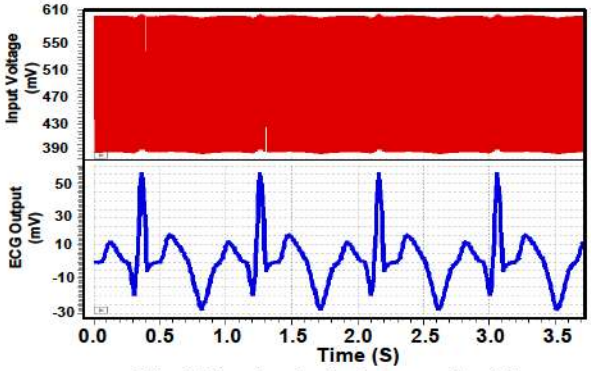

Fig. 8 Time-domain simulation results of IA

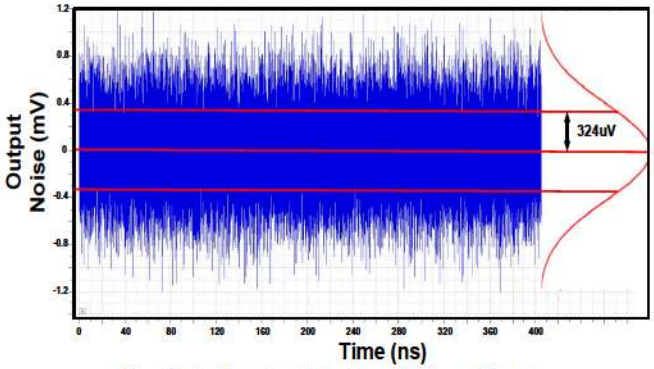

Fig. 9 Simulated output referred Noise of the IA

Fig. 9 shows the output referred noise of the IA. Without any input signal applied, a standard transient noise simulation carried out in Cadence, found the 1-Sigma RMS voltage noise at the output to be 0.324mV, referring this to input results in 0.81uV input referred RMS voltage.

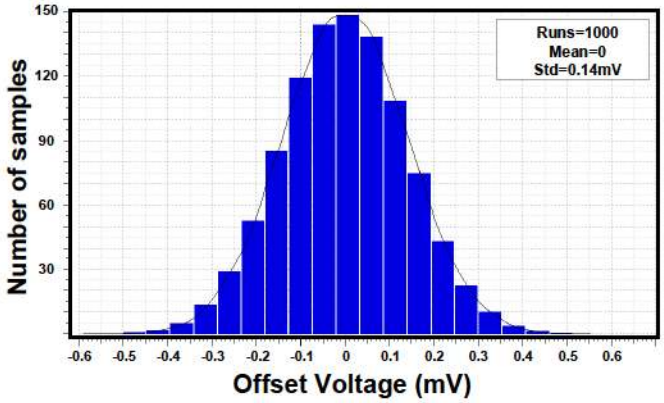

Fig. 10 Simulated input referred offset.

Fig. 10 shows the histogram of the input referred noise under slow corner and cold temperatures. A RMS 140uV was achieved with 1000 Monte-Carlo simulations. The distribution seems to be close to the Gaussian, so 99.97% of the circuits will have offset between $\pm 3\sigma$. Table-I lists the transistor as well as the passive component sizes used in the design. Table-II shows the performance summary of the proposed IA. Fig. 11 shows the simulated layout of the proposed IA, occupies 4500um^2 active area.

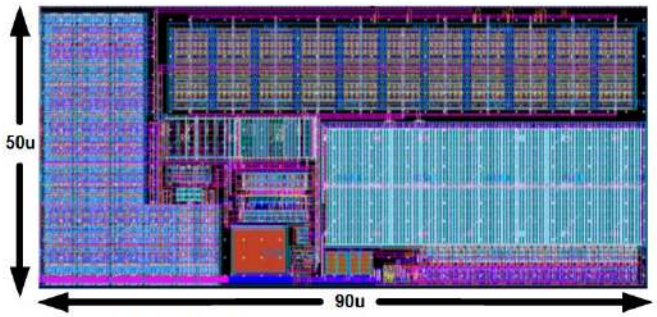

Fig. 11 Simulated Layout of the proposed IA

TABLE I Component dimensions used in the Proposed Design

Component Name	W/L (um/um)	Component Name	W/L (um/um)
M_t	96/1.8	M_{p1}	24/1.8
M_1	48/1.8	M_{p2}	96/1.8
M_2	48/1.8	M_{n1}	16/2
M_3	24/1.8	M_{n2}	8/1
M_4	6/0.45	R_{1A}	2.5K
M_5	16/1	R_{fA}	250K
M_6	32/2	C_{fA}	432f
M_7	48/1.8	R_{fB}	46K
M_8	64/2		
R_1	12.5k		
R_2	6.25K		
R_C	18K		
C_C	280f		

TABLE II Performance Summary

Parameter	Value	Units
Gain	52	dB
CMRR	123	dB
Integrated Noise	0.81	uV
Offset Voltage	0.14	mV
Input common Mode range	0.025-1.65	V
Output common Mode Range	0.1-1.72	V
Temperature range	-40 to 125	^{0}C
Power Supply	1.8	V
Power dissipation	464.4	µW
Technology	65	nm
Area	4500	µm^2

6. Conclusions: In this paper, a novel area efficient instrumentation amplifier has been presented. The new amplifier relies on a voltage to current conversion on the first stage, with a view to improve the dynamic range and current to voltage conversion on the second stage. This circuit allows different common mode voltages at the input and output, unlike the conventional circuit design. A 65nm CMOS technology-based prototype has been developed and simulation results showed significant silicon area saving by relaxing the resistor tight matching requirement. Also, the architecture is not sensitive to the resistor mismatch anymore and achieved better CMRR.

R. Nagulapalli, K. Hayatleh, S. Barker, S. Zourob, N. Yassine, S. Raparthy and A. A. Tammam
(Faculty of Technology, Design and Environment, Oxford Brookes University, Wheatley Campus, Oxford, OX33 1HX, UK)
E-mail: khayatleh@brookes.ac.uk

Appendix-I

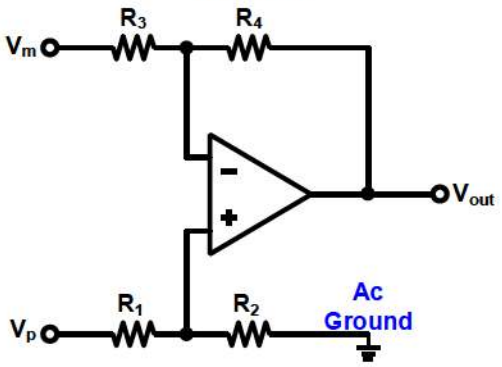

Fig. 12 Difference amplifier

Fig. 12 shows the difference amplifier. Assume all resistors are equal in value, such that it has unity differential gain. Let us say σ_R is the relative percentage mismatch between any two resistors ($\delta R/R$).
The output voltage can be expressed as:

$$V_{out} = V_p \frac{R_2}{R_2+R_1}\left(1+\frac{R_4}{R_3}\right) - V_m \frac{R_4}{R_3} \quad \text{(A1)}$$

Assuming each resistor has uncorrelated mismatch component, we can express each resistor as a sum of its mean value and deviation. Hence the expression:

$$\frac{R_4}{R_3} = \frac{R+\delta R_4}{R+\delta R_3} = 1 + \frac{\delta R_{34}}{R} \quad \text{(A2)}$$

Substituting (A2) in (A1) we can express the o/p as follows:

$$V_{out} = V_P\left(1+\frac{\delta R_{34}}{R} - \frac{\delta R_{12}}{R}\right) - V_m\left(1+\frac{\delta R_{34}}{R}\right) \quad \text{(A3)}$$

From (A3), we can deduce differential mode and common gain as follows:

$$A_{CM} = -\frac{\delta R_{12}}{R} \quad \text{(A4)}$$

$$A_{DM} = 1 - \frac{\delta R_{12}}{2R} + \frac{\delta R_{34}}{R} \quad \text{(A5)}$$

$$CMRR = \frac{A_{DM}}{A_{CM}} = \frac{1-\frac{\delta R_{12}}{2R}+\frac{\delta R_{34}}{R}}{\frac{\delta R_{12}}{R}} \quad \text{(A6)}$$

$$\approx \frac{R}{\delta R_{12}} \approx \frac{1}{\sigma_R} \quad \text{(A7)}$$

Hence CMRR depends on the matching between the resistors. For example – Imagine a unity gain difference amplifier to detect 1mV differential signal in CMOS process with 0.1% resistor mismatch. The objective is to find how much input common voltage (V_{CMI}) can be tolerated while detecting 1mV signal.

$A_{DM} = 1$ and A_{CM}=0.001 (from A4). Let us say input common mode is V_{CM}. Since the differential gain is unity and differential signal is 1mV, the output signal due to differential input is V_{ODM}=1mV. The output due to the common mode input (V_{OCM}) is 0.001*V_{CMI}. To detect without having any errors $V_{OCM} \ll V_{DCM}$, hence the input common mode should be much lesser than 1V to detect the 1mV signal. By using the factor of safety 10, we can say that the input common mode should be less than 100mV, which is very tight to design because all sensors output's common mode is above 1V.

Acknowledgement
The authors acknowledge and would like to thank Dr Bryan Hart for his valuable time and advice on the writing of this paper.

References

1. W. Wattanapanitch and R. Sarpeshkar, “A low-power 32-channel digitally programmable neural recording integrated circuit,” IEEE Trans. Biomed. Circuits Syst., vol. 5, no. 6, pp. 592–602, Dec. 2011.

2. M.-C. Cho, J.-Y. Kim, S. Cho, "A bio-impedance measurement system for portable monitoring of heart rate and pulse wave velocity using small body area", *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 3106-3109, May, 2009.

3.M. A. Smither, D. R. Pugh, L. M. Woolard, "CMRR analysis of the 3-op-amp instrumentation amplifier", Electron. Lett., vol. 13, no. 20, pp. 594, 1977.

4. B. J. van den Dool, J. H. Huijsing, "Indirect current feedback instrumentation amplifier with a common-mode input range that includes the negative rail", *IEEE J. Solid-State Circuits*, vol. 28, no. 7, pp. 743-749, Jul. 1993.

5. R. Wu, K. A. A. Makinwa, Johan H. Huijsing, "A chopper current-feedback instrumentation amplifier with a 1 mHz 1/f noise corner and an ac-coupled ripple reduction loop", *IEEE J. Solid-State Circuits*, vol. 44, no. 12, Dec. 2009.

6. S. J. Azhari and H. Fazlalipoor, "CMRR in voltage-op-amp-based current-mode instrumentation amplifiers (CMIA)", IEEE Trans. Instrum. Meas., vol. 58, pp. 563-569, 2009.

7. S. Luikitmongkol, W. Petchmaneelumka, V. Riewruja, C. Wangwiwattana, and A. Chaikla, "A Low-voltage CMOS Instrumentation Amplifier," SICE 2003 Annual Conference, Vol. 3, pp. 2995-2998, 2003.

8. R. Nagulapalli, K. Hayatleh, S. Barker, S. Zourob, A. Venkatareddy, "A CMOS technology friendly wider bandwidth opamp frequency compensation", *Electrical Computer and Communication Technologies (ICECCT) 2017 Second International Conference on*, pp. 1-4, 2017.

9. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, United Kingdom, 1998.

10. Hwang-Cherng Chow, Bing-Shiun Tang, Ji-Hong Tien, Wu-Shiung Feng, "A high performance current-mode instrumentation amplifier for biomedical applications", Signal Processing Systems (ICSPS) 2010 2nd International Conference on, vol. 2, pp. V2-64-V2-67, 2010.

11. V. Balan, "A low-voltage regulator circuit with self-bias to improve accuracy", *IEEE J. Solid State Circuits*, vol. 38, no. 2, pp. 365, Feb. 2003.

12.C. Toumazou and F. J. Lidgey, "NOVEL CURRENT-MODE INSTRUMENTATION AMPLIFIER", Electron. Lett., Vol. 25, no. 3, pp. 228-230, FEB 1989.

13. M.-H. Shen, L.-H. Hung, and P. Huang, “A 1.2 V fully differential amplifier with buffered reverse nested Miller and feedforward compensations,” in Proc. IEEE ASSCC, Nov. 2006, pp. 171–174.