A Novel Interface for Eddy Current Displacement Sensors

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Abstract—In this paper, we propose a novel interface concept for eddy current displacement sensors. A measurement method and a new front-end circuit are also proposed. The front-end circuit demonstrates excellent thermal stability, high resolution, and low-power consumption. The proposed idea is analytically investigated. The demodulation principle, as well as the interface implementation, is also addressed. This interface is being introduced for measuring submicrometer displacements in medium- to high-resolution applications. The interface system consumes less than 12 mW and has an extremely low thermal drift. The interface circuit will be implemented as a system-in-a-package (SIP). The full-scale range of displacement is 1 mm with 50-kHz signal bandwidth and 11-bit resolution (less than 500 nm). The signal conditioning circuit utilizes a standard 0.35-μm complementary metal-oxide semiconductor (CMOS) technology. Simulation results, which were achieved on the basis of experimental results of testing a prototype coil, also confirm the high performance of the interface system, as expected from analytical results. Compared with previous reports, this low-power interface system demonstrates a much lower temperature drift.

Index Terms—Displacement sensors, eddy current, low-power front-end, sensor interfacing, thermal drift.

I. INTRODUCTION

MEASURING displacement is an important demand in the sensors world. In addition to the direct measurement of displacement, displacement sensors are also utilized to detect other measurands such as pressure, acceleration, etc., which make the application range of this type of sensors very wide. Compared with other displacement sensors, eddy current displacement sensors (ECSs) have the advantage of being much less sensitive to a number of environmental variations [1]–[3].

The operating principle of an ECS is based on Lenz's law. Most often, ECSs are constructed in such a way that a sensing coil is placed in front of a metallic (conductive) target. When a metal target is present in a magnetic field and an alternating current is passed through the sensing coil, the electromagnetic induction causes a circular eddy current to flow on the surface of the target in a plane perpendicular to the magnetic field direction. The induced eddy current generates a magnetic field opposing the initial magnetic field. This phenomenon is usually

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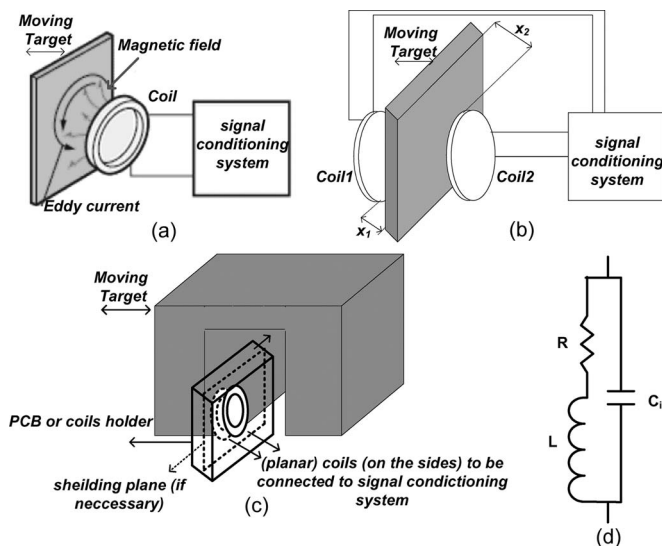
Fig. 1. Some ECS configurations. (a) Simplest configuration. (b) Two differential coils in both sides of a target. (c) Differential coils within a massive target. (d) Simplified model of an ECS probe [regarding (a)].

modeled as a mutual inductance, which appears between the coil and the target. The equivalent magnetic circuit is often presented by an air-core transformer such that the mutual inductance is related to the displacement [3]. Fig. 1 shows some possible configurations for the sensor head as well as a simplified electric model of an ECS. In the simplified model in Fig. 1(d), the equivalent inductance and resistance are functions of displacement, working frequency, and geometric parameters of the sensor head and target [3]. The following expressions present the equivalent inductance and resistance as functions of R_c, L_c, and R_t, L_t:

$$R = R_c + \frac{(2\pi f)^2 M^2}{R_t^2 + (2\pi f L_t)^2} R_t \qquad (1)$$

$$L = L_c + \frac{(2\pi f)^2 M^2}{R_t^2 + (2\pi f L_t)^2} L_t \qquad (2)$$

where R_c, L_c, and R_t, L_t, are related to the geometric dimensions of the coil and target, respectively; f is the frequency of the excitation signal; and M is the mutual inductance between the coil and the target (if the distance x between the target and the coil increases, then M drops [10]).

The effect of the resistor R in the measurement can be reduced by choosing proper sizes for the target and the coil [2]. For coils with a small number of wire turns, the parasitic interwinding capacitance C_i is negligible. Therefore, the sensor head impedance can be described as a variable inductor.

Fig. 2 shows a setup [with respect to the architecture shown in Fig. 1(b)] including two differential coils and a target in
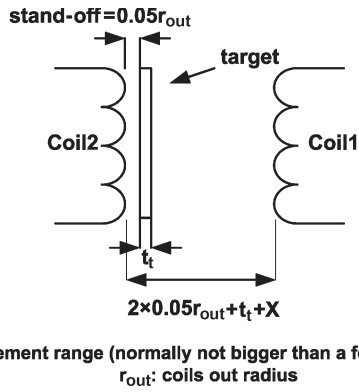
Fig. 2. Typical setup for the sensor head with differential coils based on the scheme presented in Fig. 1(b).
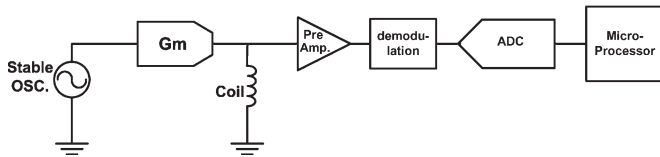

Fig. 3. ECS signal conditioning by applying a constant-frequency oscillator and utilizing a Gm block and an ADC.

between. As a rule of thumb, the displacement range should be maximum 1/2 to 1/3 of the coil diameter [4]. The target stand-off is usually considered $0.05r_{out}$, where r_{out} is the coil external radius [20].

Many different approaches have been introduced in the literature to explain how to design coils, especially planar coils. In the case of using planar coils, the approach introduced in [11] is recommended to be applied when designing the coils.

Fig. 3 shows a block diagram of a typical ECS interface using an external oscillator. In this approach, the amplitude of the voltage over the sensor coil is of interest. In other words, the baseband signal (usually a few tens of kilohertz bandwidth), which carries the displacement information, modulates the excitation frequency (i.e., amplitude modulation). The excitation frequency should be high enough (usually a few megahertz) to reduce the skin depth δ (δ^2 is inversely proportional to the frequency). As a result, in this architecture, we have at least three high-frequency blocks: a reference oscillator, a $V–I$ converter (denoted as "Gm" in Fig. 3), and a demodulator. These blocks consume considerable power due to the large bandwidth requirement. Moreover, the signal conditioning system should be able to accommodate temperature variations, which result in increased design complexity and increased power consumption for low-temperature drift applications [5], [6].

There are applications that require high sensor performance with respect to resolution, measurement speed, stability, and reliability, where the performance has to be achieved with very limited power consumption (e.g., in satellites) and/or with limited means for removing the generated heat (e.g., in a vacuum environment). These application requirements lead to the need for a high-performance electronic interface system that also has to be low power and robust to accommodate temperature variations. Therefore, power efficiency and low thermal drift are our main objectives in the presented interface system.
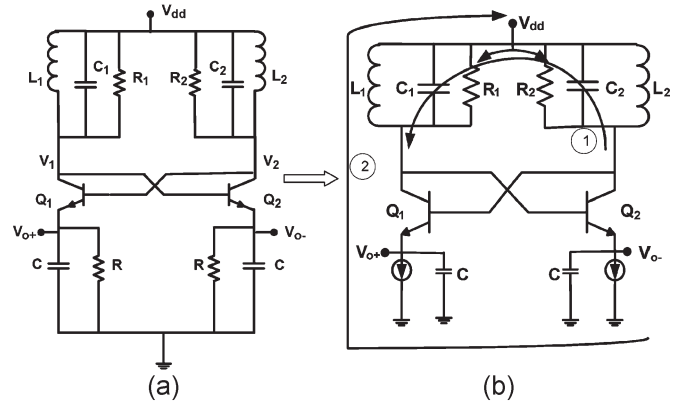

Fig. 4. Front-end stage for the ECSs proposed in [7]. (a) Circuit diagram. (b) Same circuit with ac current loops.

In [12], the basic concept of a low-power low-thermal drift interface for ECSs has been introduced and discussed. In this paper, we continue the discussion based on an in-depth analysis, extended simulation results, as well as design proposals for the adaptive level distinguisher (ALD) block and the architecture of the operational amplifier.

First, we present a self-oscillating front-end circuit to convert displacement to voltage with low-power consumption. In Sections III and IV, a low-power signal conditioning method, which is compatible with the front-end stage, is proposed. Finally, a system implementation is presented in Section V, which is completely suitable for medium- to high-resolution demands in submicrometer displacement applications. Simulation results confirming the analytical discussions are also presented in Section VI.

II. FRONT-END STAGE DESIGN

The front-end proposed in this paper can be compared to the front-end presented in [7], which is a simple self-oscillating front-end stage for ECS interfacing [see Fig. 4(a)]. For the sake of good comparison, before introducing the proposed interface, first, we shortly analyze the solution presented in [7].

A. State of the Art

The reported ECS in [7] uses two differential coils to directly convert the target displacement into the baseband signal. This front-end stage can be used along with the sensor configurations shown in Fig. 1(b) and (c). By using two coils [see Fig. 1(b) and (c)], a differential construction can be realized with improved target displacement sensitivity. Such a circuit is interesting mainly because it is expected to consume a very low power (about 4–5 mW). This front-end stage presents a differential output, which delivers the displacement information.

One problem with the circuit is the oscillation instability. If we neglect the emitter-degenerating components, the open loop transfer function $T(s)$ can be presented as

$$T(s) = \frac{g_{m1}g_{m2}}{C_1 C_2} \cdot \frac{s^2}{\left(s^2 + \frac{1}{R_1 C_1}s + \frac{1}{L_1 C_1}\right) \cdot \left(s^2 + \frac{1}{R_2 C_2}s + \frac{1}{L_2 C_2}\right)}$$
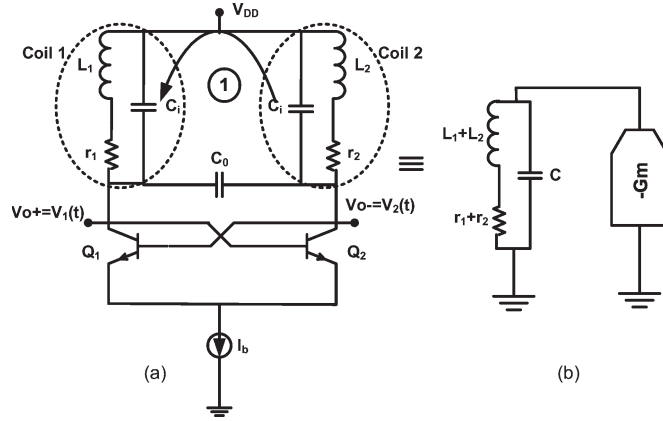
(3)

Fig. 5. Proposed front-end stage. (a) Schematic. (b) Equivalent ac model.

where R_i, C_i, and L_i are the values of the components depicted in Fig. 4(a), and g_{mi} is the transconductance of each transistor ($i = 1, 2$). Regarding the fact that $L_1 \neq L_2$ (except in the case when $x_1 = x_2$, i.e., $L_1 C_1 = L_2 C_2$), (3) reveals that we have two oscillation frequencies: $\sqrt{1/L_1 C_1}$ and $\sqrt{1/L_2 C_2}$. Therefore, it is hardly possible for such a circuit to have a stable oscillation for a wide variation range of L_1 and L_2.

Next to the oscillation instability, another important problem with this front-end stage is the high-temperature drift. The emitter-degenerating components together with the base–emitter junctions of the transistors perform amplitude detection. If we substitute the two resistors at the emitter terminals with current sources, as shown in Fig. 4(b), and assume that $V_1 \cos(\omega_c t)$ and $V_2 \cos(\omega_c t)$ are signals applied to the base terminals of the transistors (where $\omega_c = 2\pi f_c$, with f_c being the working frequency), then the differential output voltage can be obtained as [8]

$$V_{o,\text{diff.}} \approx V_1 - V_2 - V_T \ln \sqrt{V_1/V_2} \qquad (4)$$

with

$$V_T = KT/q \qquad (5)$$

where K is Boltzmann's constant, T is the temperature, and q is the charge of an electron. Equation (4) reveals that the temperature error is modulated by the value of the input signal and is very difficult to compensate for, even with very accurate temperature measurements. The real temperature sensitivity of this circuit [7] is even higher when we take into account the temperature dependence of V_1 and V_2. Their temperature dependence is due to the fact that the transistor's transconductance g_{mi} is a function of temperature. Based on our experimental observations, such a front-end [7] introduces thousands of ppm/°C thermal drift.

Fig. 4(b) shows the main ac current directions in the circuit shown in Fig. 4(a), which is helpful for analyzing the front-end stage. In this circuit, because of the low impedance of capacitors C at the oscillating frequency, a significant ac current appears in direction 2.

B. Proposed Front-End Stage

Fig. 5(a) depicts the proposed front-end stage [12]. Figs. 4 and 5 show the conceptual difference between the proposed

front-end stage and that in the previous art. Let us have a closer look at Fig. 5(a). Such a circuit is commonly used as a current-biased LC cross-coupled oscillator for radio frequency (RF) applications. However, in RF applications, the coils/capacitors have equal values. Obviously, in this circuit, the current source I_b creates a high-ac impedance from the emitter terminals of the transistors to the ground node. Therefore, if we assume two current directions in Fig. 5(a), just as in Fig. 4(b), the ac current, which flows in direction 2, is zero. Consequently, the supply voltage branch acts as a grounded branch with zero ac current (similar to an ac virtual ground). Hence, it is possible to assume that the coils are in series in ac mode. An equivalent model is depicted in Fig. 5(b). At system-level design, regarding the model depicted in Fig. 5(b), the proposed oscillator plays the role performed by the three blocks depicted in Fig. 3: oscillator, G_m, and coil(s). If the model in Fig. 5(b) is taken into consideration, then the oscillation frequency is obtained as

$$\omega = \sqrt{1/LC - (r/L)^2} \qquad (6)$$

where $L = L_1 + L_2$, $C = C_0 + C_p$, and $r = r_1 + r_2$. C_p is the equivalent parasitic capacitor that is in parallel with C_0. C_p includes the coils' parasitic capacitors and the parasitic capacitors of the junctions of the transistors. In case of utilizing a typical off-chip planar coil, C_p is about 1 pF.

In this front-end stage, the variation of the oscillation frequency is limited because $L_1 + L_2 \approx$ const. (particularly in the linear region of inductance versus displacement curve).

This circuit is very suitable for ratio-metric measurement because the same ac current passes through both coils. Fig. 6 illustrates the simulation result for the output voltages $V_1(t)$ and $V_2(t)$ in the case that C_0 is around 1 nF. The intention for the final realization is to use a system-in-a-package (SIP) solution such that the front-end stage uses discrete components, while the rest of the interface system is integrated.

III. MEASUREMENT METHOD

In the measurement systems, a ratio-metric function is typically utilized to suppress multiplicative errors. As seen in Fig. 6, the output voltage ratio depends on the values of the inductances. This figure confirms that the ratio of the voltages ($(V_{o-}/V_{o+}) \approx (192.6/320.5)$) is roughly the same as the inductances' ratio (≈ 0.6).

If the output voltages are first amplified and then applied to an analog-to-digital converter (ADC), the ratio-metric function $(\mathbf{V_1} - \mathbf{V_2})/(\mathbf{V_1} + \mathbf{V_2}) = ((\mathbf{V_1}/\mathbf{V_2}) - 1)/((\mathbf{V_1}/\mathbf{V_2}) + 1)$, which eliminates the multiplicative errors in the measurement, can be formed in the digital domain. One important source of temperature drift is the coils' current, which is a multiplicative factor. For simplicity, we focus on V_1/V_2 as the core function of the ratio-metric measurement. Since the supply voltage branch has zero ac current, we have

$$|V_1/V_2| = |y_2 I/y_1 I| = |y_2/y_1| \qquad (7)$$

where y_1 and y_2 are the admittances of the coils, and I is the coils' loop current. Note that any drift coming from the term I is omitted in the measurement function. Typically, the parasitic
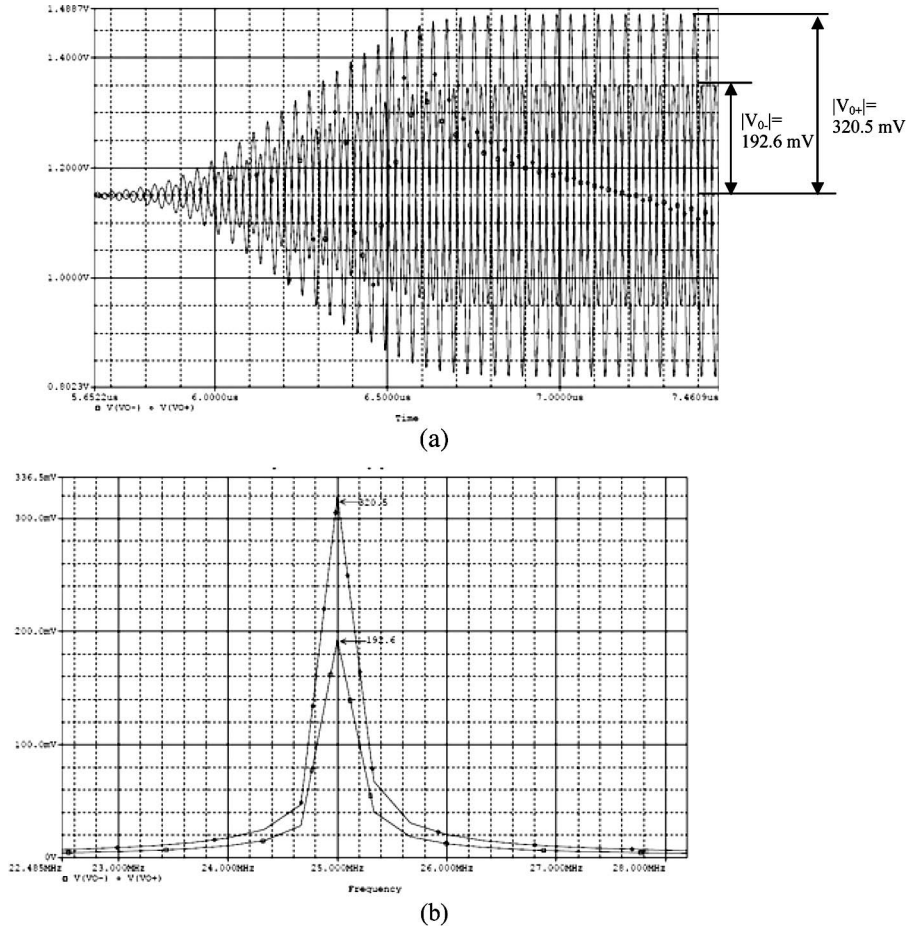
Fig. 6. Simulation results for the oscillator outputs with the experimental values of the components. (a) In time domain, showing the transient behavior of the oscillator. (b) FFT curve confirming the oscillation stability $[L_1 \approx 25$ nH, $L_2 \approx 15$ nH, $(L_2/L_1) \approx 0.6]$.

capacitor, which is in parallel with the coil [see Fig. 1(d)], is small enough to be neglected. As far as this parasitic capacitor is negligible, increasing the working frequency $f = \omega/2\pi$ results in $|V_1/V_2|$ tending to L_1/L_2, which is the ideal case. From (7), assuming finite values for f and that the parasitic capacitor is small enough to be neglected, we can derive

$$\left| \frac{V_1}{V_2} \right| = \frac{L_1}{L_2} \cdot \sqrt{\frac{1 + Q_1^2}{Q_1^2} \bigg/ \frac{1 + Q_2^2}{Q_2^2}} \tag{8}$$

where $Q_1 (= L_1\omega/r_1)$ and $Q_2 (= L_2\omega/r_2)$ are the quality factors of the coils. Therefore, the thermal drift of the measurement function caused by variations of ω is obtained as

$$\partial \left| \frac{V_1}{V_2} \right| \bigg/ \partial T = \frac{\partial |V_1/V_2|}{\partial \omega} \cdot \frac{\partial \omega}{\partial T}. \tag{9}$$

Expression (9) can be rewritten as

$$\frac{\partial \left| \frac{V_1}{V_2} \right|}{\partial T} = \left(\frac{\partial \left| \frac{V_1}{V_2} \right|}{\partial Q_1} \cdot \frac{dQ_1}{d\omega} + \frac{\partial \left| \frac{V_1}{V_2} \right|}{\partial Q_2} \cdot \frac{dQ_2}{d\omega} \right) \frac{\partial \omega}{\partial T} \tag{10}$$

where $(i = 1, 2)$ and

$$\frac{dQ_i}{d\omega} = \frac{L_i}{r_i} \tag{11}$$

and $(\partial |(V_1/V_2)|/\partial Q_i)$ is derived from (8). Hence

$$\frac{\partial \left| \frac{V_1}{V_2} \right|}{\partial T} = \frac{L_1}{L_2} \cdot \left(1 + \frac{1}{Q_1^2} \right)^{-\frac{1}{2}} \cdot \left(1 + \frac{1}{Q_2^2} \right)^{-\frac{1}{2}}$$
$$\times \left[\frac{1}{Q_2^3} \cdot \frac{1 + \frac{1}{Q_1^2}}{1 + \frac{1}{Q_2^2}} \cdot \frac{L_2}{r_2} - \frac{1}{Q_1^3} \cdot \frac{L_1}{r_1} \right] \cdot \frac{\partial \omega}{\partial T}. \tag{12}$$

For simplicity, this can be written as

$$\frac{\partial \left| \frac{V_1}{V_2} \right|}{\partial T} = k \cdot \frac{\partial \omega}{\partial T} \tag{13}$$

where k is calculated from (12). Note that in (12), $Q_i > 1$, and $L_i/r_i \ll 1$ s$(i = 1, 2)$. These facts, along with the minus sign in the bracket, guarantee that k is much smaller than 1. From (13), a very small k results in the temperature drift of the measurement function being much smaller than that of the frequency. For deriving (13), we assumed that the coils have been in series. In reality, due to the fact that the current source does not have infinite impedance, some temperature drift still remains, although it is considerably suppressed. In other words, (13) demonstrates that the applied measurement method can significantly suppress the existing temperature drift. For instance, in an extreme case, a 150-ppm/°C thermal drift for the

frequency results in less than 24-ppm/°C thermal drift for the ratio-metric function.

Another disturbing factor in measurement systems is the power supply drift. This oscillator works in the current-limited regime. Therefore, the stability of the output signal amplitude mainly depends on the stability of the bias current, which can be kept significantly independent from the power supply voltage and the temperature drifts by means of band-gap references [14]. The power supply voltage drift appears as a common-mode drift of the output voltages, which can considerably be suppressed by utilizing differential schemes.

What we have discussed so far can also be generalized for oscillators based on MOS transistors.

IV. DEMODULATION ASPECTS

The coils used in the ECS need to be excited by an excitation signal with a much higher frequency than the signal bandwidth of the input (displacement) signal. To separate the two signals (excitation and input signal), a demodulation technique should be applied. In this section, we discuss the applied demodulation approach.

A. Ratio-Metric Measurement and Demodulation

In [15], some methods for demodulating an AM-modulated signal are discussed. Demodulating a relatively high-frequency signal with low-power consumption (less than a few milliwatts) is a challenge. The main reason is the need for wide-bandwidth circuits, which consume considerable amounts of power.

The front-end oscillator has two outputs. These outputs have the same carrier frequency. By using the ratio-metric approach, we can automatically demodulate the signals without applying a special demodulation technique, as can be seen from

$$\frac{V_1(t)}{V_2(t)} = \frac{m_1(t)\cos(\omega_c t)}{m_2(t)\left(-\cos(\omega_c t)\right)} = -\frac{m_1(t)}{m_2(t)} \qquad (14)$$

where ω_c is the carrier frequency, and $m_i(t)$ is the baseband signal.

This fraction is useful for every moment of time (except zero crossings). Therefore, if we simultaneously obtain samples from the voltages, then we have

$$\frac{V_1(n)}{V_2(n)} = \frac{m_1(n)\cos(\omega_c n)}{m_2(n)\left(-\cos(\omega_c n)\right)} = -\frac{m_1(n)}{m_2(n)} \qquad (15)$$

where $n = pT_s$ $(p = 1, 2, 3, \ldots)$, T_s is the sampling period, and $m_i(t)$ is the baseband signal including displacement information [see Fig. 8(a)]. T_s is selected in such a way that certain required conditions like allowed measurement time are fulfilled. The first benefit of the proposed interface system is its compatibility with circuits utilizing switched-capacitor (SC) signal processing. Such circuits are accurate and easy to integrate.

In this approach, the power dissipation of the demodulation operation in the analog domain can be saved because demodulation occurs in the microprocessor (i.e., in the digital domain with considerably lower power) by utilizing the ratio-metric

function. This work can only be done at the cost of sampling high-frequency voltages. Therefore, a clock pulse with a small fall time for sampling and highly conductive switches for the sampling stage are needed. However, these requirements are not considered big constraints in deep submicrometer complementary metal-oxide semiconductor (CMOS) technologies that are capable of very fast switching operations.

B. Noise Considerations

For demodulation, taking samples around the voltage peaks is the logical choice. Doing so leads to a higher signal-to-noise ratio (SNR). Another important benefit of this is an improved immunity to the phase noise. This can be explained in the following way. First of all, we should mention that the injected noise is considerable only when the transistors in the oscillator are in their active region [13]. Suppose we utilize MOS transistors. Based on the general theory of oscillator noise explained in [17], if a noise impulse is injected at zero-crossing points, then it only affects the oscillation phase. The injected noise impulse at voltage peaks only affects the oscillation amplitude. Around zero-crossing points, over a short window of time, both of the cross-coupled transistors are in the saturation region [13]. Therefore, both transistors in this time frame inject noise into the tank causing uncertainty mainly for the oscillation phase (in other time intervals, including the voltage peaks, one transistor is in the triode region, while the other one is in the cutoff region. Therefore, at these moments of time, the cross-coupled transistors do not inject considerable noise into the LC tank). Thus, the peak voltage, which is of interest to this application, is not significantly affected by noise.

To consider phase noise, we show the oscillator differential output as follows [18]:

$$V_{\text{osc}}(t) = A\cos\left(\omega t + \phi(t)\right) \qquad (16)$$

where $\phi(t)$ is the phase noise. For small enough values of $\phi(t)$, as is here the case, we can rewrite (16) as

$$V_{\text{osc}}(t) \approx A\cos(\omega t) - A\phi(t).\sin(\omega t). \qquad (17)$$

Therefore, near the voltage peaks where $\omega t \approx 2l\pi$ or $(2l+1)\pi$ in (17), the second term, which includes the phase noise, is completely suppressed, and thus we have $(l = 0, 1, 2, \ldots)$

$$V_{\text{osc}}(t) \approx \pm A. \qquad (18)$$

Such a simple analysis can be applied to the oscillator single-ended outputs. In other words, if we assume $V_1(t) = A_1\cos(\omega t + \phi_1(t))$ and $V_2(t) = -A_2\cos(\omega t + \phi_2(t))$, then the terms $\phi_1(t)$ and $\phi_2(t)$ do not play a considerable role in the measurement approach, which takes care of the voltage peaks.

The dominant noise source in this measurement setup is the tail current noise, especially its $1/f$ component (see Fig. 7). A single-ended output voltage can be written as [13]

$$V_{\text{out},i} = \eta I_b R_i \qquad (19)$$

where η is the current-switching efficiency (which is practically 0.5–0.6), I_b is the bias current, and R_i is the single-ended tank
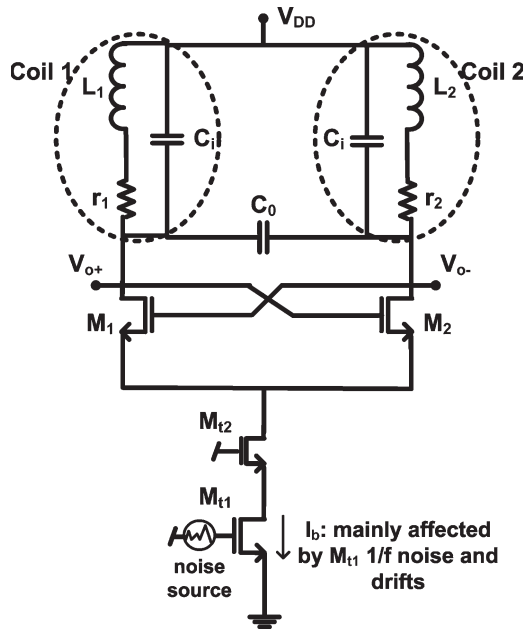
Fig. 7. *LC* oscillator with cascode current source utilized to improve the output impedance.

resistance, which is proportional to L_i. As can be understood from (19), the bias current, and hence its additive noise, appears as a multiplicative error in the product. Like temperature drift, as stated above, this noise can also be suppressed by simultaneously taking a couple of samples and then utilizing the ratiometric function.

As mentioned before, because a real current source has a limited output resistance, the ac current of the power supply branch is not zero. Thus, the effects of noise and temperature variations are not completely eliminated. Usually, for sinking high enough biasing current, M_{t1} is a large transistor. Moreover, to suppress the $1/f$ noise, using a large tail transistor is preferred. Therefore, it makes a large parasitic capacitor that lowers the output impedance of the current tail at high frequencies. To improve the output impedance, a cascode current source is utilized (see Fig. 7). It is worth noting that M_{t2} is much smaller than M_{t1}. Thus, compared with the case of only using M_{t1}, the cascode current source, including transistor M_{t2}, makes a smaller parasitic capacitor at the source-coupled point in the oscillator. The noise produced by M_{t2} is suppressed by M_{t1} and is, therefore, negligible [14].

V. SYSTEM IMPLEMENTATION

Fig. 8(b) shows a simplified circuit implementing the signal-conditioning method. The operating principle is as follows. In the first stage, the two input signals are sampled at voltage peaks by means of an adaptive level-distinguisher (ALD) block. The ALD turns off the sampling switches when the input signals are close to their peak values. Then, the sampled values are amplified according to the C_s/C_F ratio and applied to a two-channel ADC.

In the sampling stage, the first-order effect of signal-dependant charge injection is reduced by using the bottom-plate sampling technique.

Utilizing a simple MOS switch [instead of S_{bs} in Fig. 8(b)] in series with the input signal presents a residual signal-dependent charge injection (as a second-order effect) because the impedance seen from the drain side of S_1 [as shown in Fig. 8(b)] depends on the signal level. Alternatively, in addition to presenting a proper conductivity, a bootstrapped switch has considerably constant on-resistance, which does not significantly relate to the input voltage (although such a switch has a design complexity). Consequently, using bootstrapped switches can reduce the residual signal-dependent charge injection. Here, the design of the bootstrapped switches is based on the methodology proposed in [9]. Moreover, utilizing these kinds of switches can keep the total harmonic distortion (THD) constant and low enough for different input voltage amplitudes, which improves the accuracy of the measurement. In this design, the maximum THD variation for changing the input signal from its minimum to its maximum amplitude values in the first sampling stages, utilizing bootstrapped switches, is less than 32 ppm, which is based on the simulation results.

Taking samples close to the voltage peaks both improves the SNR and relaxes the constraint of fall time of the sampling clock pulse. Since the signal changes around the peaks are small (derivative closes to zero), the time required (i.e., the fall time of the clock pulse) to turn off the sampling switches (S_1/S_2) can be relaxed. Matching considerations for the switching transistors must be taken into account.

The ALD compares the oscillator output signal with a reference voltage that is adaptively generated by a peak detector. As soon as the output voltage of the oscillator becomes comparable with the output of the peak detector, there is a suitable time for turning off S_1 and its counterpart in the other channel (the bootstrapped switches are turned off shortly thereafter). This operation is performed every T_s.

To suppress the effect of offsets and low-frequency noise, an auto-zero technique on the system level is applied under the control of the microprocessor. To accomplish this, the front-end track-and-hold (T/H) stages are connected to a reference voltage at the rate of a few kilohertz. The processor saves and subtracts the result of this phase from the input signals results [for simplicity, this function is not shown in Fig. 8(b)].

A. ALD Architecture

Finding a sampling moment located very close to the peaks is a power-consuming task. The straightforward way is to use a continuous-time comparator to compare the oscillator output with a threshold voltage close to the peak values. Suppose that the window height in Fig. 8(a) is 10 mV, the full-scale voltage is 500 mV, and the oscillation frequency is 25 MHz. These assumptions reveal that the window length is about 2.5 ns. Therefore, our continuous-time comparator should react within less than 2.5 ns. Such a wide-band comparator consumes a considerable amount of power.

Fig. 9 shows our proposal for ALD block. It utilizes a regenerative SC comparator [16] together with a peak detector and a level shifter to shift the output voltage level of the peak detector slightly lower. With respect to the bandwidth and resolution demands, the sampling rate of the SC amplifiers is
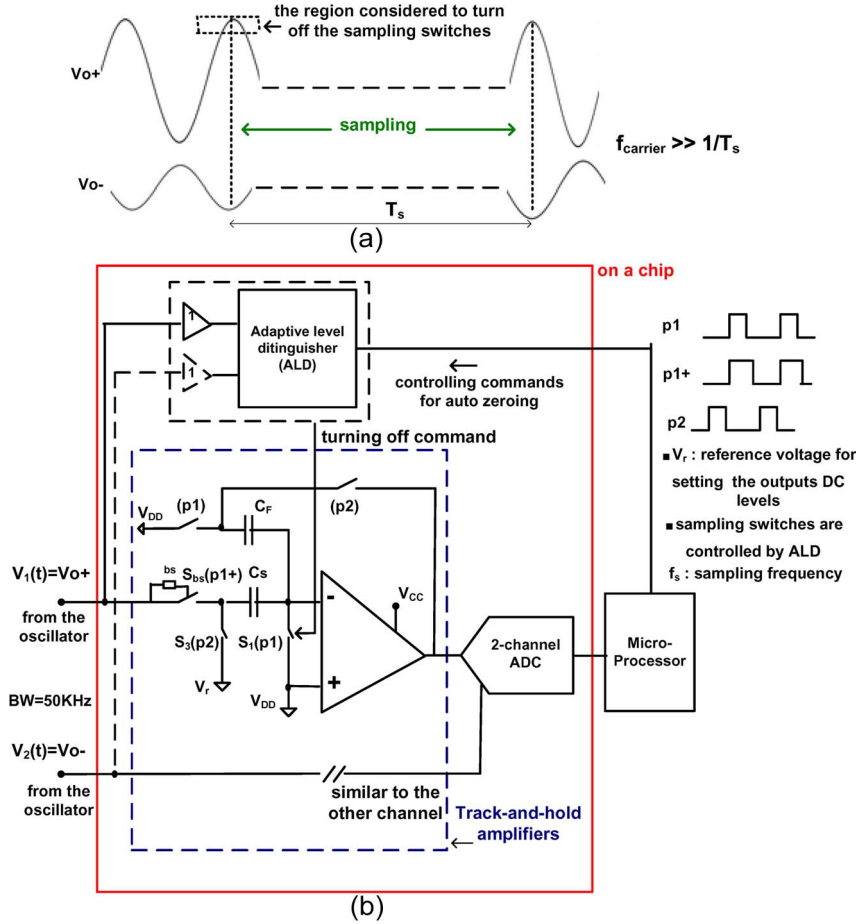
Fig. 8. (a) Method of sampling. (b) System architecture (for simplicity, the auto-zeroing operation is not shown).
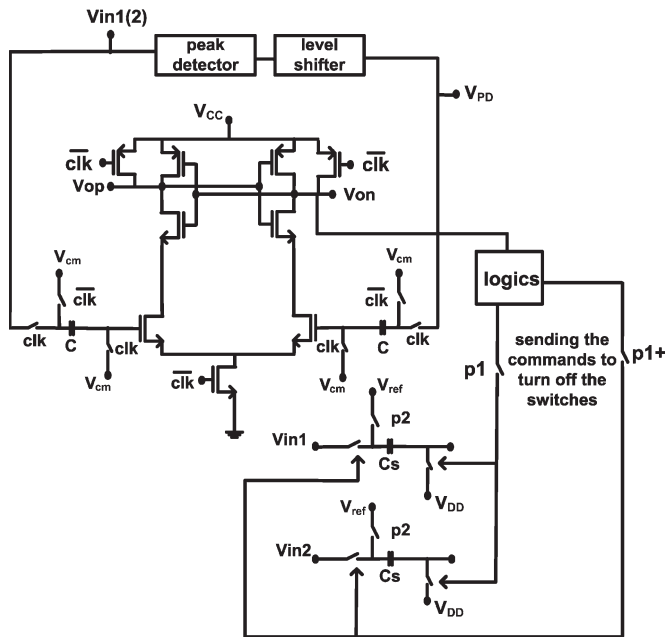

Fig. 9. ALD structure defining the sampling moments.

much smaller than the oscillation frequency. Therefore, more than one period is always available to select a peak voltage (i.e., a voltage placed in the sampling window). For instance, if the sampling frequency is 1 MS/s (500-ns sampling phase length) and the oscillation frequency is 25 MHz, then at least 12 periods are available to catch a peak. The idea is that searching 12 periods for selecting a peak results in a smaller bandwidth requirement for the comparator than just searching one period. Let us consider a dynamic comparator. To calculate the required working frequency of the comparator, we should solve a set of equations as follows. The sampling moment t_s should be selected in such a way that it can fulfill

$$V_A \sin(\omega t_s + \Phi) > V_{PD} \tag{20}$$

where V_A is the oscillation amplitude, Φ is the phase difference between the input signal and the comparison starting moment, and V_{PD} is the comparator threshold voltage (the level shifter output in Fig. 9). We can write

$$\begin{cases} \sin^{-1}(V_{PD}/V_A) + 2k\pi < \omega t_s \\ \qquad + \Phi < (2k+1)\pi - \sin^{-1}(V_{PD}/V_A) & (21) \\ t_s = mT_{\text{comp,ck}} & (22) \\ \max(m) = [T_s/T_{\text{comp,ck}}] & (23) \\ \max(k) = [T_s/T - 1] & (24) \end{cases}$$

where t_s is the sampling moment, $k, m = 0, 1, 2 \ldots$, T_s is the length of the T/H sampling time, $T_{\text{comp,ck}}$ is the working period of the comparator, and $T = 2\pi/\omega$. To calculate the minimum required speed for the comparator from (21)–(24) under different conditions, we have written a program under MATLAB.
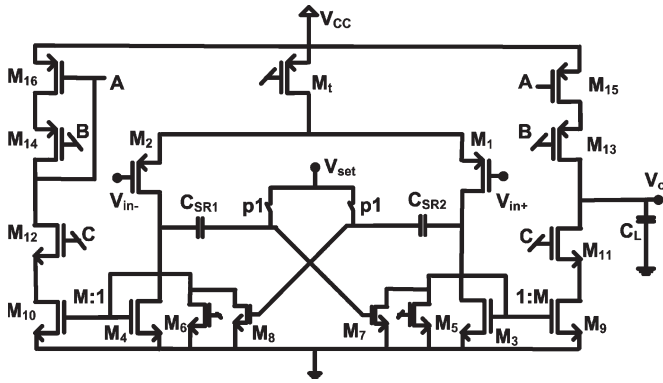
Fig. 10. Class AB opamp architecture.

For instance, if $T_s = 500$ ns, $T = 40$ ns, $V_A = 500$ mV, and $V_{PD} = 490$ mV, then running the program [including (21)–(24)] results in $T_{\text{comp,ck}} < 24$ ns.

If the same function needs to be performed in a straightforward way, then as we have already mentioned, $T_{\text{comp,ck}} < 2.5$ ns. Therefore, an improvement of more than nine times can be achieved.

As depicted in Fig. 9, an SC regenerative comparator is utilized for this job. Such a dynamic comparator consumes much less power than its continuous-time counterparts. Moreover, the decision point in this comparator can accurately be set because it depends on the capacitors' ratio [16].

After the first peak during the sampling phase has been identified, the input voltage value is frozen on the sampling capacitors by means of logic circuits and sampling switches, as stated above, after which a holding phase is started.

The comparator input offset can be taken into account in (21)–(24) as a random limited value (i.e., a few millivolts). However, the level of V_{PD} can be adjusted to compensate the effect of offset.

B. OPAMP

The opamp architecture is illustrated in Fig. 10. Obviously, the gain–bandwidth of this opamp is proportional to $1:M$ (the current ratio shown in Fig. 10). Transistors M_5–M_8 take away the dc currents of M_3–M_4. Therefore, the output impedance increases, which results in the dc gain being boosted [19]. The dc current of M_7–M_8 is adaptively controlled by the input signal level. At phase p1 (the sampling phase in which opamp does not work), the capacitors depicted as $C_{\text{SR1,2}}$ in Fig. 10 are charged to $V_{\text{set}} - V_{\text{GS3 or 4}}$, where V_{set} is a proper biasing voltage. Suppose at the next phase p2 [the holding phase in which opamp works; see Fig. 8(b)] the negative input voltage decreases. So, the drain current of M_2 rises. This causes V_{GS4} to increase. Because of the capacitive coupling with M_7 through C_{SR1}, V_{GS7} and thus M_7 drain current increase. Consequently, more current is taken away from M_3. This results that less current is mirrored in M_9.

Therefore, during the large-signal regime, the capacitive load is charged by a higher amount of current because less current is sunk by M_9. On the other hand, if the positive input voltage increases, then a similar effect (but in the opposite direction) occurs, meaning that the capacitive load is charged by M_{15} with
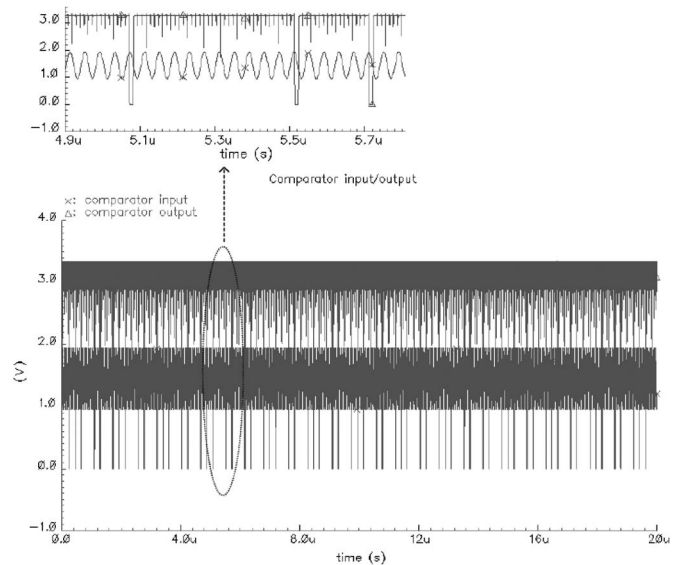

Fig. 11. Comparator simulation result. The maximum gap between the comparator pulses is magnified (the falling edge of the comparator output defines the sampling moment).

a higher amount of current. Based on the simulation results, this class AB scheme can enhance the slew rate of the opamp by about 50%.

It should be noted that the size of M_7–M_8 compared to M_5–M_6 should be small enough to prevent the instability problem in the small-signal regime of the settling period.

C. Complementary Discussions

Another advantage of sampling at the peaks is that it is possible to diminish the effect of excess terms. Using the measurement function and neglecting the parasitic components results in

$$\frac{V_1(t)}{V_2(t)} = \frac{d(\Phi_1 = L_1 i)/dt}{d(\Phi_2 = L_2 i)/dt}$$

$$= \frac{L_1(t) \cdot di(t)/dt + i(t) \cdot dL_1(t)/dt}{L_2(t) \cdot di(t)/dt + i(t) \cdot dL_2(t)/dt} \quad (25)$$

where $i(t)$ is the current of the coils. The first terms in the numerator and the denominator are dominant because the rate of current changes is much higher than that of the inductance changes. Nevertheless, in high-precision applications, it is not possible to neglect the second terms. Suppose that $i(t)$ is a sine wave. In reality, when we sample the voltage peaks, the $di(t)/dt$ term has its maximum value, and thus, the term $i(t)$ has its minimum value, approaching zero. Therefore, the second terms in (25) are completely negligible, which makes the measurement more accurate.

The sampling capacitor C_s should be small enough so that the switching operation cannot seriously affect the normal operation of the oscillator. On the other hand, C_0 in the oscillator reduces the impedance between the output nodes, and therefore, the amplitudes of the output voltages are in the order of a few hundred millivolts. Consequently, we need a large sampling capacitor to decrease the KT/C noise level, particularly for
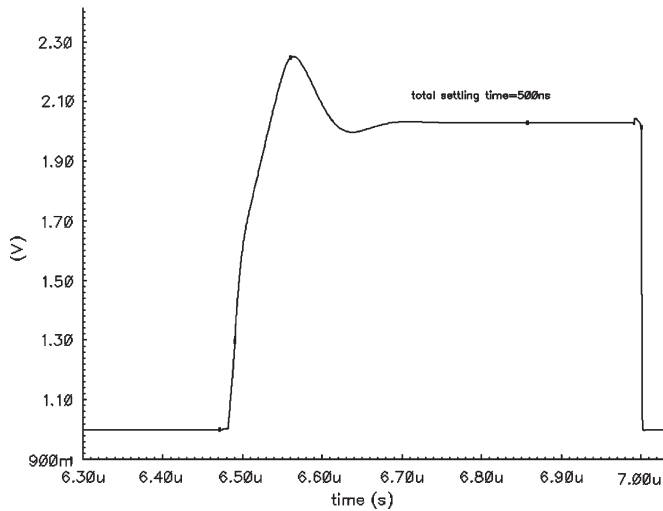
Fig. 12. Opamp settling behavior as the core of T/H.

Fig. 13. Power dissipation contributions of the system parts.

higher-resolution applications. Note that the output voltages of the oscillator are high-frequency signals. To avoid using wideband buffers at the oscillator outputs (required for driving large capacitors to suppress the KT/C noise), which adds considerable power consumption, performing oversampling and averaging (to reduce the noise level) is recommended. Therefore, the sampling job can be done by small sampling capacitors. The cost is a decrease in signal bandwidth. To have the same bandwidth, the sampling rate of the SC circuits and the ADC should be increased.

VI. RESULTS

The presented discussions are based on analytical approaches, simulations performed by Spectre, Cadence, simulator, and primary experimental results. The front-end oscillator is implemented with an off-chip resonator, whereas the rest has been designed in a standard 0.35-μm 3.3-V CMOS technology.

We designed and used a prototype coil for the primary measurements. With an impedance analyzer, we extracted an accurate model of the coil. The radius of the prototype coil was 4 mm. The specifications are in good agreement with the theory. The simulations have been carried out based on the experimental model of the coil.

Fig. 11 depicts the simulation result of the comparator behavior and the efficiency of the proposed approach for the example mentioned in Section V-A. The input frequency is 25 MHz, and the comparator working period is about 22 ns (for reliability issues, we designed the comparator with a speed of approximately 10% more than the theoretically calculated value of 24 ns). As the example was, we considered V_{PD} of about 10 mV below the input signal level. As can be seen from Fig. 11, in this case, in every 0.5 μs, at least one peak can be distinguished.

For the current application, we considered V_{PD} to be a few tens of millivolts smaller than the input signal level. In this case, a sampling frequency of about 15 MHz is enough for the comparator to distinguish at least one peak during each sampling phase.

The opamp has been designed such that there is no limitation if we want to utilize it in the future to improve the specifica-
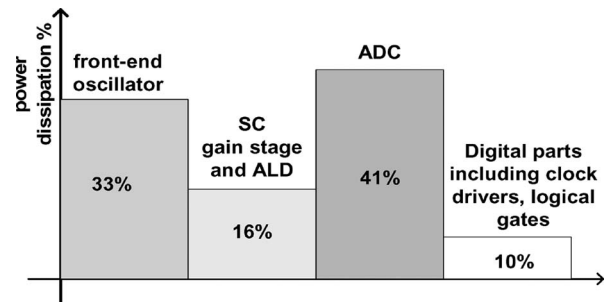
TABLE I
SUMMARIZED SPECIFICATION OF THE SENSOR SYSTEM
ALONG WITH COMPARISON WITH A PREVIOUS WORK

Design Spec.	[5]	This work
Full-scale range	1.4 mm	1 mm
Resolution	13 bits	11 bits
Thermal drift	700 ppm/°C	24 ppm/°C*
Power dissipation	100 mW	12 mW (excl. µC)
Technology	0.8 µm CMOS	0.35 µm CMOS
Bandwidth	-**	50 KHz
Output	Analog	Digital

* At a worse case
** Not available

tions. In this design, the opamp dc gain is more than 95 dB in all process corners, and the opamp slew rate is about 21 V/μs. The settling behavior of the opamp is shown in Fig. 12, where the available settling time is about 500 ns (in this case, the sampling rate for each channel is 1 MS/s). We designed a similar opamp only without the class AB part. The slew rate was around 13 V/μs. As a result, more than a 50% improvement can be seen for the proposed opamp.

On the basis of the existing dc–dc converter specifications, we placed disturbing noise sources with a 60-μV amplitude and 4-MHz signal frequency in series with the oscillator power supply, but we did not observe a considerable change in the results.

We also put a dc voltage source, which had a few millivolt amplitude, as an offset source in series with a sinus high-frequency voltage source, which had tens of microvolt amplitude, as a source of noise at the gate of one of the cross-coupled MOS transistors in the oscillator. We indeed did not observe a significant variation in the simulation results.

In Fig. 13, the estimated power consumption of each part is shown. The measurement system is implemented for 11-bit resolution and 50-kHz signal bandwidth with a 1-mm full-scale displacement range (a less than 500-nm resolution). The total

power dissipation is around 12 mW. A higher resolution can be obtained by averaging, which will lead to a reduced signal bandwidth.

Table I summarizes the specifications of the system. As can be seen, the biggest temperature drift is 24 ppm/$^\circ$C over the inductance variation range, which shows a considerable improvement compared to the previous work.

The simulation results show less than 8 ppm/$^\circ$C thermal drift in the measurement function when $L_1/L_2 \approx 1.65$. This thermal drift, as well as the power consumption, is much smaller than that reported in [5]. Compared with [7], having thousands of ppm/$^\circ$C thermal drift, an improvement of about two orders of magnitude is seen.

VII. CONCLUSION

A low-power low-thermal drift interface for ECSs has been introduced. The measurement system has been designed as an SIP, which utilizes a standard 0.35-μm CMOS technology. In this system, a front-end stage that is applicable for very-low-thermal drift and low-power applications has been introduced and discussed. The measurement method makes the system suitable for medium- to high-resolution demands.

The simulation results support the analyses. Simulations have been performed based on the experimental results of testing the prototype coil. Two differential coils were utilized to detect the target displacement. Applying ratio-metric measurement for the proposed front-end oscillator suppresses multiplicative errors such as temperature drifts. Both the system-level design and the demodulation approach were discussed. The circuitry of important blocks and their simulation results were also addressed.

The power consumption of the sensor interface is 12 mW, and the temperature drift is not larger than a few tens of ppm/$^\circ$C, showing a significant improvement compared with previous reports [5], [7].

REFERENCES

[1] V. Gupta, "Design of a proximity sensor using inductors, compatible with integrated circuit fabrication," M.S. thesis, Univ. Texas, Austin, TX, 1995.

[2] Y. Lai, "Eddy current displacement sensor with LTCC technology," Ph.D. dissertation, Universität Freiburg, Freiburg, Switzerland, 2005.

[3] G. Y. Tian, Z. X. Zhao, and R. W. Baines, "The research of inhomogeneity in eddy current sensors," *Sens. Actuators A, Phys.*, vol. 69, no. 2, pp. 148–151, Aug. 1998.

[4] S. D. Roach, "Designing and building an eddy current position sensor," *Sensors Online*, 1998.

[5] P. Kejik, C. Kluserb, R. Bischofberger, and R. S. Popovic, "A low-cost inductive proximity sensor for industrial applications," *Sens. Actuators A, Phys.*, vol. 110, no. 1–3, pp. 93–97, Feb. 2004.

[6] M. R. Nabavi and S. Nihtianov, "A survey of eddy current displacement sensors: Imperfections and signal conditioning methods," in *Proc. Int. Sci. Appl. Sci. Conf.*, Sozopol, Bulgaria, 2007, vol. 3, pp. 116–122.

[7] J. Goezinne, "Electronic circuit for detecting a change relative to a quiescent condition," U.S. Patent 6 847 215, Jan. 25, 2005.

[8] R. G. Meyer, "Low-power monolithic RF peak detector analysis," *IEEE J. Solid-State Circuits*, vol. 30, no. 1, pp. 65–67, Jan. 1995.

[9] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 349–355, Mar. 2001.

[10] P. Vasseur and A. Billat, "Contribution to the development of a smart sensor using eddy currents for measurement of displacement," *Meas. Sci. Technol.*, vol. 5, no. 8, pp. 889–895, Aug. 1994.

[11] S. Jenei, B. K. J. C. Nauwelaers, and S. Decoutere, "Physics-based closed-form inductance expression for compact modeling of integrated spiral inductors," *IEEE J. Solid-State Circuits*, vol. 37, no. 1, pp. 77–80, Jan. 2002.

[12] M. R. Nabavi and S. Nihtianov, "A low-power interface for eddy-current displacement sensors in sub-micron applications," in *Proc. I2MTC*, Victoria, BC, Canada, 2008, pp. 17–20.

[13] E. Hegazi, J. Rael, and A. Abidi, *The Designer's Guide to High-Purity Oscillator*. Norwell, MA: Kluwer, 2005.

[14] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.

[15] C. S. Koukourlis, V. K. Trigonidis, and J. N. Sahalos, "Differential synchronous demodulation for small signal amplitude estimation," *IEEE Trans. Instrum. Meas.*, vol. 42, no. 5, pp. 926–931, Oct. 1993.

[16] M. R. Nabavi and R. Lotfi, "A 1-V 12-bit switched opamp pipelined ADC with power optimization," in *Proc. ISCAS*, 2006, pp. 5359–5362.

[17] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[18] J. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design*. Norwood, MA: Artech House, 2003.

[19] L. Yao, M. S. J. Steyaert, and W. Sansen, "A 1-V 140-μW 88-dB audio sigma-delta modulator in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1809–1818, Nov. 2004.

[20] Y. Yating, D. Pingan, and W. Zhenwei, "Study on the electromagnetic properties of eddy current sensor," in *Proc. IEEE Int. Conf. Mechatron. Autom.*, 2005, vol. 4, pp. 1970–1975.

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