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A Novel IUPQC for Multi-Feeder Systems Using Multilevel Converters With Grid Integration of Hybrid Renewable Energy System

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ABSTRACT This paper presents a novel topology of interline unified power quality conditioner (IUPQC) for multi-bus/multi-feeder systems, capable of compensating both voltage and current imperfections simultaneously for power quality improvement. In this system, four voltage-source converters (VSC) with multilevel configuration are considered and space vector pulse width modulation is used in hexagonal coordinate system to reduce the complexity in generating switching pulses. In the proposed IUPQC, all converters share a common dc-link capacitor. Hence, power can be transferred from healthy feeder to adjacent feeders for compensation of sag/swell and current/voltage harmonics. This IUPQC is implemented between two feeders with hybrid renewable energy system as one of the feeders. The performance of the proposed system for various power quality problems is analyzed and presented using MATALB/SIMULINK.

INDEX TERMS Grid integration, multi-feeder systems, multi-level converters, power quality improvement, renewable energy systems.

I. INTRODUCTION

In the era of liberalization, the privatization of world electric energy market brought in a new level of competition in the energy supply business. The increasing use of sophisticated equipment for domestic and industrial applications, has increased its vulnerability to power quality problems.

In order to mitigate the power quality disturbances and to give customized solutions [1]–[3], newer devices based on power electronics called ''custom power devices'', have been developed. Modern solutions for load related problems and imperfections in supply voltage include unified power quality conditioner (UPQC) [4]. It is obtained by combining shunt compensator and series compensator to provide a solution for multiple power quality problems. The shunt compensator improves the current profile and the series compensator improves the voltage profile.

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Based on the idea of taking power from adjacent healthy feeder to compensate the problems in the existing feeder, multi-feeder custom power devices have evolved. When compared to single feeder custom power devices, superior performance is assured with these devices. Some of the interline custom power devices include interline dynamic voltage restorer (IDVR) [7], [8], interline voltage controller (IVOLCON) [9], [10], IUPQC with two VSCs [11].

In secondary selective systems the customer load is generally divided between two feeders and supplied from two different substations. In this regard, it is considered that the effect of voltage variation in a feeder on the other feeder is negligible. Hence, two feeders are considered as two isolated sources based on the fault level at point of common coupling. In IUPQC [11] with two VSCs, one converter is connected in shunt with one feeder and another converter in series with another feeder. In this configuration, current profile of the first feeder and the voltage profile of the second feeder are improved. In this connection, many other possibilities are explored by the addition of third converter [12]–[16] with

different nomenclature such as UPQS [13], DS-UniCon [12] and MC-UPQC with 3 VSCs [16].

A new topology of unified power-quality conditioning system, IUPQC with four VSCs is proposed in this paper. This IUPQC is able to improve voltage and current profiles in multi-bus/multi-feeder systems simultaneously. The proposed IUPQC is implemented between grid and the HRES [17].

II. PROPOSED SYSTEM

The proposed IUPQC system is connected between two feeders, in which HRES is considered as one feeder and another feeder from grid as shown in Fig.1. The HRES consists of solar, wind energy system supported by battery storage system.

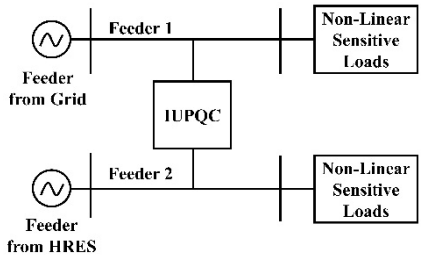


FIGURE 1. General block diagram of proposed system.

A. INTERLINE UNIFIED POWER QUALITY CONDITIONER

1) SYSTEM DESCRIPTION

In this IUPQC configuration, two shunt VSCs and two series VSCs exist. This system can be connected between two adjacent feeders to compensate the imperfections in both source voltage and load current on both the feeders. To have the power transfer capability between the feeders for the compensation of sag/swell and voltage/current harmonics, all converters are connected back to back with a common dc-link capacitor as shown in Fig.2.

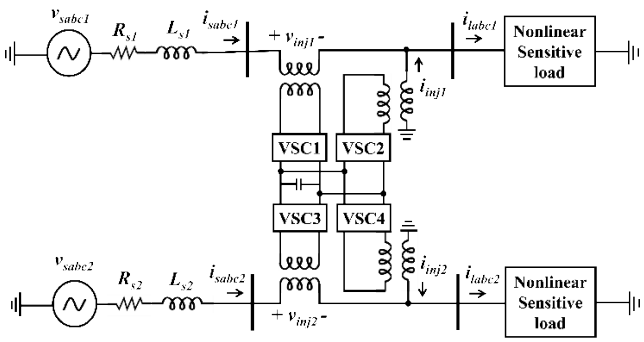


FIGURE 2. Single line diagram of four converter topology for multi-feeder system.

In the proposed configuration, two VSCs are connected in series and two VSCs are connected in parallel with loads at feeders 1 and 2. It is capable of regulating load voltages to protect the loads from voltage disturbances in the system. Also, compensates for the reactive and harmonic components of nonlinear load currents (i_{l1} and i_{l2}). Here, series VSCs are operated so as to control voltage while the shunt VSCs are operated to control current in both the feeders.

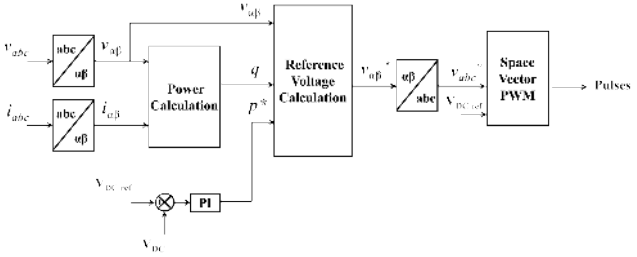


FIGURE 3. Shunt compensation control diagram.

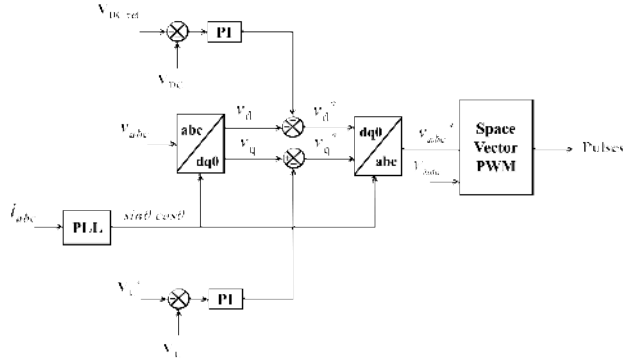


FIGURE 4. Series compensation control diagram.

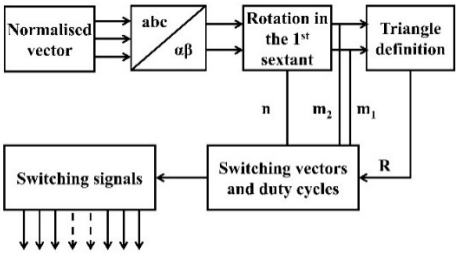


FIGURE 5. Control diagram for SVPWM implementation.

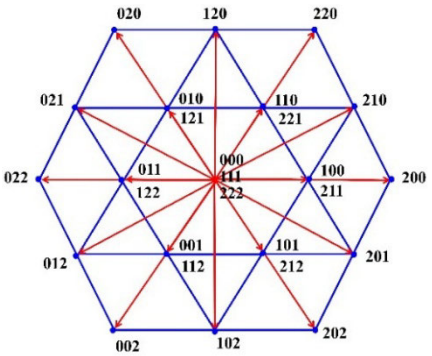


FIGURE 6. Space vector diagram of three-level inverter.

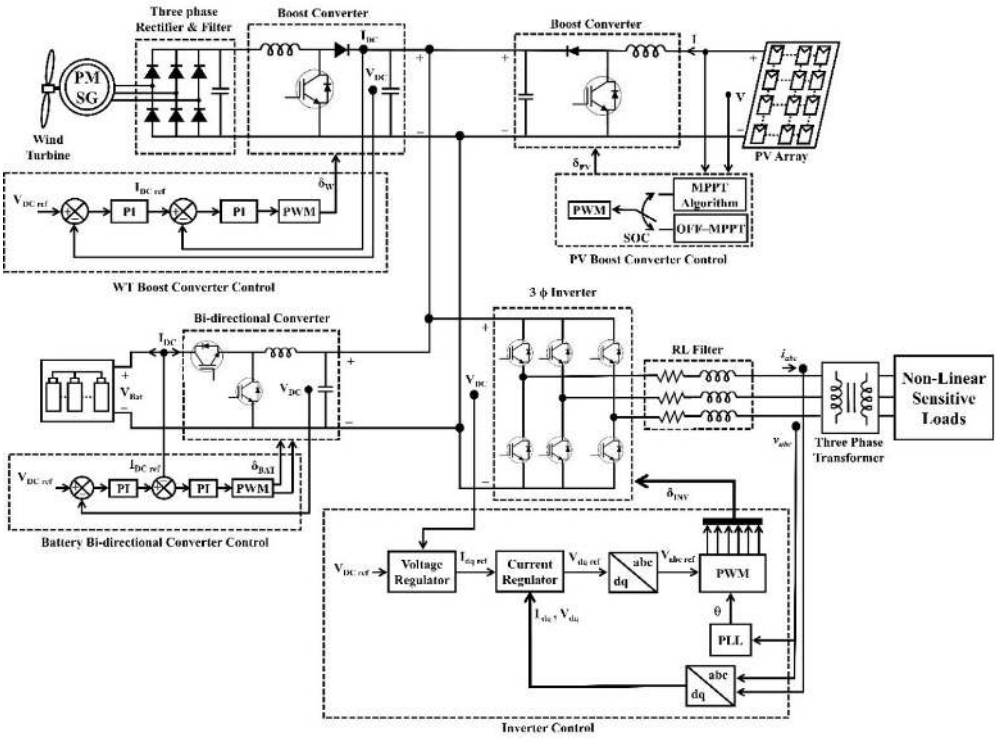


FIGURE 7. Schematic diagram of HRES.

TABLE 1. Equivalent components in first sector.

gh components	Sector	Equivalent Components
$V_g > 0$ & $V_h >= 0$	1	$m_1 = V_g$, $m_2 = V_h$
$V_g < 0$ & $V_h >= 0$ & $(V_g + V_h) >= 0$	2	$m_1 = V_g$, $m_2 = V_g + V_h$
$V_g < 0$ & $V_h >= 0$ & $(V_g + V_h) < 0$	3	$m_1 = V_h$, $m_2 = -V_g - V_h$
$V_g < 0$ & $V_h < 0$	4	$m_1 = -V_h$, $m_2 = -V_g$
$V_g > 0$ & $V_h < 0$ & $(V_g + V_h) < 0$	5	$m_1 = -V_g - V_h$, $m_2 = V_g$
$V_g >= 0$ & $V_h < 0$ & $(V_g + V_h) >= 0$	6	$m_1 = V_g + V_h$, $m_2 = V_h$

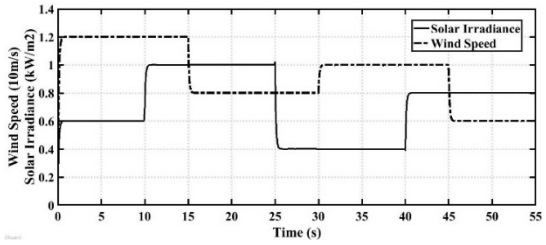


FIGURE 8. Solar irradiance and wind speed levels.

Multilevel converters are used for the VSCs in the proposed system. Three level diode-clamped three phase converters are used. Many PWM techniques such as sinusoidal triangular comparison technique, selective harmonic elimination & hysteresis techniques, and space vector pulse width modulation (SVPWM) [18] are available for the multilevel converters. Based on the advantage of reducing common mode and balancing DC link capacitor voltage, SVPWM is preferred for multilevel inverters in this work.

TABLE 2. Parameter of HRES.

Equipment	Parameter	Value
PMSG	Nominal Power	750 kW
	Nominal Voltage	575 V
	Rated Speed	25 rpm
	Stator Resistance R_S	0.01 Ω
	Stator Self-Inductance, L_S	7.79 mH
	Pole pairs, p	42
	Permanent Magnetic Flux, ϕ_a	7.35 Nm/A
PV Arrays	Total Maximum Power	600 kW
	No. of arrays in parallel	3
	No. of Parallel Strings per array	64
	No. of Series Strings per array	10
PV Module	Nominal Power	315 W
	Open Circuit Voltage	64.6 V
	Maximum Power Point Voltage	54.7 V
	Short-Circuit Current	6.14 A
	Current at MPP	5.76 A
Battery	Voltage	48 V
	Capacity	58.5 Ah
	No. of Batteries in series	12
DC Bus and RL Filter	DC-bus voltage reference	1000 V
	Filter resistance	1 mΩ
	Filter inductance	45 μH

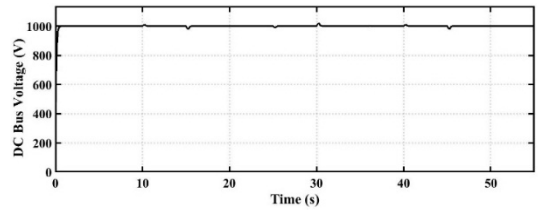
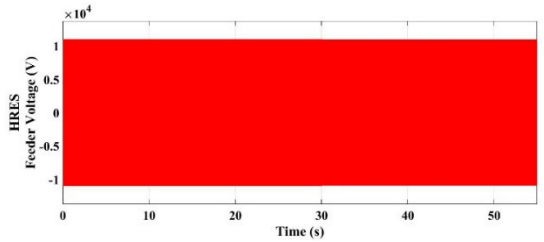
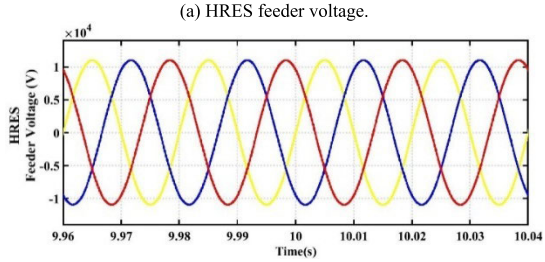


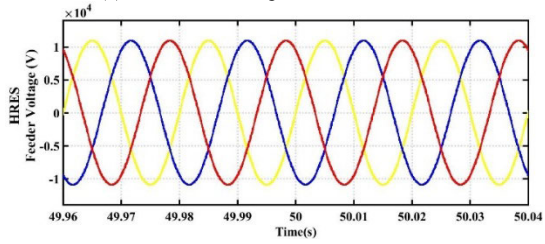
FIGURE 9. DC Bus voltage.



(a) HRES feeder voltage.

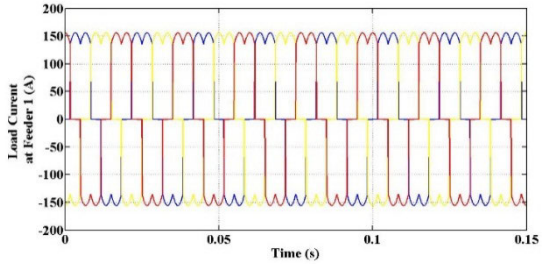


(b) HRES feeder voltage from 9.96s to 10.04s.

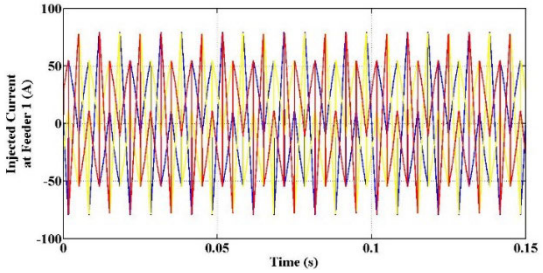


(c) HRES feeder voltage from 49.96s to 50.04s.

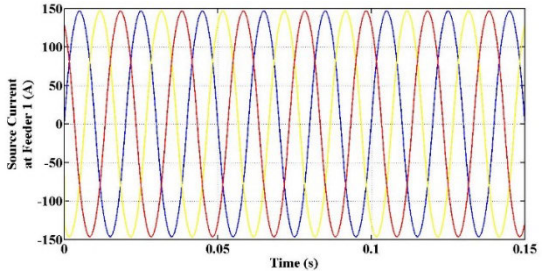
FIGURE 10. HRES feeder voltage.



(a) Load current at feeder 1.



(b) Injected current at feeder 1.



(c) Source current at feeder 1.

FIGURE 11. Voltages and currents at feeder 1.

2) CONTROL STRATEGY

Independent control of all VSCs is adopted in this configuration. Shunt VSCs compensate reactive and harmonic components of the nonlinear loads in addition to capacitor voltage regulation. Series VSCs mitigate voltage distortions like sag/swell, harmonics and interruptions. Series VSCs control is based on SRF (synchronous reference frame) theory and PQ theory is used for instantaneous power calculation in order to control the shunt VSCs.

The shunt VSC control for each feeder is shown in Fig 3. power reference values are calculated from load voltages and load currents by using *abc* to $\alpha\beta$ transformation. To achieve synchronization with supply, desired voltage reference values are generated with the compensated power references. The voltage references in addition to DC reference voltage are given to SVPWM controller to generate the gating pulses to the shunt VSC.

The series VSCs control diagram is shown in Fig.4. The series VSC is operated such that the injected voltages (V_{inja}, V_{injb} and V_{injc}) compensate the distortions in the supply voltages (V_{sa}, V_{sb} and V_{sc}). This ensures perfectly sinusoidal voltages at PCC (V_{la}, V_{lb} and V_{lc}) with the required amplitude. In SRF theory, using Park's transformation, source voltages are converted to rotating reference frame to estimate the reference signal. The DC bus voltage and load voltages are controlled by two PI controllers. The SVPWM generator produces the gating pulses to the series VSCs based on the actual and reference values of load voltages.

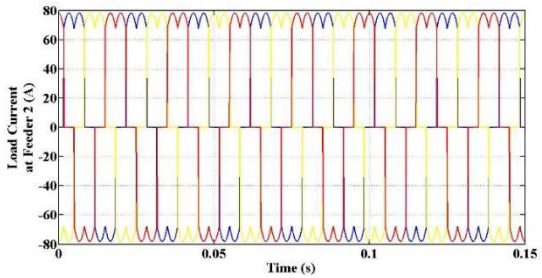
Implementation of SVPWM involves complex computations. Control diagram for SVPWM is shown in Fig.5. Based on the refrence voltage, the sector in which the voltage vector lies is identified.

Sector division with corresponding voltage spaces are represented with switching positions in Fig.6. With the sector identification, corresponding duty cycles are calculated and sequence of voltage states is generated.

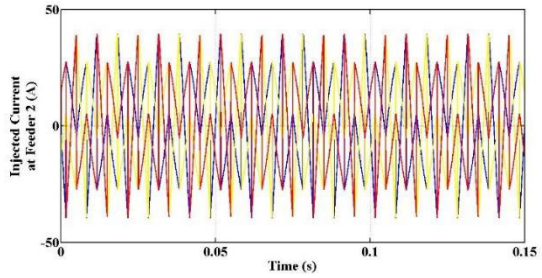
To determine the reference voltage vector location, hexagonal (g-h space) coordinate system is used, as it is complex with cartesian coordinate system. Sectors and their equivalent components in g-h space are mentioned in Table.1.

B. HYBRID RENEWABLE ENERGY SYSTEM

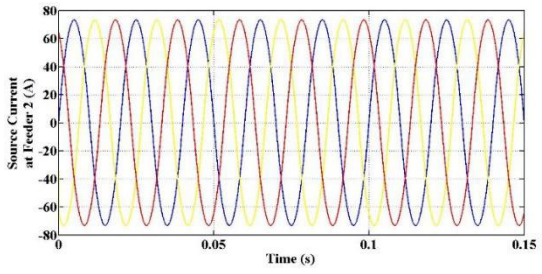
The HRES consists of a 750kW permanent magnet synchronous generator (PMSG) based wind turbine, a 600kW



(a) Load current at feeder 2.



(b) Injected current at feeder 2.



(c) Source current at feeder 2.

FIGURE 12. Voltages and currents at feeder 1.

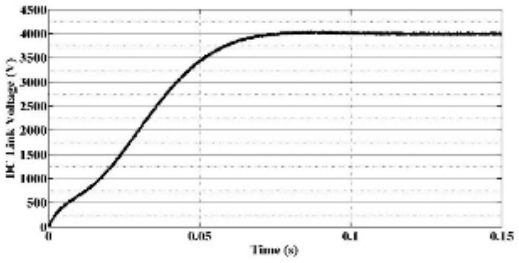
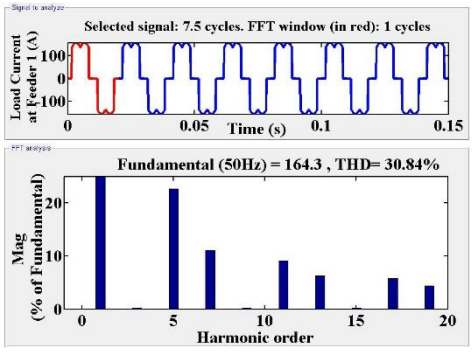
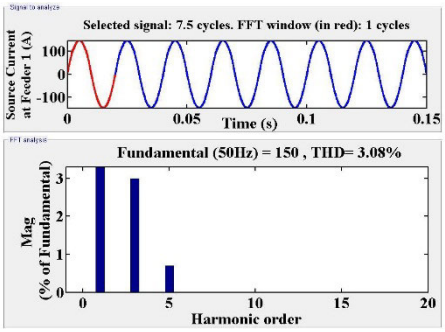


FIGURE 13. DC link voltage.

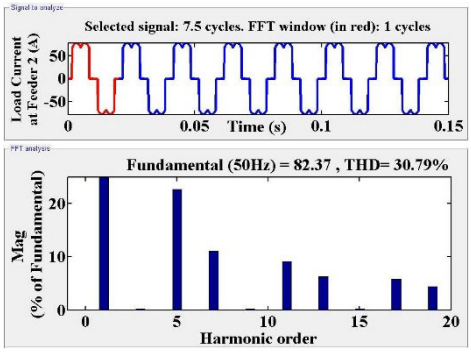


(a) Load current feeder 1

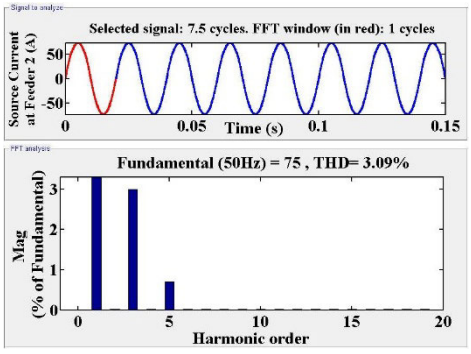


(b) Source current at feeder 1

FIGURE 14. FFT analysis at feeder 1.



(a) Load current feeder 2.

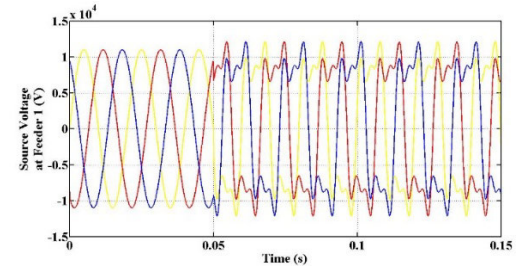


(b) Source current at feeder 2.

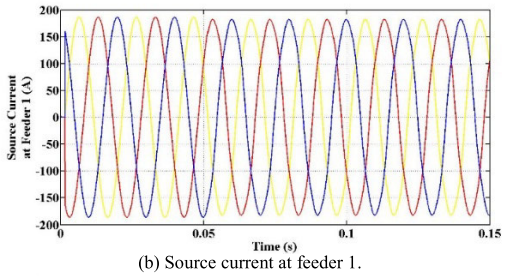
FIGURE 15. FFT analysis at feeder 2.

photovoltaic system comprising of four sets of arrays connected in parallel with each array consisting of 10 panels connected in series and 64 panels connected in parallel, and a battery energy storage system (BESS) consisting of 12 lithium-ion batteries connected in series. This HRES is designed to maintain constant voltage at the dc link regardless of the variations in the solar irradiance level and wind speed. This is achieved by appropriate control of BESS. The detailed HRES parameters are shown in Table 2.

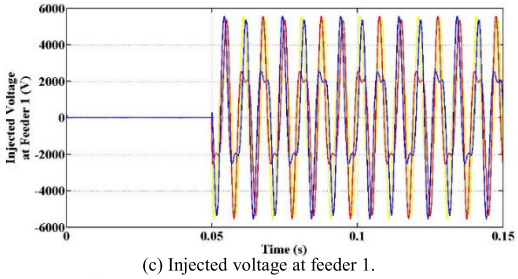
The detailed schematic of the HRES system is shown in Fig.7. The PMSG based wind turbine output is rectified and the voltage is boosted to 1kV with the help of a boost converter. The wind turbine boost controller uses a simple PI controller. The solar PV array operates in two modes of operation; MPPT mode and off-MPPT mode. Depending on the state of charge (SoC) of the battery, the PV mode of operation is switched to either the P&O based maximum power point tracking mode or off-MPPT mode inorder to mainatin the system power balance.



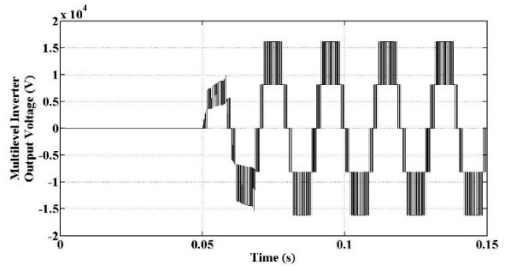
(a) Source voltage at feeder 1.



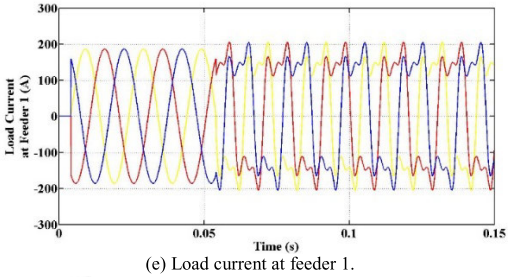
(b) Source current at feeder 1.



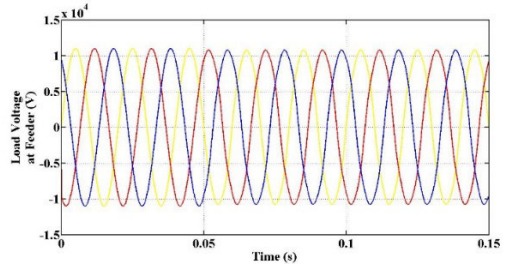
(c) Injected voltage at feeder 1.



(d) Multilevel inverter output voltage.

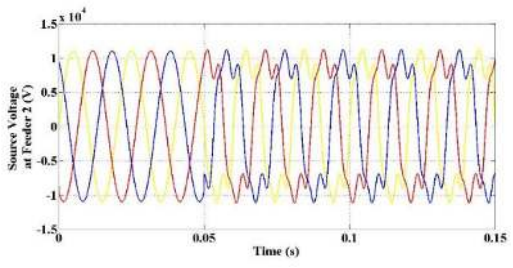


(e) Load current at feeder 1.

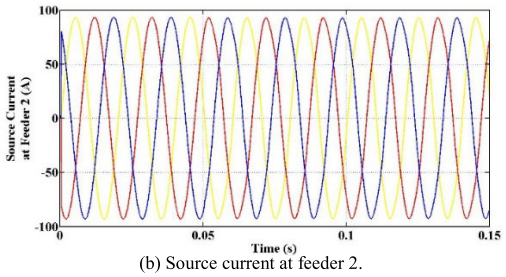


(f) Load voltage at feeder 1.

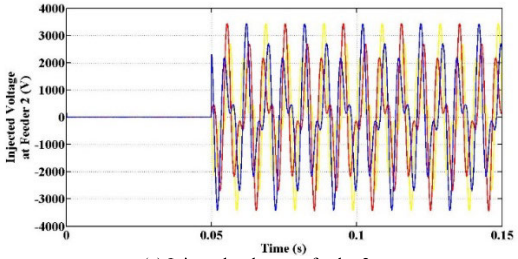
FIGURE 16. Voltages and currents at feeder 1.



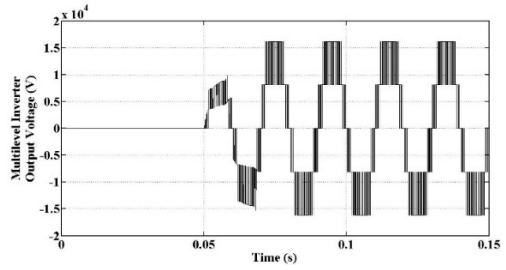
(a) Source voltage at feeder 2.



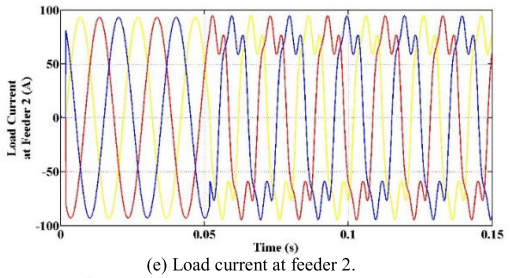
(b) Source current at feeder 2.



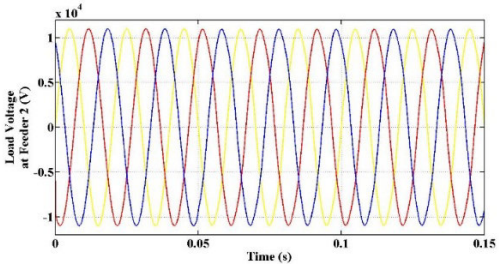
(c) Injected voltage at feeder 2.



(d) Multilevel inverter output voltage.



(e) Load current at feeder 2.



(f) Load voltage at feeder 2.

FIGURE 17. Voltages and currents at feeder 2.

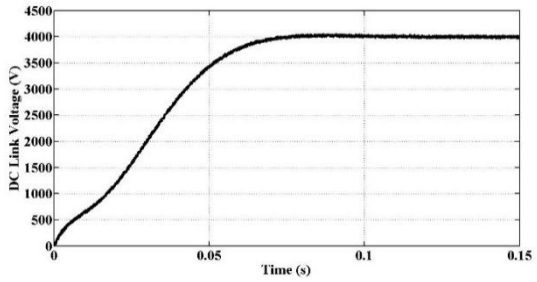
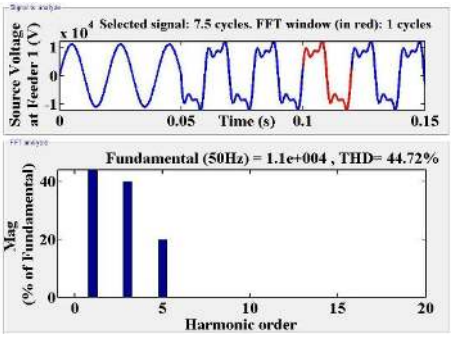
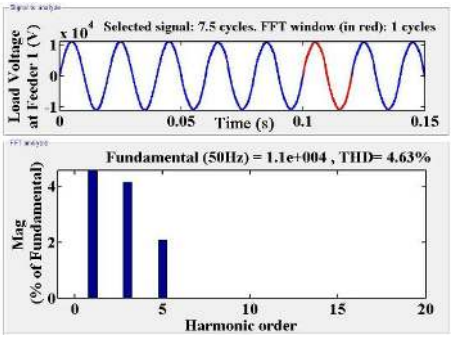


FIGURE 18. DC link voltage.



(a) Source voltage at Feeder 1.

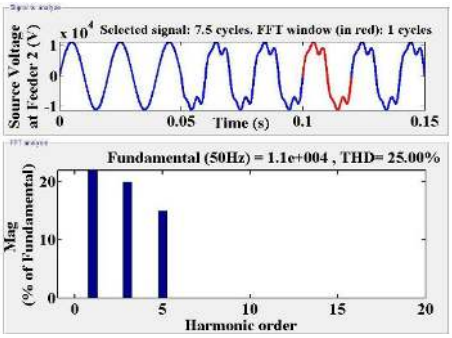


(b) Load voltage feeder 1.

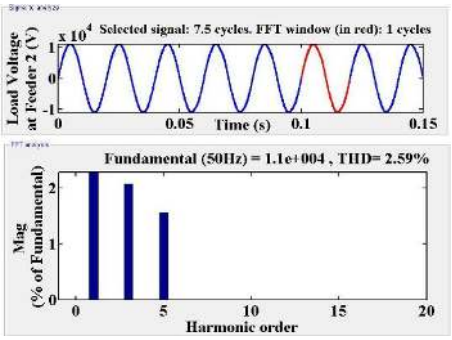
FIGURE 19. FFT analysis at feeder 1.

The BESS consists of batteries connected in series and a bi-directional buck boost converter. When the power generated from RES is insufficient to meet the load demand, the BESS operates in boost mode and delivers power. When there is excess power generation from RES, the BESS operates in buck mode and receives power and thus charging the batteries, also during this condition, when the SoC of the battery reaches its maximum limit, then in order to avoid damage to the batteries, the PV boost converter operates in off-MPPT mode. The bidirectional converter uses a PI based controller.

The HRES consists of the PMSG based WT, PV array and the BESS all connected to a dc bus. A three-phase inverter is connected to this dc bus and with the help of an inverter control algorithm, the inverter provides a constant output voltage. The inverter output is filtered and stepped up to 11kV by the step-up power transformer and supplies power to the load.



(a) Source voltage at feeder 2.



(b) Load voltage feeder 2

FIGURE 20. FFT analysis at feeder 2.

III. RESULTS AND DISCUSSIONS

The performance of the proposed system is analyzed and presented using MATALB/SIMULINK. Firstly, the performance of HRES is presented by considering various combinations of renewable energy inputs. Later, the performance evaluation of IUPQC for grid integration of HRES is discussed.

A. HRES PERFORMANCE

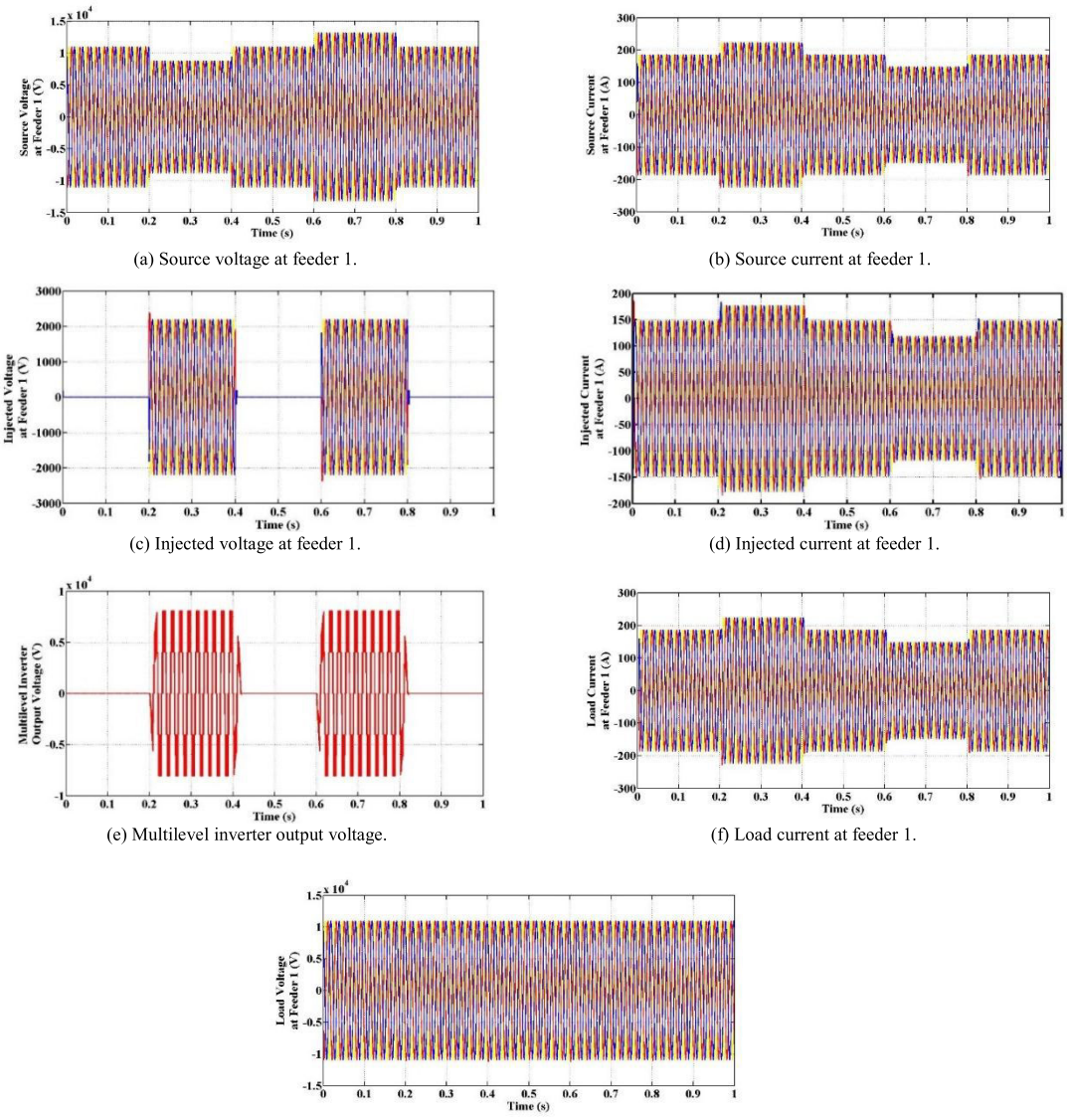
The HRES is designed to maintain a constant voltage regardless of the variations in the wind and solar inputs with the help of BESS. The HRES is designed to provide the performance of an actual grid. As shown in Fig. 8., the solar irradiance and wind speeds are varied for different combinations of wind and solar conditions in order to test the performance of the HRES.

The dc bus voltage is maintained for 1kV as shown in Fig. 9, even for the different variations of the wind speed and solar irradiance, the voltage is maintained constant at the dc bus, this is achieved by the BEES.

The voltage at the output of the transformer secondary is shown in Fig. 10 and it is remains constant at 11kV since the dc bus voltage is maintained constant. Thus, the HRES system provides a stable constant voltage and frequency which can be supplied to the load.

B. IUPQC PERFORMANCE

The proposed IUPQC topology for two feeder System and its control schemes have been tested through extensive case studies. The power system with two feeders of three-phase, three-wire 11kV, 50-Hz utilities is considered. Results are



(a) Source voltage at feeder 1.

(b) Source current at feeder 1.

(c) Injected voltage at feeder 1.

(d) Injected current at feeder 1.

(e) Multilevel inverter output voltage.

(f) Load current at feeder 1.

(g) Load voltage at feeder 1

FIGURE 21. Voltages and currents at feeder 1.

presented, and the performance of IUPQC is discussed. Different power quality problems namely, current harmonics due to nonlinear loads and supply voltage imperfections like sag/swell and voltage harmonics, are considered as different cases and the performance of IUPQC is presented.

1) CURRENT HARMONICS

The feeders 1 and 2 are supplying resistive loads 100ohms and 200 ohms respectively through diode bridge rectifier to have nonlinearities in the load.

It can be clearly seen in Fig. 11 and Fig. 12 that the load currents are containing harmonic content due to the nonlinear loads and source currents are almost sinusoidal.

The DC link capacitor voltage is presented in Fig.13, showing good dynamic response of the system.

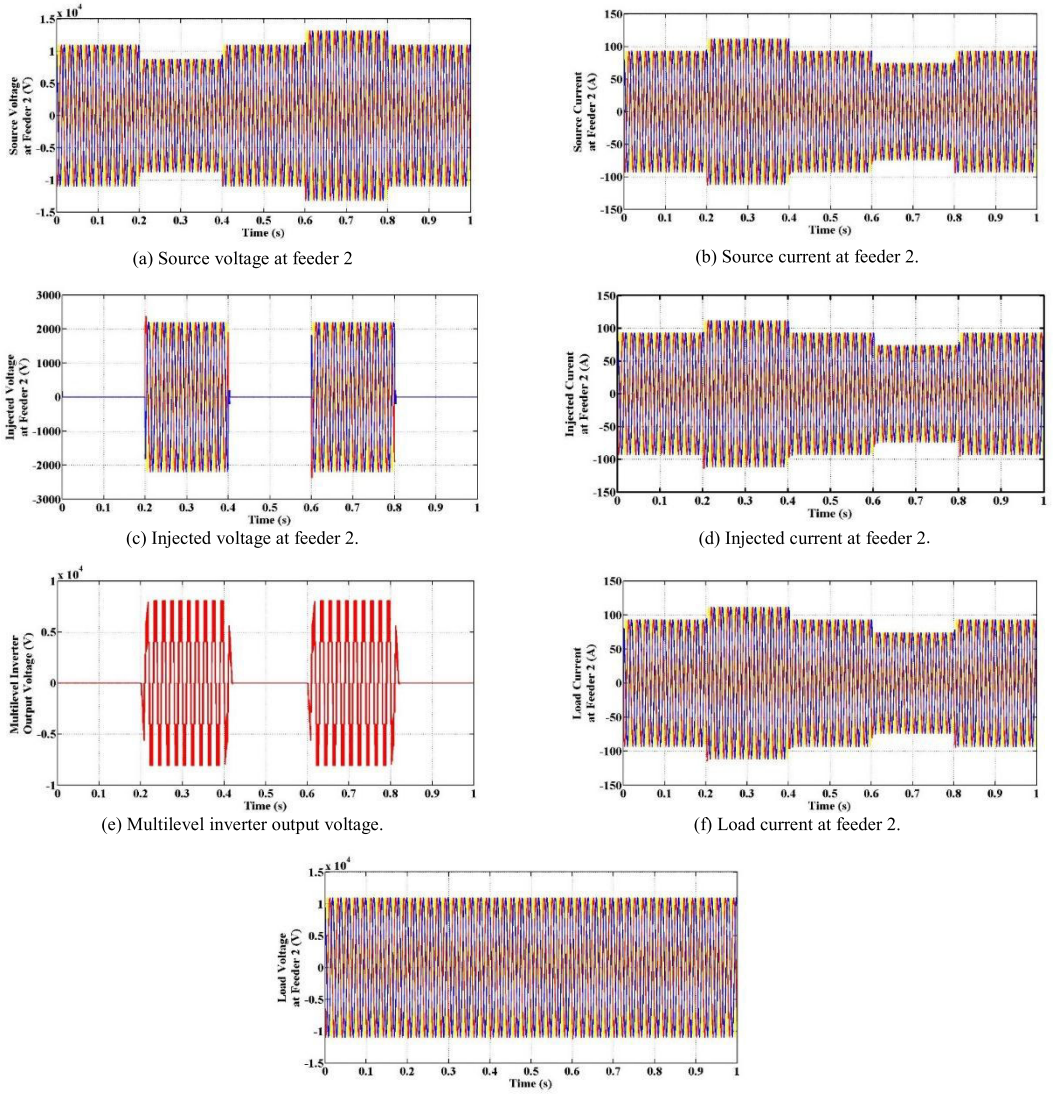
From load current to source current, THD of first feeder is reduceed from 30.84% to 3.08% and that of second feeder is reduced from 30.79% to 3.09%. FFT analysis with THD values are shown in Fig.14 and Fig. 15.

2) VOLTAGE HARMONICS

To consider supply voltage imperfections, 3rd and 5th harmonics are introduced intentionally in both the feeders. First feeder voltage with 15% 3rd and 20% 5th order harmonics, second feeder with 15% 3rd and 15% 5th order harmonics are considered from t = 0.05s to supply the loads.

Source voltages, load voltages, source currents, load currents, injected voltages and multilevel converter voltages of both the feeders are shown in Fig. 16 and Fig. 17.

Distorted voltages at the source side of both the feeders are compensated at the load side. Good dynamic response of



(a) Source voltage at feeder 2

(b) Source current at feeder 2.

(c) Injected voltage at feeder 2.

(d) Injected current at feeder 2.

(e) Multilevel inverter output voltage.

(f) Load current at feeder 2.

(g) Load voltage at feeder 2.

FIGURE 22. Voltages and currents at feeder 2.

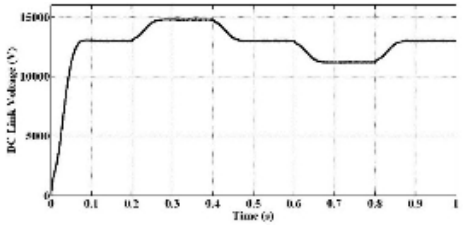


FIGURE 23. DC link voltage.

the system can be observed by the DC link capacitor voltage in Fig.18.

FFT analysis with THD values are shown in Fig. 19 and Fig. 20. It is observed that THD of Feeder 1 is improved from 44.72% to 4.63% and that of Feeder 2 is improved from 25% to 2.59%.

3) SAG AND SWELL

Sag and swell conditions are introduced in the source voltages of both the feeders simultaneously. Considered feeder voltages contain 20% sag and swell between 0.2s to 0.4s and 0.6s to 0.8s respectively. First feeder supplies RL of 50Ω and 100mH and second feeder supplies RL load of 100Ω and 200mH. Source voltages, source currents, load voltages, load currents, injected voltages and multilevel converter voltages of both the feeders are shown in Fig. 21 and Fig. 22.

It can be observed that source voltages are compensated at the loads of both the feeders. DC link capacitor voltage can be observed from Fig. 23.

IV. CONCLUSION

The hybrid renewable energy system is developed and implemented for different variations in the supply and load demand.

The results show that proposed IUPQC can be satisfactorily implemented for grid integration of HRES. IUPQC is capable of regulating load voltages to protect the loads from voltage disturbances in the system. Also, compensates for the reactive and harmonic components of nonlinear load currents. Power can be transferred from healthy feeder to adjacent feeders for compensation of sag/swell and current/voltage harmonics. It can be inferred that IUPQC can be a better solution to multiple power quality problems in multi-feeder systems.

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