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A Novel Mechanism for Harmonic Reduction in Single Source Isolated Buck-Boost Hybrid Multilevel Inverter

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Abstract: Traditional Hybrid Multilevel inverter produces (2n+1) levels at output voltage of inverter for n number of sources by a switching mechanism which requires 4n number of switches. However, one underlying problem of single phase multilevel inverter is that it requires isolated sources which render it inappropriate except where isolated energy sources are available. In this paper, firstly, a new technique is proposed for generating multiple isolated Buck-Boost DC sources of variable voltages from a single DC source. Secondly, a new switching algorithm is proposed by which number of output voltage levels can be increased by 80%, 157% and 833% while reducing number of switch count by 0%, 16.66% and 25% keeping voltage stress across the switches unhampered for two, three and four source inverter respectively compared to traditional multilevel inverter. As a result, conspicuous improvement is achieved in terms of harmonic distortion dropping it down to 4% and less than 1% for three and four source inverter respectively even without using output filters or sinusoidal PWM switching signals. A meticulous analysis of the circuit configuration and switching algorithm along with detailed performance analysis is provided throughout the paper.

Keywords: Hybrid Multilevel Inverter, Simulated Annealing, THD, Fuzzy Logic, Harmonics Reduction

1. Introduction

Multilevel inverter has become popular especially in high power applications due to its inherent capability of reducing voltage stress across semiconductor devices. At the same time, multilevel inverter is capable of producing higher output voltage which contains lesser harmonics and sub-harmonics [1]. Most popular inverter topologies in recent literature have been diode-clamped multilevel inverter (DC-MLI), flying capacitor multilevel inverter (FC-MLI) and cascaded H-bridge multilevel inverter (CHB-MLI) [2]. Among these, intuitive arrangement of CHB-MLI facilitates reduced circuit components, flexible low frequency switching techniques, low electro-magnetic interference and better output frequency spectrum [1].

Traditional CHB-MLI requires n isolated DC sources for an output voltage which exhibits (2n+1) discrete voltage levels which precludes its universal implementation for high power applications [5]. Leon M. Tolbert adopted a pragmatic approach by using a single DC source with the remaining (n–1) dc sources being capacitors [3, 7]. One inherent problem with that configuration is that it offers limited control over capacitors voltage as the capacitors are charged as a part of overall current flow. As capacitors are charged to an equal voltage levels, output voltage can only obtain limited discrete values. An adroit switching arrangement can increase number of voltage levels, hence reducing harmonic distortion. This approach demands unequal source voltage for each hybrid inverter block [4-9]. Moreover, it does not maneuver to determine optimum values of sources which exhibit lowest

harmonic distortion in output voltage. High frequency PWM signals can be used to reduce THD instead of increasing discrete voltage levels, but it hampers one fundamental advantage of MLI [11-15]. It would increase device rating, switching loss and overall efficiency as a result of high frequency switching.

In this paper, a systematic approach is introduced to overcome some of the existing drawbacks of traditional CHB-MLI while simultaneously improving power quality in terms of frequency spectrum. Firstly, isolated DC sources are generated from a single DC source by slightly modifying typical Buck-Boost circuit arrangement and connecting them parallel. Traditional way is to generate isolated sources by using tapped transformer and traditional Buck-Boost circuit. But, transformer generally aggravates circuit efficiency and it makes the circuit bulky. Typical Buck-Boost circuit is shorted together at the ground with the source; as a result parallel connection would not isolate the sources. Modified circuit arrangement offers isolation while maintaining the flexibility of changing output voltage by varying duty cycle to the pulse. A non-linear artificially intelligent fuzzy logic controller monitors output voltage of the DC-DC converters. Secondly, an optimization algorithm, Simulated Annealing, determines best possible combinations of source voltages which collectively generate minimum distortion at output voltage of inverter. A pulse generator circuit correspondingly generates suitable pulsing signals for the switching block. New switching scheme allows creating as many voltage levels as can be generated from all possible combinations of summation and subtraction from isolated sources. As increased number of levels can be generated, overall harmonic distortion in output wave shape is reduced tremendously. Thirdly, inverter circuit arrangement is slightly modified to reduce total number of switches used for the inversion. As a consequence, cost, weight, size and other corresponding attributes of the overall circuit reduces and reliability and longevity of the package increases.

2. Proposed Methodology

Proposed methodology can be divided into three broad categories: *1)* Buck-Boost circuit Block *2)* Decision making and Pulse generation circuit *3)* Hybrid inverter block. First block consists of parallel connected modified Buck-Boost converters along with corresponding control circuitry and functionalities comprising Fuzzy logic and Simulated Annealing. Simulated Annealing (SA) is an optimization algorithm which is activated only upon any change to the desired peak voltage of output voltage of inverter. It calculates such subsets of voltages whose combinations deliver minimum distortion in inverter output provided that cumulative summation is equal to the desired peak of output voltage. Fuzzy Logic Block maintains the actual voltage of the DC-DC converters to the desired levels by changing the duty cycle of the pulse. Pulse generation and control circuitry consists of decision making and switching time estimation, Interrupt and ADC functionality, general I/O and Opto-coupler isolation. Inverter Block consists of cascaded inverter legs. Switching Pulse along with the isolated voltage sources is supplied to inverter block which generates a multilevel output at the laod.

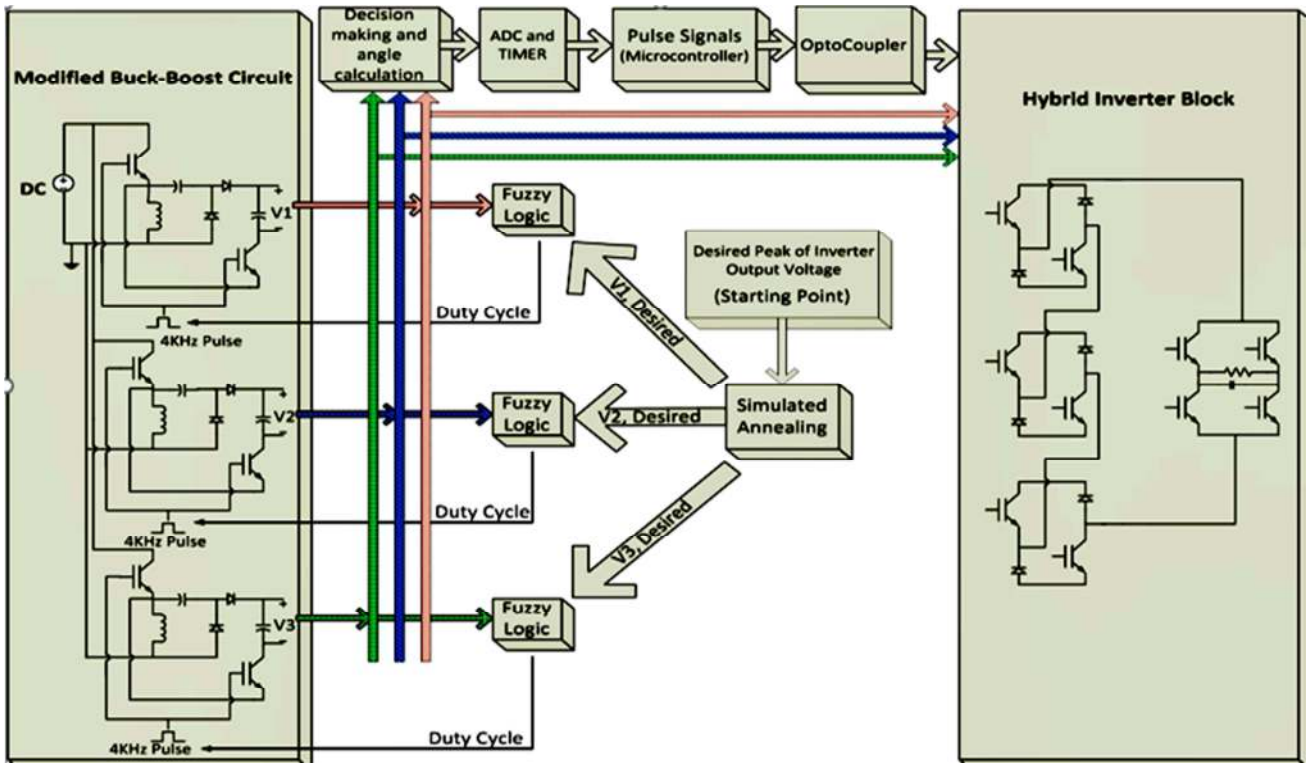


Figure 1. *Block Diagram of Proposed Methodology.*

3. Isolated Buck-Boost Converter

Operating principles and detailed analysis of overall DC-DC converter methodology will be discussed in this section. Starting point of the methodology is the desired peak voltage of inverter output.

3.1. Simulated Annealing

In proposed methodology, all possible combinations of addition and subtraction define all the discrete levels at output of multilevel inverter. As the number of levels increases, THD decreases gradually. THD also depends on the values of discrete levels. Simulated Annealing is an artificially intelligent algorithm which optimizes the values of voltage sources. Goal of SA algorithm is to determine possible values of voltages whose combinations exhibits lowest THD for desired number of sources (such as three) for a sinusoidal wave of desired Peak Amplitude A_m.

Algorithm:

Step 1: Randomly choose three random numbers (x, y, z) whose sum is equal to A_m. Asume, T=1000; i=100

Step 2: determine all possible combinations: {C}=[0 x y z x+yy+zz+x x-y x-z y-z x+y+zx+y-zy+z-xz+x-y x-y-z x-z-y y-z-x]

Step 3: Choose unique values from {C} and sort them in ascending order.

Step 4: Determine switching angles for all combinations of {C} as: $\{\theta\}=(\sin^{-1}(\{C\}/A_m)\frac{180}{\pi})$

Step 5: Formulate a staircase output from {C} &{θ}

Step 6: Calculate cumulative mean squared cumulative error, e by comparing desired sinusoidal output and staircase output.

Step 7: Randomly choose another three numbers (xn, yn, zn) and determine error, en following step 1 to step 6.

Step 8: if en<=e; then x=xn, y=y, z=zn

Step 9: if en>e, then if $exp^{(e-en)/T} > random\ number$, then x=xn, y=yn, z=zn.

Step 10: T=T-(random number)*T*i

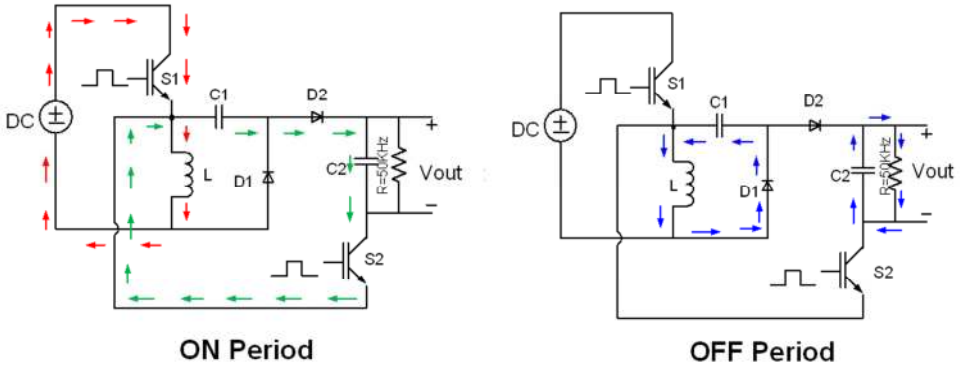
Step 11: i=i-1;

Step 12: Repeat Step 2 to Step 11 until i>=1

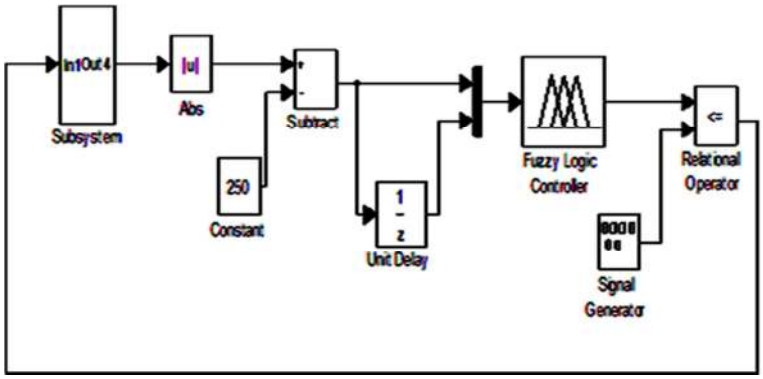
Step 13: x, y, z are the desired values which exhibits lowest THD.

3.2. Buck-Boost Circuit

Three isolated Buck-Boost converter is connected to a DC source in parallel. Traditional configuration is slightly modified so that their output nodes are not tied together. Referring to Figure 2(a), During "ON" period, inductor L is charged through switch S1 while capacitor C_1 is discharged through RC parallel branch. During "OFF" period, inductor de-energizes through capacitor, C_1 while smoothing capacitor, C_2 retains its charged state by partial discharge through large resistance, R. Inductor and capacitors are selected such that energy transfer is in equilibrium state for the desired output voltage.



(a) Buck Boost Circuit Current flow at "ON" and "OFF" period



(b) Integration of Fuzzy Logic controller

Figure 2. *Operation of Buck Boost Converter.*

Fuzzy Logic system has been integrated with proposed circuit primarily to stabilize voltage near desired voltage level as specified by simulated annealing algorithm. As proposed circuit is nonlinear, Fuzzy logic is more suitable for it than linear control system. Here in Figure 2(b), Subsystem refers to Buck-Boost converter, Out 4 refers to output voltage and in1 refers to switching gate pulse.

3.3. Hybrid Multilevel Inverter

Hybridmultilevel inverter consists of cascaded inverter legs where each inverter leg is dependent on upper-left and lower-right switches for its effective inversion. Traditional inverter block is slightly modified to reduce number of switches where upper-right and lower left switches have been replaced by diodes. Instead, only one traditional inverter block has been added which is responsible for overall inversion while cascaded inverter legs are responsible for generating all possible arithmetic combinations (addition and subtraction) of voltage levels from isolated sources. The configuration is arranged in such a way that source of greater value is connected to upper inverter leg than source of smaller value. Figure 3 shows circuit configuration and corresponding current flow path for some unique example combinations.

4. Performance Assessment

Increased voltage levels reduce THD in output voltage and output current. Figure 4(a) shows performance of SA algorithm at successive iteration. Figure 4(b) shows output voltage where sources are not optimized. Figure 4(c) and Figure 4(d) shows optimized output voltage and corresponding FFT where harmonic distortion has been reduced to 4.6%.

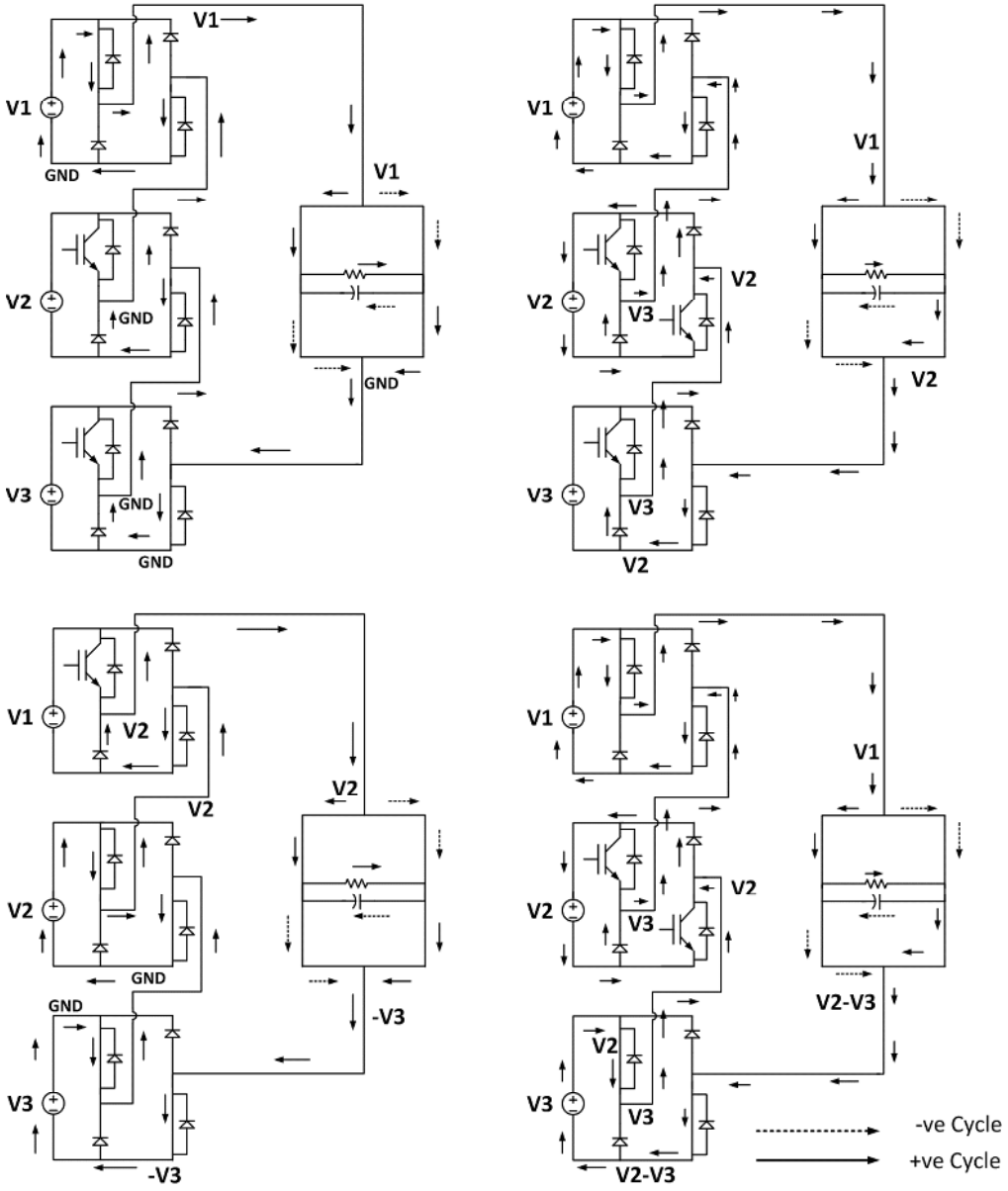
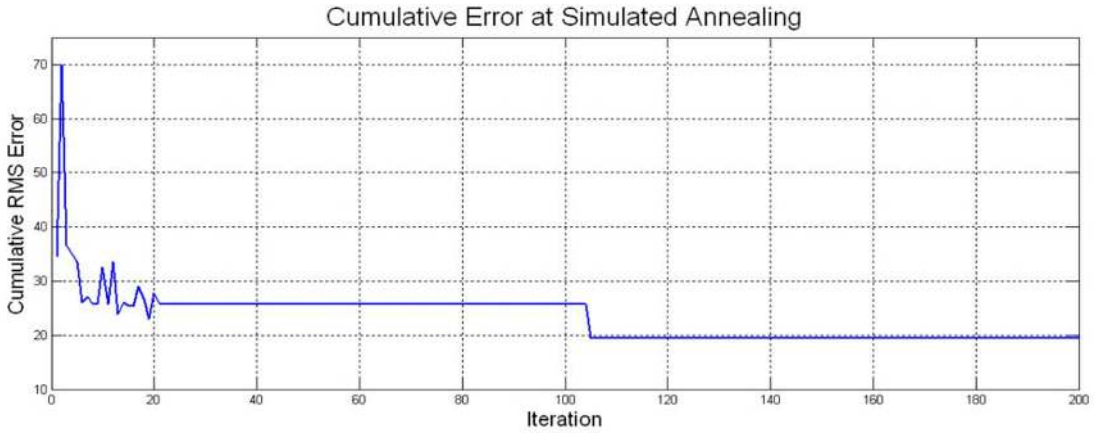
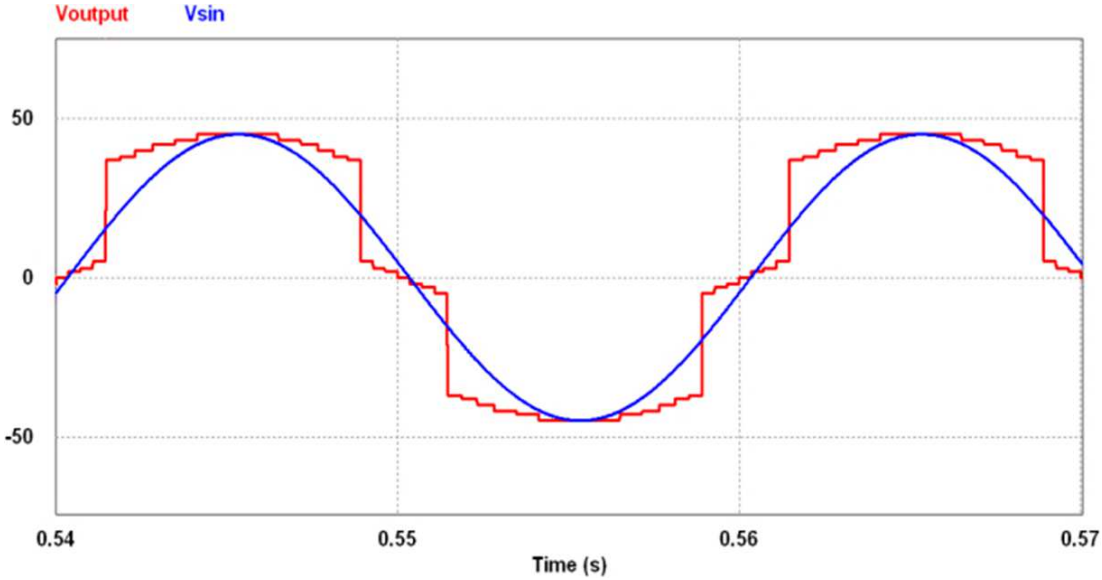


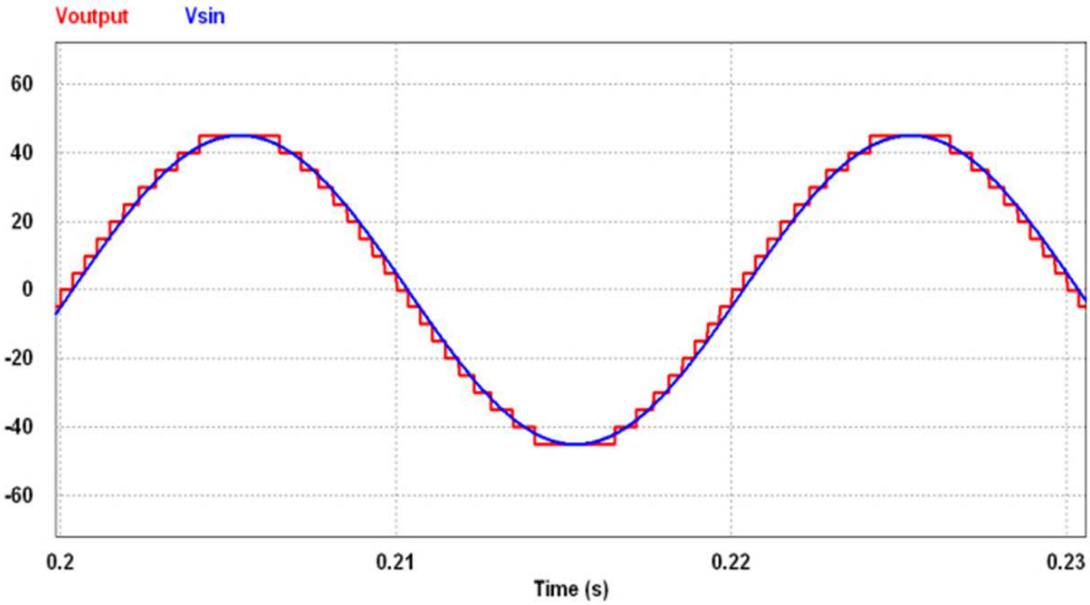
Figure 3. *Hybrid multilevel inverter.*



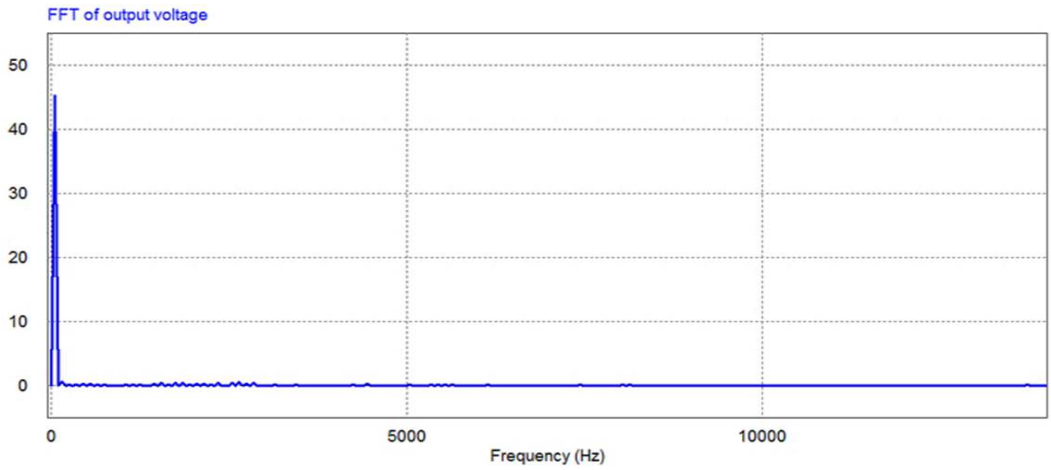
(a) Cumulative Error (THD dependent) Vs Iteration.



(b) Output voltage without SA algorithm.



(c) Optimized Output Voltage.



(d) FFT for Optimized Output Voltage.

Figure 4. *Performance Assessment.*

5. Conclusion

This paper illustrates a systematic approach to generate Low THD output power with reduced number of switches from a Single DC source using isolated Buck-Boost inverter. Simulated Annealing algorithm effectively provides a solution to generate lowest possible THD under the constraint of limited number of sources. Additional complexity in pulse generation has been supplanted by the aggrandizement in overall power quality.

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