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A novel memristor-based rSRAM structure for multiple-bit upsets immunity

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Abstract: A radiation hardened resistive SRAM structure (rSRAM) is proposed for the SRAM-based FPGAs in this paper. The rSRAM extends the conventional 6T SRAM structure by connecting memristors between the information nodes and drains of the transistors which compose cross-coupled invertors. With memristors connected to drains of OFF transistors configured to high resistance state while others configured to low resistance state forming stable voltage dividing path, the rSRAM structure is immune to both multiple-node upsets and multiple-bit upsets (MBUs). The simulation result demonstrates that rSRAM cell can tolerate simultaneous disruptions affecting all sensitive nodes with an LET (Liner Energy Transfer) of 100 Mev-cm^2/mg.

Keywords: MBUs, memory, radiation hardened, memristors, FPGA

Classification: Integrated circuits

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1 Introduction

With the aggressive technology scaling nowadays, the configuration bits in FPGAs, which are normally implemented as SRAM cells, become more vulnerable to upsets caused by particle strikes [1]. Such upsets change the value stored in SRAM cells and thus lead to device failures or functional errors, which is fatal for critical applications like aerospace. Many approaches have been designed to deal with these upsets in SRAM cells [13]. However, most of them focus on mitigating single event upset (SEU). As device size shrinks, the chances for multiple-bit upsets (MBUs) are increasing for certain particle trajectories [2]. Due to its complexity and wide applications, the MBUs-tolerant circuit design has developed as an important research area. MNDT latch [2], DEC-TED code [3], and Reed-Solomon code [4] are existing techniques that provide certain level of MBUs-tolerance. However, these approaches incur significant area overhead and none of them can protect all sensitive nodes in an SRAM cell or array.

In this paper, we propose a novel radiation hardened resistive SRAM cell (rSRAM) by extending the conventional 6T SRAM cell with memristors. All sensitive nodes in an rSRAM are protected from upsets through the stable voltage dividing path implemented by memristors. Simulation results demonstrate that under simultaneous disruptions affecting all sensitive nodes with an LET up to 100 Mev-cm^2/mg, the proposed rSRAM is still reliable.

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2 Design of rSRAM memory cell

Fig. 1 (a) shows the conventional 6T SRAM cell. As demonstrated in [8], when a particle strike happens, the upset sensitive nodes in an SRAM are typically those transistors with reverse-biased drain junctions (i.e., biased in OFF state), such as MN1/MP2 in Fig. 1 (a) when the cell stores 1. To mitigate MBUs, we propose memristor-based rSRAM structure as shown in Fig. 1 (b). The rSRAM extends the 6T SRAM with additional four memristors (M1 to M4) bridging internally and four extra transistors (MN3/MN5/MN6/MN8) to program these memristors.

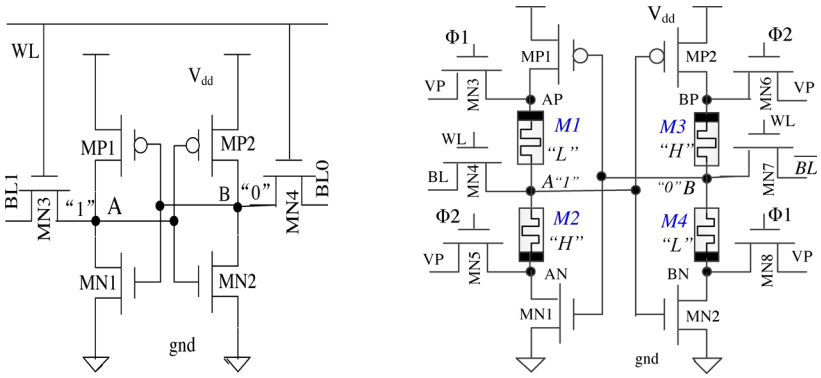

Fig. 1. (a) Conventional 6-T SRAM cell; (b) the proposed rSRAM Structure.

The memristor, known as the resistive random-access memory (RRAM), is a two-terminal device which can be fabricated between the top metal layer and other metal layers upon transistor layer within the same die [9]. By applying specific current pulse, the memristor could switch between high resistance state (HRS) and low resistance state (LRS). Once configured, the state is stable even under radioactive environment [11], which is the major motivation for its application in the proposed rSRAM. Furthermore, memristor has nano-scale feature size and CMOS-compatible process [10], which brings low area and fabrication overhead for rSRAM.

The working mechanism of rSRAM is explained as follows. Since node upsets are primarily due to ion strikes at drain of OFF transistors [8], memristors connecting to drain of OFF transistors are configured to HRS while others are configured to LRS to maintain the correct voltage level. For example, when the rSRAM cell store 1, the OFF transistors are MN1 and MP2. As such, the memristor M2 should be configured to HRS through MN4 and MN5, and so does M3 through MN6 and MN7. The other two memristors (M1/M4) are set to LRS (as the initial state shown in Fig. 1 b). Under such configuration, when a heavy ion strikes at the drain of transistor MN1 (MP2), the node AN (BP) will go low (high) to voltage V_{gnd} (V_{dd}) or below (above). In conventional 6T SRAM cell, this lead to stored value change at A and B. However, in rSRAM, the voltage of A (B) depends on the voltage dividing action of MP1, M1 and M2 (M3, M4 and MN2). Since the ratio of HRS to

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LRS is larger than 10^2 [5], $R_{M2} \gg R_{M1} + R_{MP1\text{-}ON}$ ($R_{M3} \gg R_{M4} + R_{MN2\text{-}ON}$). Thus the voltage amplitude at A (B) will still stay at high (low) and does not exceed the switching point of the opposite inverter. In other words, the voltage level of A (B) remains under the heavy ion collision.

Since a pulse of more than 10 ns is needed for switching a memristor from HRS to LRS or reversely [5], the voltage disturbances induced by heavy ions will not affect the state of memristors. Similar recovery mechanism applies when the rSRAM cell stores 0.

3 Operation scheme

The operation scheme of an rSRAM cell includes write and read operation. For write-1 operation, the state of the memristor M2/M3 should be configured to HRS while M1/M4 should be configured to LRS, and vice versa for the write-0 operation. The read operation of rSRAM cell is similar to the conventional 6T SRAM cell. The detail timing diagram for read and write operation is shown in Fig. 2.

Write operation: Three cycles are needed to write an rSRAM cell. We here take the write-1 operation as an example. Firstly, its word line WL and

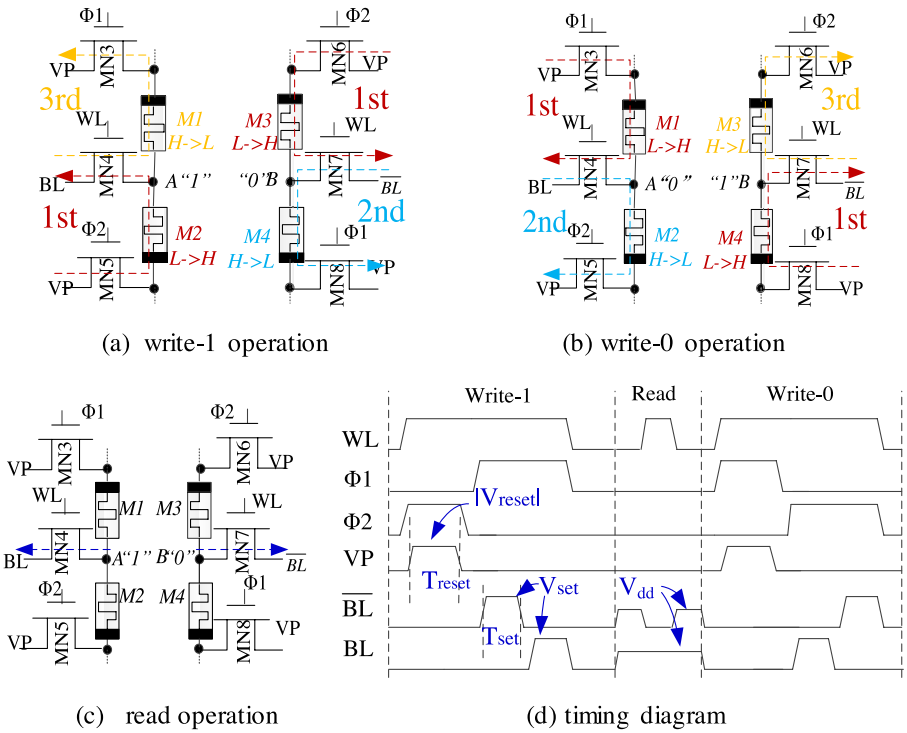

Fig. 2. Simplified rSRAM cell and timing diagram for operation scheme. The required voltage value (V_{set} and V_{reset}) and voltage pulse (T_{set} and T_{reset}) for switching the state of the memristor back and forth is different for different kind of memristors. In this paper, we take $V_{set} = 2$ v, $V_{reset} = -1.6$ v, $T_{set} = 31$ ns, $T_{reset} = 43$ ns and $V_{dd} = 1.2$ v as in [5].

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the node Φ2 are set to high voltage; BL/$\overline{\text{BL}}$ are set to V_{gnd}, and the node VP is kept at $|V_{reset}|$ for time of T_{reset}. With this biasing condition, backward currents flow through M2/M3 from VP to BL or $\overline{\text{BL}}$, which configures M2/M3 to HRS. Secondly, the node Φ1 is set to high voltage while Φ2 is set to V_{gnd}, and $\overline{\text{BL}}$ is set to V_{set} for time of T_{set}. As such, the current flows from $\overline{\text{BL}}$ to VP through MN7, M4 and MN8, to configure M4 to LRS. Thirdly, BL is set to V_{set} for time of T_{set}, to configure M1 to LRS. At this moment, the voltage of the node A approximately equals V_{set} and the voltage of the node B equals V_{gnd}. At the same cycle, when WL/Φ1 are set to V_{gnd}, the voltage of A and B will stay at V_{dd} and V_{gnd} respectively due to a regeneration effect between the two inverters, just as the write operation for the SRAM cell. As the write-0 operation is exactly opposite to the write-1 operation, we omit its detail operation procedures here.

Read operation: The read operation of an rSRAM cell is similar to the SRAM cell. The bitline BL/$\overline{\text{BL}}$, which are connected to sense amplifier, are precharged to V_{dd} before read operation. When read operation begins, the wordline WL is set to high voltage and Φ1/Φ2 are set to V_{gnd}, to transmit the voltage of A/B is to BL/$\overline{\text{BL}}$.

4 Simulation results

To verify the proposed rSRAM, SPICE simulation based on 0.13 um SMIC transistor model is performed with memristor model from [6]. To model ion strikes, the double-exponential current pulse [7] is used:

$$I(t) = \frac{Q_{tot}}{(t_2 - t_1)} \times (e^{-t/t_2} - e^{-t/t_1}) \quad (1)$$

where Q_{tot} is the charge deposited from the heavy-ion strike, t_1 is the collection time constant of the junction, and t_2 is the ion track establishment time constant. In silicon, an LET of 97 MeV-cm^2/mg corresponds to a charge deposition of 1 pC/um [8]. Parameter t_1 and t_2 are usually assumed to have values of 10 ps and 100∼200 ps respectively [7]. In this paper, we take t_1 = 10 ps and t_2 = 150 ps. Suppose the ion strike happens at the time of 1 ns. Fig. 3 shows the simulation results under previous settings.

For the 6T SRAM cell storing "1" (i.e., the node A is high and B is low), Fig. 3 (a) shows that the values at A and B are forced to switch under an ion strike with an LET of 1 Mev-cm^2/mg, which means the SRAM is flipped. However, in the case of rSRAM cell storing the same data as shown in Fig. 3 (b), even for larger LET up to 100 Mev-cm^2/mg at the node AN, output A and B maintain the correct value, which means the upset is resisted. Fig. 3 (c) demonstrates similar upset immune ability when the ion strike happens to the node BP. Finally, Fig. 3 (d) shows that under both negative and positive transients occur at AN and BP concurrently which models the multiple node upset situation [12], the proposed rSRAM still successfully maintains the correct voltage at output node A and B, which proves its multiple-bit upsets immune ability.

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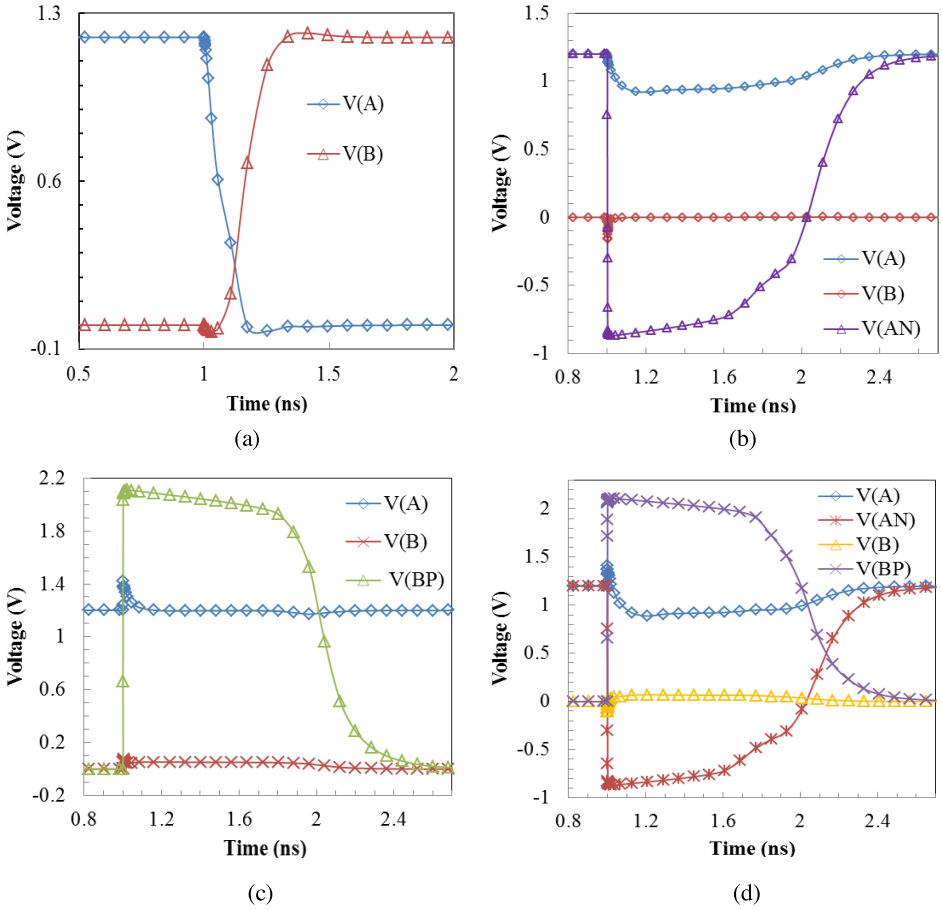

Fig. 3. (a) simulation waveforms for an SRAM affected by an ion at the node A with an LET of 1 Mev-cm^2/mg; (b) simulation waveforms for a negative upset at the node AN of the rSRAM cell with an LET of 100 Mev-cm^2/mg; (c) simulation waveforms for a positive upset at the node BP of the rSRAM cell with an LET of 100 Mev-cm^2/mg; (d) simulation waveforms for both negative and positive upsets at AN and BP respectively with an LET of 100 Mev-cm^2/mg.

Based on the simulation results described above, we can conclude that the rSRAM cell is immune to single event upset and multiple-node upsets with an LET of 100 Mev-cm^2/mg. Since there are only two sensitive nodes in an rSRAM cell, and no upset occurs even when ions strike at them at the same time, it's clear that an rSRAM array tolerate MBUs.

5 Comparison with other structures

Existing MBUs-tolerant schemes include MNDT latch [2], DEC-TED code [3], and Reed-Solomon code [4]. DEC-TED code can correct double bit failures and detects triple failures that functions by appending 2m parity bits to each data word ($2^{m-1} + 2^{m/2}$ bits). A Reed-Solomon code is defined by three parameters n, k, and t, and any positive integer m $>$ 2 such that

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Table I. Comparison to existing MBUs-tolerant approaches.

	Upset Correction	Area/bit unit(6T*)	All sensitive nodes/bits	Upset Correction Ratio(UCR)
rSRAM	2 nodes	1.67	2	100%
MNDT latch	3 nodes	6.67	8	37.5%
DEC-TED code	2 bits	$2^{m-1}+2^{m/2}$ /($2^{m-1}+2^{m/2}$-2m)	$2^{m-1}+2^{m/2}$	2 / ($2^{m-1}+2^{m/2}$)
Reed-Solomon code	(n-k) / 2 bits	n /k	n	(n-k) / (2n)

6T* represents the area of a conventional 6T SRAM cell

$(n, k) = (2^m - 1, 2^m - 1 - 2t)$, where the total length of the word is $n = 2^m - 1$ symbols, k is the number of data symbols, $n - k = 2t$ is the number of check symbols, and the symbol-error correcting capability equals t ($t \geq 2$). An MNDT latch is a MBUs-tolerant design, which utilizes layout-based interleaving and can tolerate 3 nodes disruptions per cell.

Table I presents a comparison between rSRAM and MBU tolerant approaches mentioned above. Column 1 presents all MBUs-tolerant approaches. Column 2 presents the upset correction ability, the unit of which is nodes for a cell and bits for coding approaches. Column 3 presents the area needed for an effective data bit. Column 4 presents all sensitive nodes/bits. The Upset Correction Ratio (UCR) in column 5 is defined as upset-correction-ratio (column 2) divided by all-sensitive-nodes/bits (column 4). We can see that the proposed approach can protect all sensitive nodes in the cell and its UCR value is the highest with moderate area.

6 Conclusion

In this paper a radiation hardened rSRAM structure based on memristors is proposed with the purpose of tolerating multiple-node upsets and MBUs. Memristors which are connected to drains of OFF transistors are configured to HRS as voltage dividers, and others are configured to LRS. Simulation result shows that the proposed rSRAM is resistant to simultaneous strikes with an LET up to 100 Mev-cm^2/mg affecting multiple nodes. Compared to existing techniques with similar level of MBU immunity, the proposed rSRAM cell structure has low area overhead.

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