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A Novel Open-loop Frequency Estimation Method for Single-Phase Grid Synchronization under Distorted Conditions

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***Abstract*—In this paper, a new open-loop architecture with good dynamic performance and strong harmonic rejection capability is proposed for single-phase grid synchronization under distorted conditions. Different from previous single-phase grid synchronization algorithms based on the phase locked loop (PLL) technique, the proposed method is to estimate the frequency and phase angle of the grid voltage in an open-loop manner so that fast dynamic response and enhanced system stability can be achieved. Firstly, an open-loop frequency estimation algorithm is introduced under ideal grid condition. Then, it is extended to distorted grid voltages through the combination of the developed frequency estimation unit and a pre-filtering stage consisting of a second-order low-pass filter and a cascaded delayed signal cancellation (DSC) module. In addition, a transient process smoothing (TPS) unit is designed to achieve smooth frequency transients in cases where the grid voltage experiences fast and large changes. The working principle of the new frequency estimation algorithm and the developed single-phase grid synchronization approach is given in detail, together with some simulation and experiment results for verifying their performance.**

***Keywords*—Grid synchronization, phase locked loop (PLL), frequency estimation, delayed signal cancellation (DSC), transient process smoothing (TPS).**

I. Introduction

Single-phase inverters are widely used as grid side converters that convert the power from the dc-bus and properly inject this power to the grid, with which the injected current has to be synchronized. In addition, the integration of renewable energy sources into the power grid has to follow modern grid codes [1]-[3], which requires an injection of high quality power in the normal operation mode. That is, the grid-tied inverter should be able to inject synhcronized grid currents of high power quality. Furthermore, the fault ride through capability by the grid side converter is becoming necessary, even in small single-phase systems, as it is observed in recent work in Japan [4] and the Italian technical rules issued in 2012 [5]. Therefore, the grid-connected converter should achieve an accurate and fast response to inject synchronized grid currents of high power quality and also provide voltage and frequency support immediately when a grid fault occurs.

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Consequently, the grid synchronization method for single-phase inverters should be enhanced to meet these stringent but essential requirements. In the literature, a large number of single-phase grid synchronization techniques have been proposed. Discrete Fourier transform [6], zero-crossing detection [7], Kalman filtering [8], least-squares estimation algorithm [9], artificial neural network [10], adaptive notch filter [11], complex-vector filter [12], and phase-locked loop (PLL) [13]-[25] are some of them. Among these reported grid synchronization approaches, PLLs have become the most widely used solutions.

The power-based PLL (pPLL) [13], enhanced PLL (EPLL) [14], and the orthogonal signal generator (OSG) based PLL (OSG-PLL) which can be implemented by combining pPLL and different OSGs [15]-[18], are among the most popular single-phase PLLs. A low-pass filter is needed to reject the twice grid frequency oscillations in pPLL, thus leading to a slow dynamic response. Compared with pPLL, EPLL provides a faster response because it exhibits no twice grid frequency fluctuations in the steady state, and therefore can get rid of the low-pass filter. Similarly, there is no need to insert a low-pass filter in OSG-PLLs because of the involved OSG. However, the presence of low-order harmonics introduces ripples into the estimated parameters of both EPLL and OSG-PLLs. According to [19], the standard PLL is a type-2 control system because of the use of the proportional-integral (PI) controller as loop filter. With lower bandwidth design, an enhanced harmonic rejection capability can be achieved, but at the expense of a slower response speed.

Recently, some advanced PLLs with pre/in-loop filtering stage have been reported for distorted grid voltages. With the notch filter, moving average filter (MAF), delayed signal cancellation (DSC) block or multi-harmonic decoupling cell (MHDC), the harmonic rejection performance of resulting PLLs can be significantly improved [20]-[23]. However, the pre/in-loop filter has great influence on both the response speed and system stability. It has been pointed out in [24] that the open-loop bandwidth of PLL must be sufficiently lower than the minimum frequency of disturbances rejected by the filtering stage to avoid possible interactions between the filtering stage and the PLL loop. As a result, the settling time generally cannot be less than two fundamental grid cycles when considering distorted conditions. Such a long settling time may not be acceptable in some applications, such as grid-connected distributed generation systems and fault ride through. Another drawback of the PLL technique is that the

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phase angle and frequency are estimated within a single loop which causes large frequency transient during phase jumps [25]. The effect of this undesired frequency swing is also reflected back on the phase estimation and, hence, causes delay in the process of grid synchronization [25].

The literature survey shows that traditional PLLs require proper tuning for tracking the grid voltage dynamics and for rejecting the negative effects caused by grid disturbances and harmonics. A low bandwidth has to be chosen for the purpose of harmonic rejection at the expense of a slower dynamic response. Moreover, there are interdependent loops and, therefore, each loop influences others at the same time. Consequently, the tuning of the controller parameters is more sensitive, thus reducing the stability margins.

In light of the above issues, this paper presents a novel single-phase grid synchronization algorithm which can achieve fast and accurate synchronization performance under several grid voltage disturbances and also when the measured grid voltage contains odd harmonics and dc offset. Different from previous PLLs, the proposed method is to estimate the frequency and phase angle of the grid voltage in an open-loop manner so that fast dynamic response and enhanced system stability can be achieved. It firstly estimates the frequency of the grid voltage instead of the phase angle in this work. Then, the phase angle is calculated based on the estimated frequency. Similar to existing PLLs for distorted grid voltages, the harmonic rejection capability is achieved by using a pre-filtering stage consisting of a second-order low-pass filter and a cascaded delayed signal cancellation (CDSC) module in this study. In addition, a transient process smoothing (TPS) unit is designed to achieve smooth frequency transients in cases where the grid voltage experiences fast and large changes. As an open-loop setup, the proposed grid synchronization approach can significantly improve the dynamic response, avoid system instability issues, and reduce the design complexity compared with conventional closed-loop PLLs.

II. PROPOSED FREQUENCY ESTIMATION ALGORITHM UNDER IDEAL GRID CONDITION

In this section, the basic concept of the proposed frequency estimation method is firstly introduced under ideal grid condition, and, then, its design considerations are briefly given. Finally, the developed frequency estimation method is compared with a widely used frequency locked loop (FLL).

A. Basic Concept of the Proposed Frequency Estimation Method Under Ideal Grid Condition

In an ideal single-phase grid condition (pure sinusoidal voltages), the frequency of the grid voltage can be estimated fast and accurately in an open-loop way.

To illustrate the principle of the proposed frequency estimation method, the single-phase grid voltage $v_\alpha(t)$ is assumed to be

$$v_\alpha(t) = V_p \ \sin(\omega_1 t) \tag{1}$$

where V_p and ω_1 represent the amplitude and the angular frequency, respectively, of the grid voltage. Firstly, two fictitious signals $v_{a1}(t)$ and $v_{a2}(t)$ are derived from the sampled grid voltage signal $v_\alpha(t)$ as

$$\begin{aligned} v_{a1}(t) &= v_a(t-T_1) = V_p \ \sin(\omega_1 t - \omega_1 T_1) \\ v_{a2}(t) &= v_a(t-2T_1) = V_p \ \sin(\omega_1 t - 2\omega_1 T_1) \end{aligned} \tag{2}$$

where T_1 is a constant delay time. For digital implementation of (2), $v_{a1}(t)$ and $v_{a2}(t)$ are obtained by delaying the sampled grid voltage signal $v_\alpha(t)$ with a fixed time T_1 and $2T_1$, respectively. In order to implement the frequency measurement, the intermediate signal M_1 is then derived from $v_\alpha(t)$, $v_{a1}(t)$ and $v_{a2}(t)$ as

$$\begin{aligned} M_1 &= v_{a1}^2(t) - v_\alpha(t) v_{a2}(t) \\ &= v_\alpha^2(t-T_1) - v_\alpha(t) v_\alpha(t-2T_1) \\ &= V_p^2 \sin^2(\omega_1 t - \omega_1 T_1) - V_p^2 \sin(\omega_1 t) \sin(\omega_1 t - 2\omega_1 T_1) \\ &= V_p^2 \sin^2(\omega_1 t - \omega_1 T_1) \\ &\quad - V_p^2 \sin(\omega_1 t)[\sin(\omega_1 t - \omega_1 T_1)\cos(\omega_1 T_1) \\ &\quad - \cos(\omega_1 t - \omega_1 T_1)\sin(\omega_1 T_1)] \\ &= V_p^2 \sin(\omega_1 t)\cos(\omega_1 t - \omega_1 T_1)\sin(\omega_1 T_1) \\ &\quad - V_p^2 \sin(\omega_1 t - \omega_1 T_1)\cos(\omega_1 t)\sin(\omega_1 T_1) \\ &= V_p^2 \sin(\omega_1 T_1)[\sin(\omega_1 t)\cos(\omega_1 t - \omega_1 T_1) \\ &\quad - \cos(\omega_1 t)\sin(\omega_1 t - \omega_1 T_1)] \\ &= V_p^2 \sin^2(\omega_1 T_1) \end{aligned} \tag{3}$$

Obviously, the resulting signal M_1 does not contain any oscillating components, and is a pure dc term which is a function of the amplitude and frequency of the measured grid voltage. In addition, it is worth mentioning that (3) is obtained by rigorous mathematical deduction without any approximation so that the accuracy of M_1 is independent of the sampling frequency.

Technically speaking, the grid frequency can be easily achieved from (3) if the voltage amplitude V_p has been obtained. However, it is not easy to estimate the voltage amplitude fast and accurately in practice. As a consequence, we try to implement the required frequency measurement while avoiding the voltage amplitude estimation. To achieve this goal, another intermediate signal M_2 is obtained by replacing T_1 in (2) and (3) with another constant variable T_2 ($T_2 > T_1$) as

$$\begin{aligned} v_{b1}(t) &= v_a(t-T_2) = V_p \ \sin(\omega_1 t - \omega_1 T_2) \\ v_{b2}(t) &= v_a(t-2T_2) = V_p \ \sin(\omega_1 t - 2\omega_1 T_2) \\ M_2 &= v_{b1}^2(t) - v_\alpha(t) v_{b2}(t) \\ &= V_p^2 \sin^2(\omega_1 t - \omega_1 T_2) - V_p^2 \sin(\omega_1 t)\sin(\omega_1 t - 2\omega_1 T_2) \\ &= V_p^2 \sin^2(\omega_1 T_2) \end{aligned} \tag{4}$$

It follows from (3) and (4) that the voltage amplitudes in M_1 and M_2 can be cancelled out as

$$m = \frac{M_2}{M_1} = \frac{V_p^2 \sin^2(\omega_1 T_2)}{V_p^2 \sin^2(\omega_1 T_1)} = \frac{\sin^2(\omega_1 T_2)}{\sin^2(\omega_1 T_1)} = \frac{\sin^2(2\pi f \cdot T_2)}{\sin^2(2\pi f \cdot T_1)} \tag{5}$$

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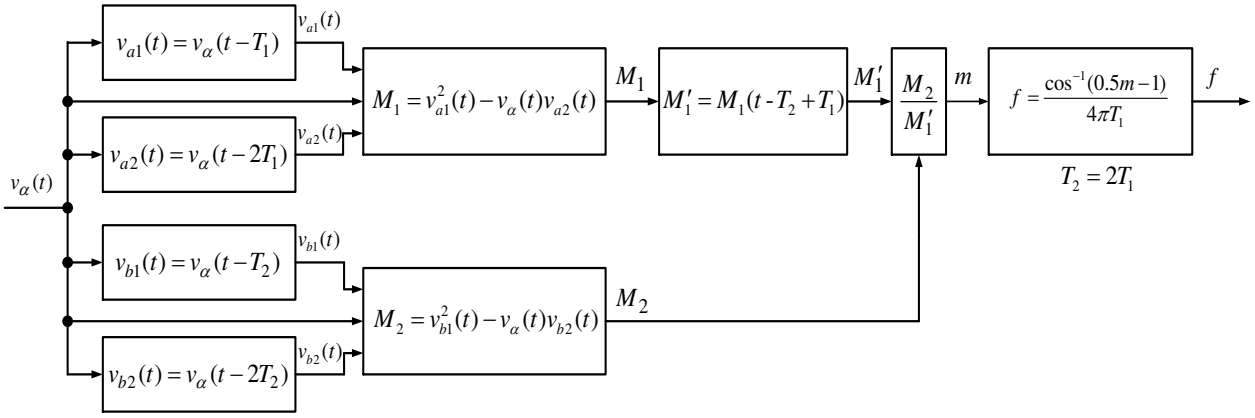

Fig. 1. Proposed frequency estimation method under ideal grid condition.

As a result, the obtained signal m is independent of the voltage amplitude, and is a function of only the grid frequency f. It means that the grid frequency can be directly solved from (5). Considering the common trigonometric function $\sin(2\omega_1 T_1) = 2\sin(\omega_1 T_1)\cos(\omega_1 T_1)$, the delayed time constant T_2 is set to $2T_1$ so that the angular frequency ω_1 and the corresponding grid frequency f can be expressed as

$$\omega_1 = \frac{\cos^{-1}(0.5m - 1)}{2T_1}, \qquad f = \frac{\omega_1}{2\pi} \tag{6}$$

As analyzed above, there are different time delays during the generation processes of M_1 and M_2, which are associated with the magnitude of the input grid voltage as shown in (3) and (4). Consequently, when the input grid voltage experiences magnitude variations, M_2/M_1 may have large transients because M_1 settles to the new steady-state value before M_2. To deal with this issue, $M_1' = M_1(t - T_2 + T_1)$ is used instead of M_1 for calculating the grid frequency. Note that this modification has no impact on the steady-state frequency estimation. Finally, the overall structure of the developed frequency estimation algorithm can be derived as shown in Fig. 1.

B. Design Considerations of the Proposed Frequency Estimation Method

It is clear from the above-mentioned analysis that two parameters T_1 and T_2 should be selected during the design of the proposed frequency estimation method. Considering the possible high-frequency random noise $v_x(t)$ in the sampled grid voltage signal as $\widetilde{v}_\alpha(t) = V_p\sin(\omega_1 t) + v_x(t)$, (3) can be rewritten as

$$\begin{aligned}\widetilde{M}_1 &= \widetilde{v}_{a1}(t)\widetilde{v}_{a1}(t) - \widetilde{v}_\alpha(t)\widetilde{v}_{a2}(t)\\ &= V_p^2\sin^2(\omega_1 T_1) + V_x^2(t - T_1)\\ &\quad + 2V_P\sin(\omega_1 t - \omega_1 T_1)V_x(t - T_1) - V_x(t)V_x(t - 2T_1)\\ &\quad - V_P\sin(\omega_1 t - 2\omega_1 T_1)V_x(t) - V_P\sin(\omega_1 t)V_x(t - 2T_1)\\ &= V_p^2\sin^2(\omega_1 T_1) + v_{n1}(t)\end{aligned} \tag{7}$$

The physical quantities with superscript $\sim$ in this paper indicate the existence of random noise. In (7)

$$\begin{aligned}&|v_{n1}(t)|\\ &= |v_x^2(t - T_1) + 2V_P\sin(\omega_1 t - \omega_1 T_1)v_x(t - T_1)\\ &\quad - v_x(t)v_x(t - 2T_1) - V_P\sin(\omega_1 t - 2\omega_1 T_1)v_x(t)\\ &\quad - V_P\sin(\omega_1 t)v_x(t - 2T_1)|\\ &\le |v_x^2(t - T_1)| + |2V_P\sin(\omega_1 t - \omega_1 T_1)v_x(t - T_1)|\\ &\quad + |v_x(t)v_x(t - 2T_1)| + |V_P\sin(\omega_1 t - 2\omega_1 T_1)v_x(t)|\\ &\quad + |V_P\sin(\omega_1 t)v_x(t - 2T_1)|\\ &\le |V_{xmax}^2| + 2|V_pV_{xmax}| + |V_{xmax}^2| + |V_pV_{xmax}| + |V_pV_{xmax}|\\ &= 2|V_{xmax}^2| + 4|V_pV_{xmax}|\end{aligned} \tag{8}$$

where V_{xmax} is the possible maximal noise level. The ratio k_1 of the noise $v_{n1}(t)$ to the dc term $V_p^2\sin^2(\omega_1 T_1)$ is defined as

$$k_1 = \frac{|v_{n1}(t)|}{|V_p^2\sin^2(\omega_1 T_1)|} \le \frac{2}{\sin^2(\omega_1 T_1)} \times \frac{|V_{xmax}^2| + 2|V_pV_{xmax}|}{|V_p^2|} \tag{9}$$

Similarly, the ratio k_2 of the noise $v_{n2}(t)$ to the dc term $V_p^2\sin^2(\omega_1 T_2)$ in the generated signal M_2 can be derived as

$$k_2 = \frac{|v_{n2}(t)|}{|V_p^2\sin^2(\omega_1 T_2)|} \le \frac{2}{\sin^2(\omega_1 T_2)} \times \frac{|V_{xmax}^2| + 2|V_pV_{xmax}|}{|V_p^2|} \tag{10}$$

Note that, with the decrease of T_1 and T_2, k_1 and k_2 increase significantly, which means weak noise rejection capability. In this study, T_1 and T_2 are set to be above 2 ms for noise rejection consideration. On the other hand, the response time of the proposed frequency estimation method is $2T_2$ ($T_2 = T_1$). Therefore, small T_2 is preferred from the viewpoint of dynamic response. In this paper, T_1 and T_2 are set to 2 ms and 4 ms, respectively, for simply verifying the feasibility of the proposed frequency estimation algorithm.

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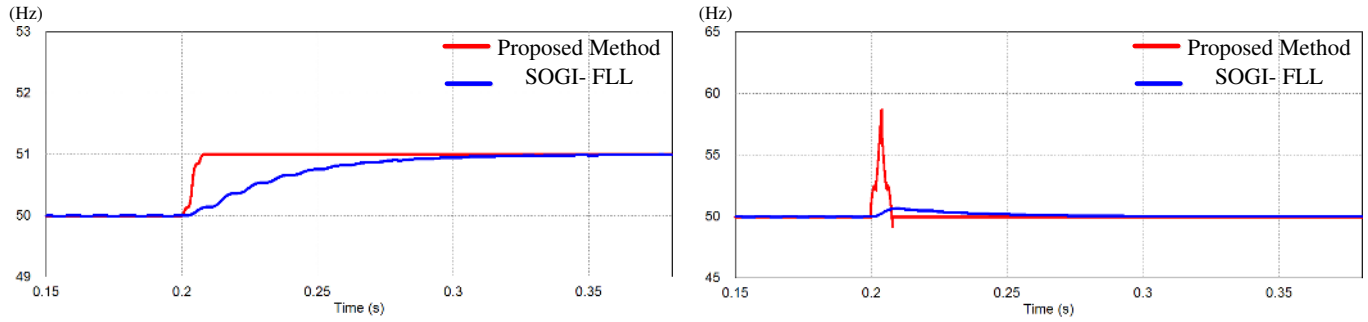

Fig. 2. Comparison between the proposed frequency estimation method and SOGI-FLL. (a) 1 Hz frequency jump. (b) 10 degrees phase jump.

C. Comparison between the Proposed Frequency Estimation Method and SOGI-FLL

As well known, PLLs synchronize with the phase of the input signal, and hence, the accuracy and dynamic response of its estimation under transient conditions are highly influenced by phase angle jumps. On the contrary, FLL estimates the frequency instead of the phase angle of the input signal, which does not experience such sudden changes. As a consequence, the FLL instead of the conventional PLL has been used in some advanced synchronization structures. Here, the SOGI-FLL discussed in [26] is used as a benchmark.

Unlike the proposed frequency estimation method which is an open-loop algorithm, the SOGI-FLL in [26] is a closed-loop feedback system, which requires elaborated tuning for achieving satisfactory dynamic and steady-state performance. The key parameters of the simulated SOGI-FLL are obtained from [26]. Fig. 2 shows the comparison results between the proposed frequency estimation method and the SOGI-FLL. The outstanding advantage of the developed method over the SOGI-FLL is its superior dynamic performance. In the case of 1 Hz frequency jump, the proposed frequency estimation method can provide very fast and smooth frequency estimation. As for 10 degrees phase jump, a large frequency transient is observed. It is because two different delay coefficients ($T_2 = 2T_1$) are used for producing signals M_1 and M_2 in the presented frequency estimation method. To best use the fast characteristic of the introduced frequency estimation method while not suffering from large frequency transients during phase angle jumps, an assisting strategy designed for obtaining smooth frequency transients is presented in Section IV. Moreover, since the discussed frequency estimation approach has no filtering capability, a proper pre-filtering solution for enhanced harmonic rejection should be considered when applying it to distorted grid condition.

III. EXTENSION OF THE PROPOSED FREQUENCY ESTIMATION METHOD TO DISTORTED GRID CONDITION

The direct application of the frequency estimation algorithm, introduced in the previous section, may suffer from errors in the estimated frequency, when considering distorted grid condition. The main sources of error are the dc offset and some dominant low-order odd harmonics in the sampled single-phase grid voltage. Before introducing the selected filtering solution, the impact of the dc offset and harmonics on the developed frequency estimation algorithm is analyzed first. Substituting $v_\alpha(t) = V_p \sin(\omega_1 t) + V_n \sin(n\omega_1 t) + V_{dc}$ into (3) yields

$$\begin{aligned} M_1 &= v_{a1}^2(t) - v_\alpha(t) v_{a2}(t) \\ &= V_p^2 \sin^2(\omega_1 T_1) + V_n^2 \sin^2(n\omega_1 T_1) + O_{dc}(t) + O_n(t) \\ O_{dc}(t) &= 2V_p V_{dc}[1 - \cos(\omega_1 T_1)] \sin(\omega_1 t - \omega_1 T_1) \\ O_n(t) &= 2V_n V_{dc}[1 - \cos(n\omega_1 T_1)] \sin(n\omega_1 t - n\omega_1 T_1) \\ &\quad + 2V_p V_n \sin(\omega_1 t - \omega_1 T_1) \sin(n\omega_1 t - n\omega_1 T_1) \\ &\quad - V_p V_n [\sin(\omega_1 t) \sin(n\omega_1 t - 2n\omega_1 T_1) \\ &\quad + \sin(\omega_1 t - 2\omega_1 T_1) \sin(n\omega_1 t)] \end{aligned} \tag{11}$$

where V_n is the amplitude of the n^{th} harmonic and V_{dc} represents the dc offset. As shown in (11), the n^{th} harmonic not only causes a dc error $V_n^2 \sin^2(n\omega_1 T_1)$, but also gives rise to oscillations $O_n(t)$. In addition, the involved dc offset is responsible for the line-frequency oscillations $O_{dc}(t)$ which are difficult to be removed. Similarly, the other intermediate signal M_2 also suffers from such dc error and oscillations. As a consequence, the proposed frequency estimation approach introduces dc errors and oscillations in the estimated frequency when considering distorted grid voltages.

The aforementioned oscillating components can be significantly rejected by using a low-pass filter with a very low cut-off frequency at the expense of dynamic speed. However, it is impossible to cancel out the induced dc errors with any filtering solutions within/after the frequency estimation block. Therefore, a pre-filtering stage must be used for removing the dc offset and harmonics from the measured grid voltage before sending it to the frequency estimation unit.

A. Pre-filtering Stage

This subsection is to introduce a simple yet effective pre-filtering solution for removing the possible dc offset and low-order odd harmonics in the sampled grid voltage. Similar to [27], a general situation where the measured grid voltage contains dc offset and odd harmonics is considered in this paper.

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TABLE I. Magnitudes of $H(jn\omega_0)$ at several harmonic frequencies

$n\omega_0$	0	ω_0	$3\omega_0$	$5\omega_0$	$7\omega_0$	$9\omega_0$	$11\omega_0$	$13\omega_0$	$15\omega_0$
$\lvert H(jn\omega_0)\rvert$	1.57	1.0	0.169	0.062	0.032	0.019	0.013	0.009	0.007

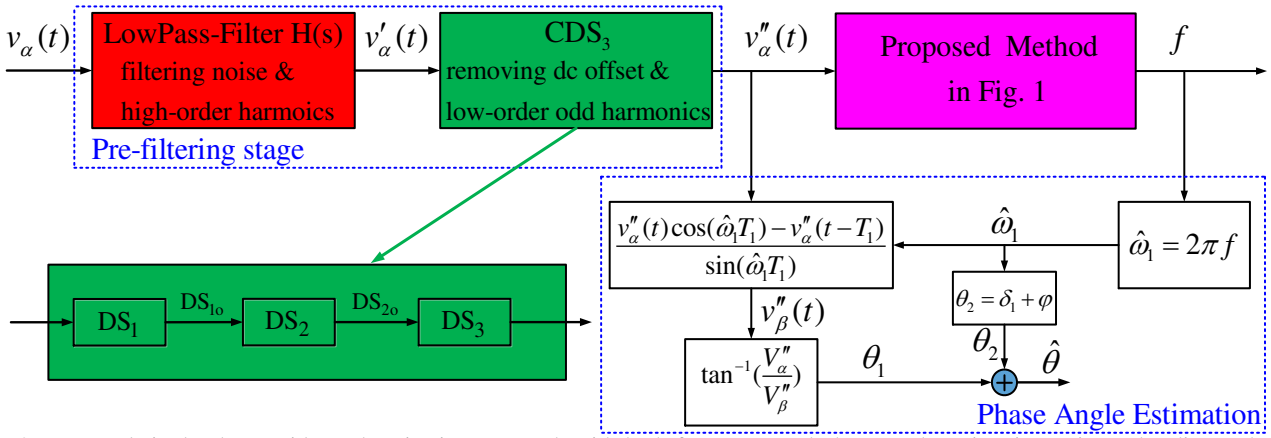

Fig. 3. Proposed single-phase grid synchronization approach with both frequency and phase angle estimation units under distorted grid voltages.

Given that the widely used second-order low-pass filter is of strong rejection capability for high-frequency components, a low-pass filter $H(s)$ with center frequency tuned at the nominal angular frequency ω_0 (314 rad/s in this paper) is first implemented for significantly attenuating high-order harmonics as well as high-frequency noises, as shown below:

$$H(s) = \frac{2\mu\omega_0}{s^2 + 2\mu s + \omega_0^2} \tag{12}$$

where μ defines the gain factor, and is set to 242.5 for achieving the fastest transient response according to [28]. Substituting $s = jn\omega_0$ into (12), the magnitude and phase expressions of $H(s)$ are

$$\begin{aligned} H(jn\omega) &= \frac{2\mu\omega_0}{\sqrt{4\mu^2 n^2\omega_0^2 + (n^2\omega_0^2 - \omega_0^2)^2}} \angle(-\delta_n) \\ \tan(\delta_n) &= \frac{2\mu n\omega_0}{\omega_0^2 - n^2\omega_0^2}, \quad n = 0, 1, 3, 5, 7, 9 \cdots\cdots \end{aligned} \tag{13}$$

The magnitudes of $H(s)$ at several harmonic frequencies of interest are listed in Table I. It is obvious that the fine-tuned low-pass filter $H(s)$ can let pass the fundamental voltage component while significantly attenuating high-order odd harmonics. However, the dc offset and low-order odd harmonics still remain in the output of $H(s)$. According to [29], the DSC technique can be employed for eliminating the specific-order harmonic. Consequently, a cascaded DSC (CDSC) module CDS_3 is designed to deal with the negative influence of the remaining dc offset and low-order odd harmonics (3^{rd}, 5^{th}, 7^{th} and 9^{th}) on the estimated frequency. For the purpose of illustration, the input $v'_\alpha(t)$ to the CDS_3 module is assumed to be

$$\begin{aligned} v'_\alpha(t) = {} & V_1\sin(\omega_1 t) + V_3\sin(3\omega_1 t) + V_5\sin(5\omega_1 t) \\ & + V_7\sin(7\omega_1 t) + V_9\sin(9\omega_1 t) + V_{dc} \end{aligned} \tag{14}$$

The first DSC operator DS_1 with a delay of $\frac{1}{6}$ of the fundamental period $T_f = \frac{2\pi}{\omega_1}$ is used to remove both the 3^{rd} and 9^{th} harmonics, and its output is derived as

$$\begin{aligned} DS_{1o}(t) &= \frac{v'_\alpha(t) + v'_\alpha(t - \frac{T_f}{6})}{2} \\ &= V_1\cos(\frac{\omega_1 T_f}{12})\sin(\omega_1 t - \frac{\omega_1 T_f}{12}) \\ &\quad + V_{51}\sin(5\omega_1 t + \varphi_{51}) + V_{71}\sin(7\omega_1 t + \varphi_{71}) + V_{dc} \end{aligned} \tag{15}$$

The second DSC operator DS_2 with a delay of $\frac{1}{10}$ of the fundamental period is adopted to eliminate the 5^{th} harmonic. The output of DS_2 is expressed as

$$\begin{aligned} DS_{2o}(t) &= \frac{DS_{1o}(t) + DS_{1o}(t - \frac{T_f}{10})}{2} \\ &= V_1\cos(\frac{\omega_1 T_f}{12})\cos(\frac{\omega_1 T_f}{20})\sin(\omega_1 t - \frac{\omega_1 T_f}{12} - \frac{\omega_1 T_f}{20}) \\ &\quad + V_{72}\sin(7\omega_1 t + \varphi_{72}) + V_{dc} \end{aligned} \tag{16}$$

Then, both the 7^{th} harmonic and dc offset are removed by the third DSC operator DS_3 with a delay of $\frac{1}{7}$ of the fundamental period as

$$\begin{aligned} v''_\alpha(t) &= DS_{2o}(t) - DS_{2o}(t - \frac{T_f}{7}) \\ &= 2V_1\cos(\frac{\omega_1 T_f}{12})\cos(\frac{\omega_1 T_f}{20})\sin(\frac{\omega_1 T_f}{14}) \\ &\quad \sin(\omega_1 t - \frac{\omega_1 T_f}{12} - \frac{\omega_1 T_f}{20} - \frac{\omega_1 T_f}{14} + \frac{\pi}{2}) \\ &= V_1''\sin(\omega_1 t - \varphi) \end{aligned} \tag{17}$$

The total time delay introduced by the CDS_3 module is $0.41T_f$, i.e., 8.2 ms for a 50 Hz power grid. Thus, the dc offset and the most significant low-order odd harmonics can

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be significantly rejected when the sampled grid voltage passes through the low-pass filter $H(s)$ and the CDSC module CDS_3. As a matter of fact, the real power grid may experience frequency variations, but most cases involve only small frequency variations, such as the ones less than 0.2 Hz in China. Given that the designed CDS_3 based on constant fundamental frequency can still strongly reject the distortions of interest under slightly varying frequency conditions, the fundamental period T_f is assumed to be 50 Hz and remains constant in this paper. In cases where the grid frequency undergoes large deviations, T_f should be adjusted online according to the estimated frequency by the frequency estimation stage.

B. Phase Angle Estimation

Since the phase angle of the grid voltage is essential for the real-time control of grid-connected converters, the established frequency estimation unit should be equipped with a phase angle estimation unit as seen in Fig. 3. The estimated angular frequency $\hat{\omega}_1 = 2\pi f$ is sent to the OSG module for generating an orthogonal signal $v''_\beta(t)$ with respect to $v''_\alpha(t)$ with the OSG technique in [30] as

$$v''_\beta(t) = \frac{v''_a(t)\cos(\hat{\omega}_1 T_1) - v''_a(t-T_1)}{\sin(\hat{\omega}_1 T_1)} \tag{18}$$

Subsequently, the phase angle θ_1 of $v''_\alpha(t)$ is obtained by using $\tan^{-1}(\frac{v''_\alpha(t)}{v''_\beta(t)})$. Because the pre-filtering stage introduces extra phase delay on the fundamental voltage component, θ_1 is not locked to the actual phase angle $\hat{\theta}$ of the fundamental grid voltage. Hence, the difference θ_2 between θ_1 and $\hat{\theta}$ must be compensated. Under the frequency locked condition, θ_2 can be calculated based on (13) and (17) as

$$\begin{aligned} \theta_2 &= \delta_1 + \varphi \\ \tan(\delta_1) &= \frac{2\mu\hat{\omega}_1}{\omega_0^2 - \hat{\omega}_1^2} \Rightarrow \delta_1 \approx \frac{\pi}{2} - \frac{\omega_0^2 - \hat{\omega}_1^2}{2\mu\hat{\omega}_1} \\ \varphi &= \frac{43\hat{\omega}_1 T_f}{210} - \frac{\pi}{2} \end{aligned} \tag{19}$$

where δ_1 is the phase delay arising from the employed low-pass filter $H(s)$ in (13) and φ is induced by the module CDS_3 in (17). Therefore, the actual phase angle of the grid voltage can be achieved as

$$\hat{\theta} = \theta_1 + \theta_2 \tag{20}$$

Although the use of the voltage magnitude is avoided during the frequency measurement process in this work, the magnitude of the grid voltage can be obtained if necessary and is given by

$$\hat{V}_p = \sqrt{\frac{M_1}{\sin^2(\hat{\omega}_1 T_1)}} \quad or \quad \sqrt{\frac{M_2}{\sin^2(\hat{\omega}_1 T_2)}} \tag{21}$$

where $\hat{V}_p$ represents the estimated magnitude of the grid voltage.

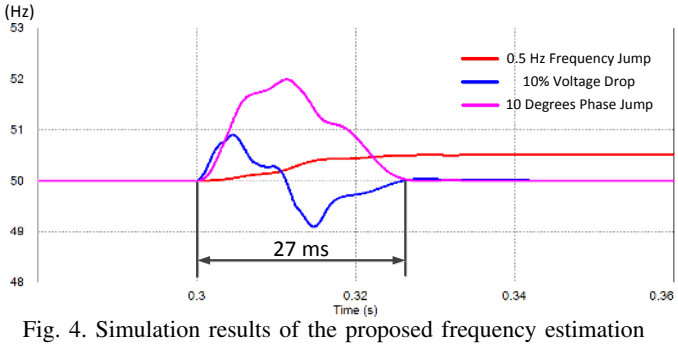

Fig. 4. Simulation results of the proposed frequency estimation method with pre-filtering stage under different grid disturbances.

IV. TRANSIENT PROCESS SMOOTHING (TPS)

Fig. 4 depicts the simulation results of the proposed frequency estimation method under different grid disturbances. Note that, the proposed frequency estimation method used in the following sections represents the one which is equipped with the designed pre-filtering stage as shown in Fig. 3. As shown in Fig. 4, the presented frequency estimation algorithm has nearly the same settling times in spite of different types of grid disturbances. This is because the settling times of the pre-filtering stage and the frequency estimation stage are constant and independent of grid disturbances. Compared with the 0.5 Hz frequency jump, both the 10 degrees phase jump and 10% voltage drop cause larger frequency transients. As a matter of fact, the voltage is more likely to vary than the frequency in a real power grid. Furthermore, the allowable variation range of the grid frequency is generally small in normal operation mode such as 0.2 Hz in China, while the grid voltage may suffer from the large and dramatic increase or decrease. Consequently, voltage variations are more challenging for the developed frequency estimation approach than frequency deviations. To deal with this issue, a transient process smoothing (TPS) unit is designed to achieve smooth frequency transients in cases of fast and large voltage changes in this section, which is illustrated below and in Fig. 5.

Step 1: Calculate the absolute error between the currently estimated frequency f and the previous steady-state frequency f_s, $|f - f_s|$.

Step 2: When $|f - f_s| > 0.1$ Hz, T_t starts to increase. When $T_t < T_{th}$ ($T_{th} = 5$ ms), the previous steady-state frequency is used as the output grid frequency f_g at present.

Step 3: If $|f - f_s| > 0.5$ Hz is met before T_t increases to T_{th}, then let the output frequency f_g be equal to the previous steady-state frequency until a new steady state arrives; otherwise f_g is equal to f when $T_t > T_{th}$.

Step 4: After the the frequency estimation unit settles to a new steady state, f is delivered to f_g and T_t is reset to zero. Meanwhile, the steady-state frequency f_s is updated according to f.

The simulation results of the proposed frequency estimation method without and with the TPS unit are shown in Fig. 6. It is clear that the frequency estimation with TPS has negligible frequency transients in response to either 10 degrees phase jump or 10% voltage drop. Moreover, the TPS unit only affects the transient processes, while not impacting the

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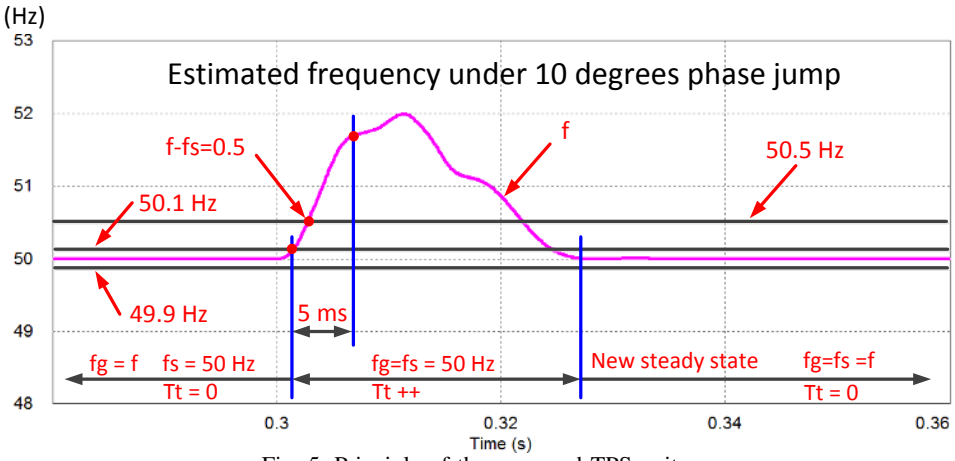

Fig. 5. Principle of the proposed TPS unit.

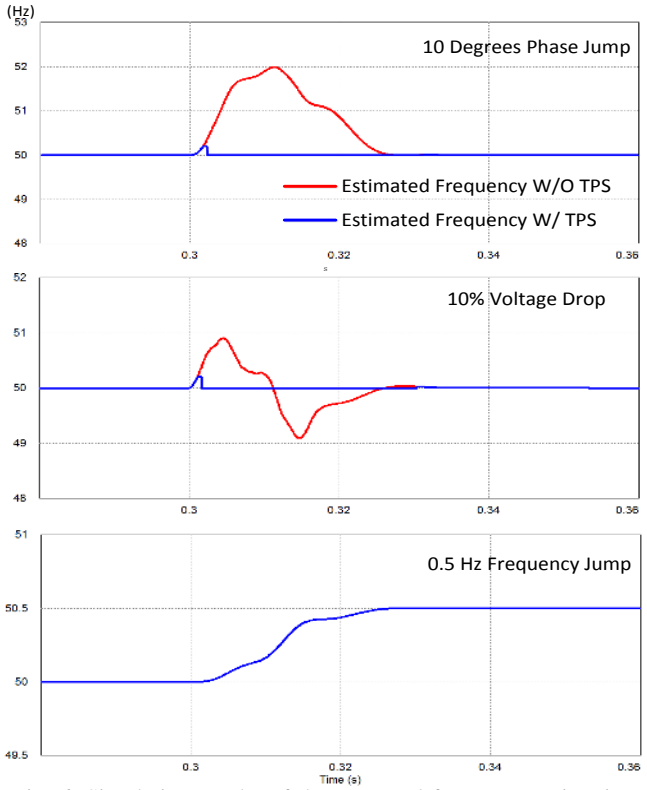

Fig. 6. Simulation results of the proposed frequency estimation method w/o and w/ TPS.

steady-state performance. In the case of 0.5 Hz frequency jump, the estimated frequency with TPS always overlaps with that without TPS. This is because the small frequency variation cannot induce fast and large changes of the estimated frequency so that the TPS unit cannot be activated. Similarly, the estimated frequency of the proposed method in response to small and slow voltage variations also undergoes slow changes so that the TPS would not take its role as in the case of 0.5 Hz frequency jump. It matches well with the design purpose that the TPS unit is mainly adopted for cases with relatively fast and large voltage variations, which cause large frequency overshoots or undershoots in both the proposed grid synchronization approach and conventional PLLs. Finally, the grid synchronization approach can be further improved with the designed TPS unit as shown in Fig. 7.

V. SIMULATION RESULTS

The performance of the proposed single-phase grid synchronization approach is firstly verified through simulation results. For the purpose of comparison, the advanced PLLs, CDSC-EPLL [22] and MHDC-PLL [23], are tested as well. These three methods are tested under distorted voltages and under other grid disturbances such as phase jump, voltage sag and frequency variation. The MAF-PLL, which can be also used for the accurate grid synchronization under distorted grid voltages, is equivalent to CDSC-PLL under certain conditions [29], and,therefore, is omitted here. The open-loop grid fundamental and harmonic component decomposition method in [31] can be used for single-phase grid synchronization as well. However, to make it applicable in frequency varying cases, a PLL must be used instead of the open-loop magnitude and phase estimation unit for online adjusting the delay factors of the involved CDSC blocks [31]. With such a modification, the resulting method becomes a closed-loop system, and is similar to the previous CDSC based PLLs from the view point of concept. Hence, this paper did not compare this method with the proposed one for brevity.

A. Frequency Variation

The performance of the proposed method for a frequency step change of 0.5 Hz is compared with those of CDSC-EPLL and MHDC-PLL in Fig. 8. It can be observed that the proposed method shows a faster dynamic response than the CDSC-EPLL and MHDC-PLL in terms of both the frequency and phase angle estimations. It should be noted that the MHDC-PLL presents some oscillations on both the estimated frequency and phase angle due to the imperfect response of the discrete implementation of the quarter-cycle delay block [23].

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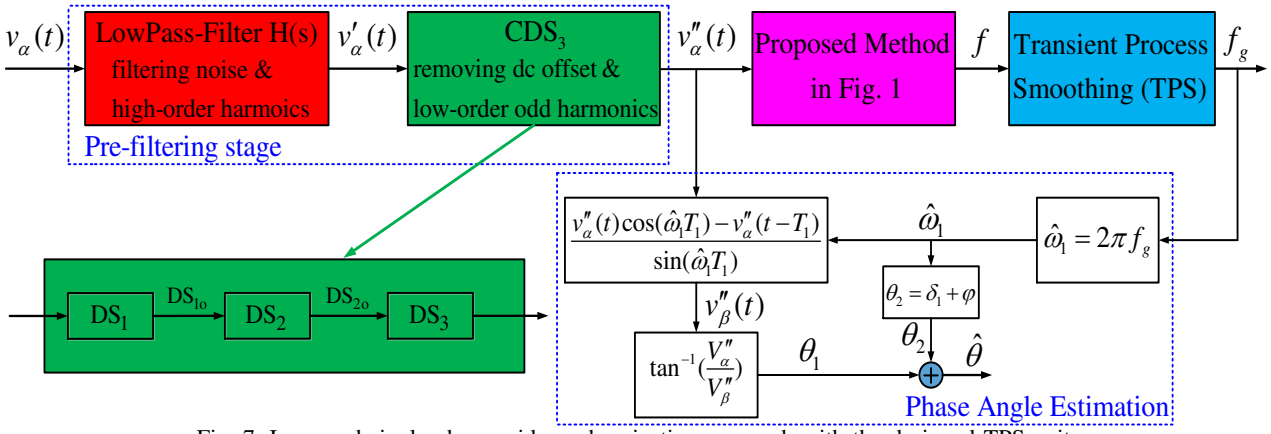

Fig. 7. Improved single-phase grid synchronization approach with the designed TPS unit.

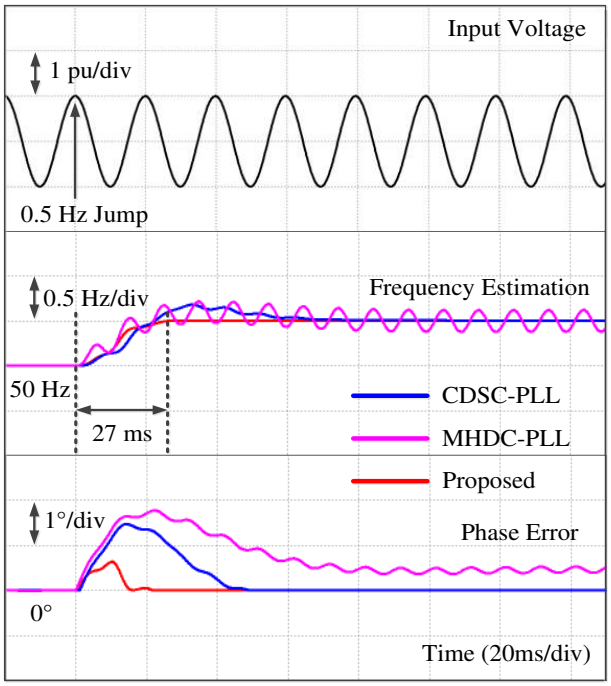

Fig. 8. Simulation under 0.5 Hz step change in frequency.

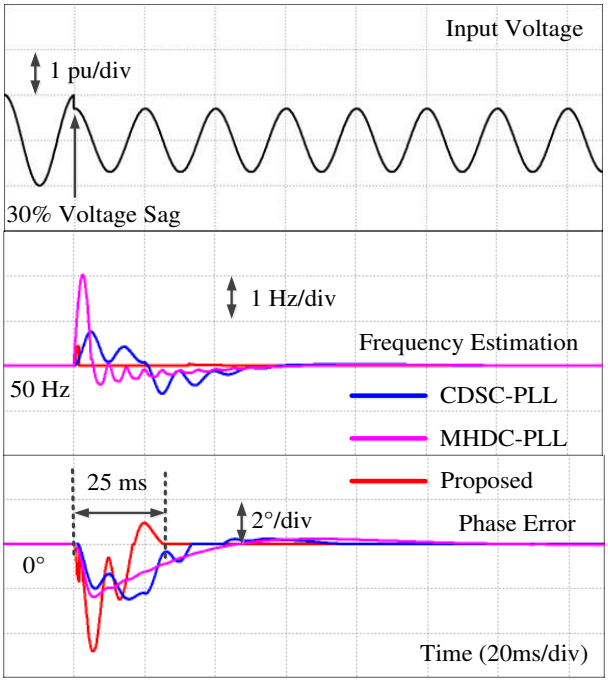

Fig. 9. Simulation under 30% voltage sag.

B. Voltage Sag

Fig. 9 illustrates the performance of the developed method, CDSC-EPLL and MHDC-PLL under the grid voltage sag of 0.3 p.u. In terms of the estimated frequency, the proposed method shows relatively short and negligible transient, while 0.48 Hz and 2 Hz overshoots are present in CDSC-EPLL and MHDC-PLL, respectively. Besides, CDSC-EPLL and MHDC-PLL take more than two cycles to settle to a new steady state. Although the proposed approach presents a larger phase undershoot (4.8 degrees) than CDSC-EPLL and MHDC-PLL, its phase error decreases below those of CDSC-EPLL and MHDC-PLL rapidly and reduces to zero within 25 ms. It should be mentioned that the estimated phase angle of the proposed method takes a little more than one cycle to settle to a new operating condition due to the time delay of the pre-filtering stage, although the accurate frequency can be obtained with nearly no delay.

C. Phase Angle Jump

Fig. 10 demonstrates the performance of these three synchronization methods in response to a phase angle jump of 40 degrees. It can be noted that CDSC-EPLL and MHDC-PLL take much longer time than the proposed method to settle to a new operating state. The frequency overshoot and phase angle undershoot are measured as 8 Hz and 15.7 degrees, and 9 Hz and 7.6 degrees with CDSC-EPLL and MHDC-PLL, respectively. In comparison, the estimated frequency shows no obvious variations, as well as the phase error exhibits relatively small undershoot and becomes zero within 22 ms, in the proposed approach.

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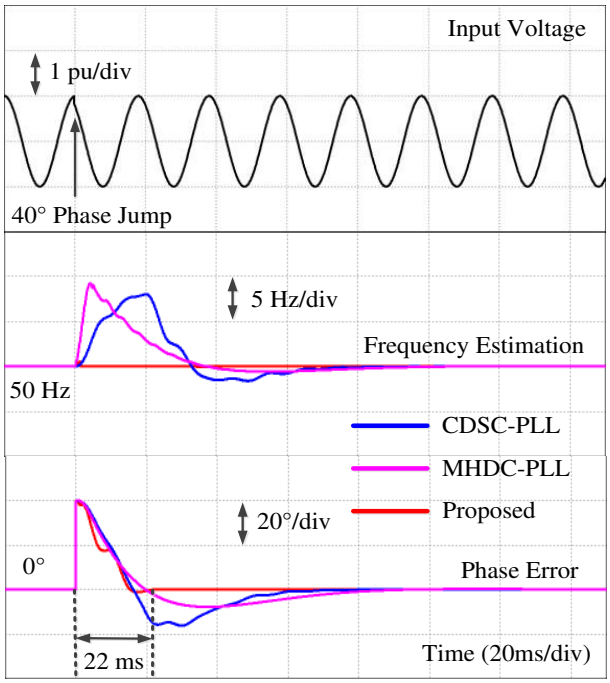

Fig. 10. Simulation under 40 degrees phase angle jump.

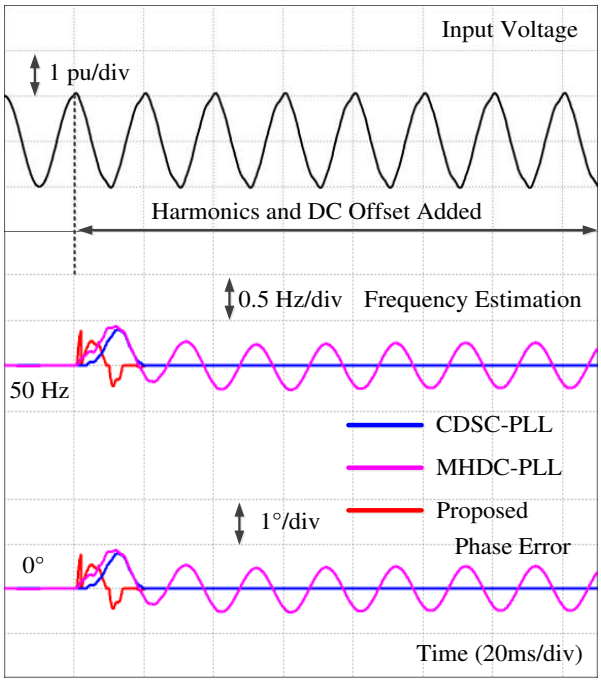

Fig. 11. Simulation under distorted grid voltages.

D. Distorted Grid Voltages

Finally, the low-order harmonics ($3\%\ 3^{rd}, 2\%\ 5^{th}, 2\%\ 7^{th}$) and dc offset ($2\%$) are added to the voltage signal for evaluating the performance of the developed method, CDSC-EPLL and MHDC-PLL under distorted conditions in Fig. 11. It is clear that both the proposed technique and CDSC-EPLL can provide accurate frequency and phase angle estimations even after the low-order harmonics and dc offset are added. However, obvious low-frequency oscillations can be seen on the estimated frequency and phase angle of MHDC-PLL. It is because the design of MHDC-PLL in [23] does not consider the existence of dc offset in the measured grid voltage signal.

VI. EXPERIMENTAL RESULTS

Experiments of the proposed single-phase grid synchronization method using a DSP chip (TMS30F28335) based platform are performed to validate the former analysis. The artificially produced grid voltage by using a programmable signal generator is detected by an A/D sensing board. Then, the sampled grid voltage is sent to the DSP chip, where the proposed approach is implemented with C code, for frequency and phase angle measurement. For the purpose of better observation, the sampled grid voltage, estimated frequency, and phase angle error are converted to analog signals for display in the oscilloscope by using an external D/A circuit. The initial amplitude of the grid voltage is set as the nominal voltage (1 p.u.) and the frequency as 50 Hz. All the operations are conducted at 10 kHz sampling frequency. Fig. 12 depicts the corresponding synchronization signals estimated by the developed method under several grid conditions: a) a frequency step change of 0.5 Hz, b) 30% voltage sag, c) 40 degrees phase angle jump, and d) distorted grid voltage with low-order harmonics ($3\%\ 3^{rd}, 2\%\ 5^{th}, 2\%\ 7^{th}$) and dc offset ($2\%$). As shown in Fig. 12(a), the frequency can be estimated smoothly and quickly with the proposed method for a small frequency jump condition. In addition, the estimated frequency has negligible transient process in both Fig. 12(b) and Fig. 12(c), which is due to the developed TPS unit. It is worth noting that the settling time of the developed grid synhcronization method is less than 30 ms in all the experimental cases, while it is seldom to be achieved in previous PLLs that can ensure zero steady-state error under distorted conditions. Considering the distorted grid voltage with significant harmonics and dc offset, the proposed approach can still estimate the required information without steady-state error and ripples as shown in Fig. 12(d). Therefore, both the harmonic-rejection robustness and fast dynamic response can be achieved by using the proposed synchronization method. It can be also observed that all the experimental results shown in Fig. 12 match well with the simulation results in the last section, which further validate the theoretical analysis mentioned above.

VII. CONCLUSIONS

In this paper, a novel open-loop frequency estimation algorithm is firstly developed for the purpose of fast frequency measurement. With the help of the proposed frequency estimation algorithm, a single-phase grid synchronization method, which can provide enhanced stability, fast dynamic performance, and strong harmonics rejection capability, is then introduced in this paper. In terms of the open-loop structure, the presented grid synchronization approach suffers from no stability issues. The rejection capability for the possible dc

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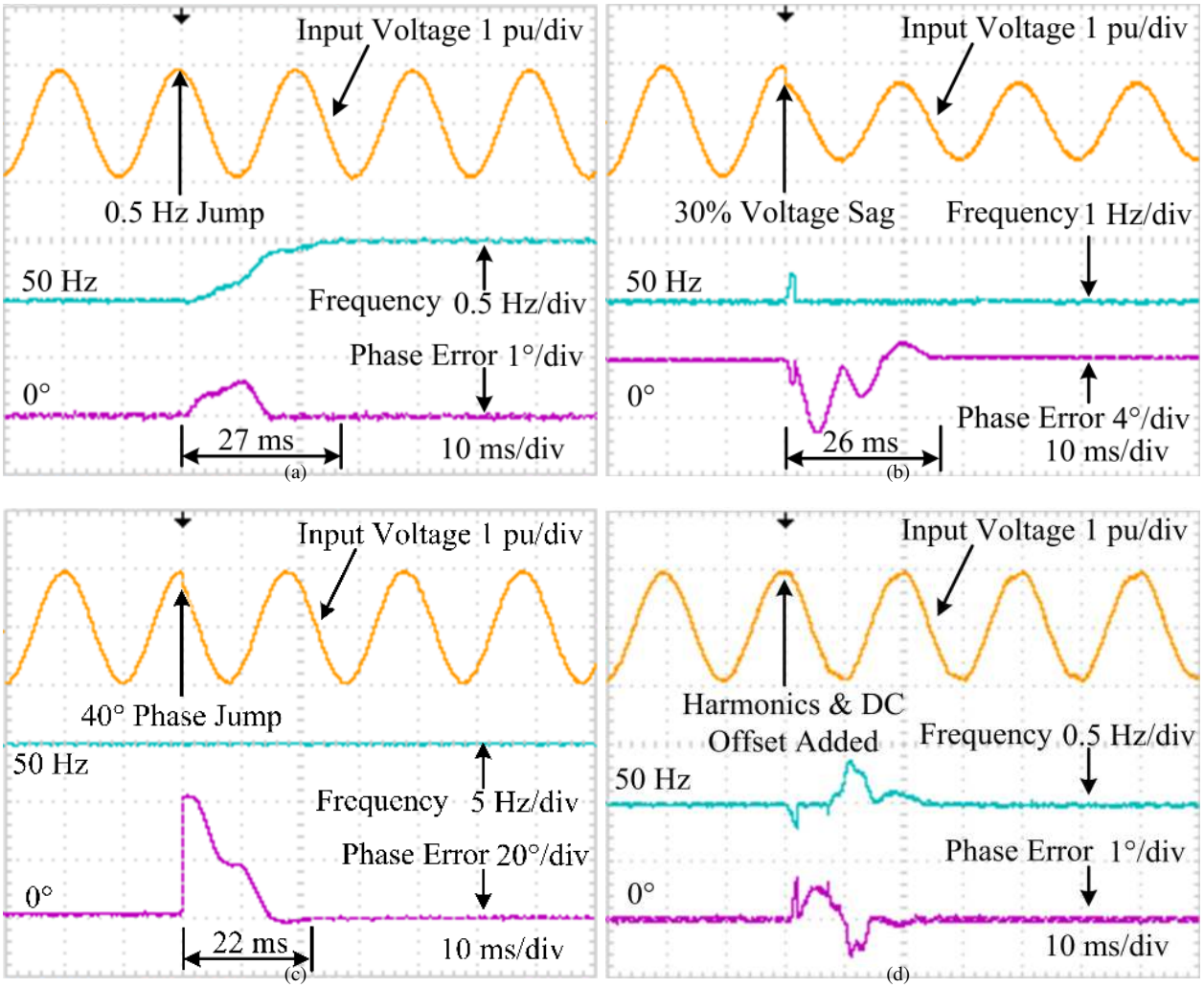

Fig. 12. Experimental results. (a) 0.5 Hz frequency jump. (b) 30% voltage sag. (c) 40 degrees phase jump. (d) Harmonics and dc offset added.

offset and harmonics is achieved by using a second-order low-pass filter and a CDSC module in the presented grid synchronization approach. The combination of the second-order low-pass filter and the DSC technique is beneficial for enhancing the harmonics rejection performance and also simplifying the design of the pre-filtering stage. With the designed pre-filtering stage, accurate grid synchronization performance can be achieved even under distorted conditions. Given that the estimated frequency would experience large transients when the grid voltage undergoes large amplitude and phase angle jumps, TPS is designed for obtaining smooth frequency estimations in cases of relatively fast and large voltage variations. The simulation and experimental results demonstrate that the proposed grid synchronization algorithm can provide faster and more accurate performance than CDSC-PLL and MHDC-PLL, under several grid disturbances (e.g., voltage sag, phase jump) and under distorted grid voltages.

REFERENCES

[1] IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems, IEEE Std. 1547-2003, pp. 1-27, 2003.

[2] B.-I. Craciun, T. Kerekes, D. Sera, and R. Teodorescu, "Overview of recent grid codes for PV power integration," in Proc. OPTIM, pp. 959-965, 2012.

[3] R. Teodorescu, M. Liserre, and P. Rodriguez, "Grid Converters for Photovoltaic and Wind Power Systems," New York, NY, USA: Wiley, 2011.

[4] H. Kobayashi, "Fault ride through requirements and measures of distributed PV systems in Japan," in Proc. IEEE-PES General Meet., Jul. 2226, 2012, pp. 16.

[5] Reference Technical Rules for Connecting Users to the Active and Passive LV Distribution Companies of Electricity, Comitato Elettrotecnico Italiano, Standard CEI 0-21, 2012.

[6] M. S. Reza, M. Ciobotaru, and V. G. Agelidis, "Accurate estimation of single-phase grid voltage parameters under distorted conditions," IEEE Trans. Power Del., vol. 29, no. 3, pp. 74-80, Feb. 2014.

[7] O. Vainio and S. J. Ovaska, "Noise reduction in zero crossing detection by predictive digital filtering," IEEE Trans. Ind. Electron., vol. 42, no. 1, pp. 58-62, Feb. 1995.

[8] A. Routray, A. K. Pradhan and K. P. Rao, "A novel Kalman filter for frequency estimation of distorted signals in power systems," IEEE Trans. Instrum. Meas., vol. 51, no. 3, pp. 469-479, June 2002.

[9] H. S. Song, N. Kwanghee and P. Mutschler, "Very fast phase angle estimation algorithm for a single-phase system having sudden phase

angle jumps," in Conf. Rec. 37th IEEE IAS Annu. Meeting, pp. 925-931, 2002.

[10] L. L. Lai, C. T. Tse, W. L. Chan and A. T. P. So, "Real-time frequency and harmonic evaluation using artificial neural networks," IEEE Trans. Power Del., vol. 14, no. 1, pp. 52-59, Jan. 1999.

[11] D. Yazdani, A. Bakhshai, G. Joos and M. Mojiri, "A nonlinear adaptive synchronization technique for grid-connected distributed energy sources," IEEE Trans. Power Electron., vol. 23, no. 4, pp. 2181-2186, July 2008.

[12] W. Li, X. Ruan, C. Bao, D. Pan and X. Wang, "Grid synchronization systems of three-phase grid-connected power converters: A complex-vector-filter perspective," IEEE Trans. Ind. Electron., vol. 61, no. 4, pp. 1855-1870, Apr. 2014.

[13] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications," IEEE Trans. Ind. Electron., vol. 55, no. 8, pp. 2923-2932, August 2008.

[14] M. Karimi-Ghartemani, and M. R. Iravani, "A method for synchronization of power electronic converters in polluted and variable-frequency environments," IEEE Trans. Power Syst., vol. 19, no. 3, pp. 1263-1270, August 2004.

[15] R. Zhang, M. Cardinal, P. Szczesny, and M. Dame, "A grid simulator with control of single-phase power converters in DQ rotating frame," in Proc. IEEE Power Electron. Spec. Conf., pp. 1431-1436, 2002.

[16] R. Y. Kim, S. Y. Choi, and I. Y. Suh, "Instantaneous control of average power for grid tie inverter using single phase DQ rotating frame with all pass filter," in Proc. IEEE Ind. Electron. Conf., Busan, Korea, pp. 274-279, 2004.

[17] M. Saitou, and T. Shimizu, "Generalized theory of instantaneous active and reactive powers in single-phase circuits based on Hilbert transform," in Proc. 33rd Annu. IEEE PESC, pp. 1419-1424, 2002.

[18] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," in Proc. 37th IEEE PESC, pp. 1511-1516, 2006.

[19] P. Kanjiya, V. Khadkikar, and M. El Moursi, "A Novel Type-1 Frequency-Locked Loop for Fast Detection of Frequency and Phase with Improved Stability Margins," IEEE Trans. Power Electron., vol. 31, no. 3, pp. 2550-2561, Mar. 2016.

[20] K.-J. Lee, J.-P. Lee, D. Shin, D.-W. Yoo, and H.-J. Kim, "A novel grid synchronization PLL method based on adaptive low-pass notch filter for grid-connected PCS," IEEE Trans. Ind. Electron., vol. 61, no. 1, pp. 292-301, Jan. 2014.

[21] S. Golestan, M. Ramezani, J. M. Guerrero, et al., "Moving Average Filter Based Phase-Locked Loops: Performance Analysis and Design Guidelines," IEEE Trans. Power Electron., vol. 29, no. 6, pp. 2750-2763, June 2014.

[22] F. Wu, D. Sun, et al., "Influence of Plugging DC Offset Estimation Integrator in Single-Phase EPLL and Alternative Scheme to Eliminate Effect of Input DC Offset and Harmonics," IEEE Trans. Ind. Electron., vol. 62, no. 8, pp. 4823-4831, Aug. 2015.

[23] L. Hadjidemetriou, E. Kyriakides, Y. Yang and F. Blaabjerg, "A synchronization method for single-phase grid-tied inverters," IEEE Trans. Power Electron., vol. 31, no. 3, pp. 2139-2149, March 2016.

[24] S. Golestan, M. Monfared, and F. D. Freijedo, "Design-oriented study of advanced synchronous reference frame phase-locked loops," IEEE Trans. Power Electron., vol. 28, no. 2, pp. 765-778, Feb. 2013.

[25] M. K. Ghartemani, S. A. Khajehoddin, P. K. Jain, and A. Bakhshai, "Problems of startup and phase jumps in PLL systems," IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1830-1838, Apr. 2012.

[26] P. Rodrguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 127-138, 2011.

[27] Z. Dai, W. Lin, and H. Lin, "Estimation of Single-Phase Grid Voltage Parameters with Zero Steady-State Error," IEEE Trans. Power Electron., vol. 31, no. 5, pp. 3867-3879, May 2016.

[28] F. R. Xiao, L. Dong and X. Z. Liao, "Fast reactive current detection method for single-phase grid-connected inverters," IET Power Electron., vol. 9, no. 3, pp. 401-407, 2016.

[29] S. Golestan, M. Ramezani, J. M. Guerrero and M. Monfared, "dq-frame cascaded delayed signal cancellation-based PLL: Analysis, design, and comparison with moving average filter-based PLL," IEEE Trans. Power Electron., vol. 30, no. 3, pp. 1618-1632, March 2015.

[30] L. Xiong, F. Zhuo, F. Wang, X. Liu, and M. Zhu, "A Fast Orthogonal Signal-Generation Algorithm Characterized by Noise Immunity and High Accuracy for Single-Phase Grid," IEEE Power Electron., vol. 31, no. 3, pp. 1847-1851, March 2016.

[31] Y. F. Wang and Y. W. Li, "A grid fundamental and harmonic component detection method for single-phase systems," IEEE Trans. Power Electron., vol. 28, no. 5, pp. 2204-2213, May 2013.