A Novel Packaging with Direct Dielectric Liquid Cooling for High Voltage Power Electronics

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***Abstract*—This work investigates a packaging solution for high voltage semiconductors (20 kV), allowing for a dramatic reduction in size and complexity of power electronics modules. The standard packaging structures typically introduce a competition between electrical insulation (which requires thick insulating layers) and thermal performance (where thin, high thermal conductivity layers are preferred). Here, we introduce a concept which addresses this competition and is based on direct cooling using dielectric liquid. Single-chip heatsinks are designed, optimized using computational fluid dynamics (CFD), built and tested.**

***Index Terms*—High voltage, Insulation, Packaging, Dielectric fluid, CFD, Cooling, power electronics**

I. Introduction

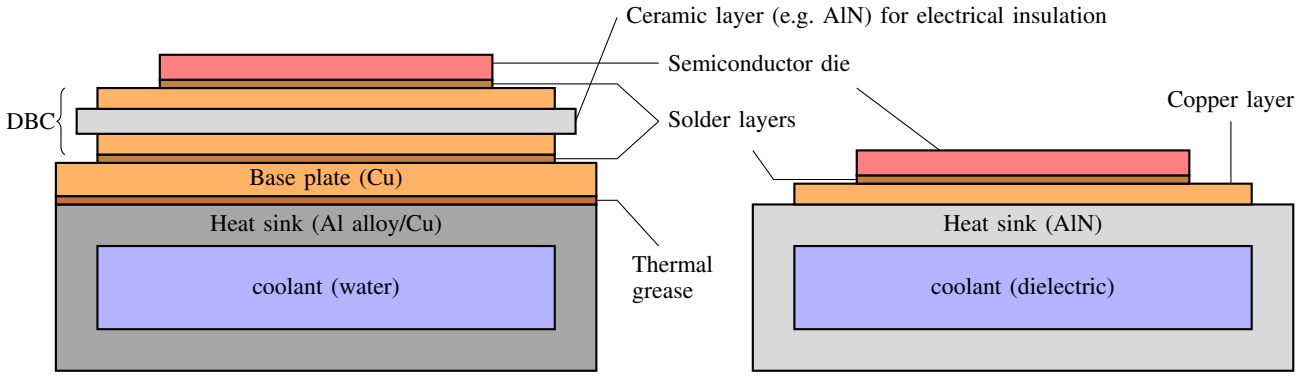
With the recent development of the silicon carbide (SiC) technology, higher voltage power devices become possible. For example, $> 3.3\,\mathrm{kV}$ SiC power devices are discussed in [1]. In [2], a 10 kV DMOSFET is presented and a switching test for 20 kV SiC IGBT is demonstrated in [3]. The Wolfspeed company [3] also developed 10 kV and 15 kV MOSFETs.

While most research studies focus on the high voltage semiconductor devices themselves, their packaging also presents some technical challenges, particularly regarding electrical insulation and thermal management. In traditional high voltage packages, a thick solid layer (typically aluminium nitride ceramic) is required for the electrical insulation, which degrades the cooling performance. While high voltage SiC devices exhibit very attractive electrical performances, these are found to be very sensitive to the temperature, with a dramatic drop in the on-state resistance of SiC MOSFET (e.g. a 2 to 3-fold increase in on-state resistance for 10 kV MOSFETs between 25 and 150 °C [4]). Various studies showed that it is preferable to operate high voltage SiC devices below 100 °C junction temperature to take full advantage of their performance [5], [6], as their on-state resistance increases dramatically with temperature.

Mouawad [7] and Johnson [8] introduced a packaging technology for a highly integrated 10 kV SiC MOSFET module which addresses both the insulation constraint and the thermal management. The module uses stacked DBA (Direct Bonded Aluminium (AlN)) substrates (selected for their high thermal-cycling capability) to provide for a more uniform electric field distribution, allowing a reduction in the total thickness of the ceramic compared to a single-layer substrate. The cooling system of the same package is investigated in [15]: a cooling system, based on jet impingement was directly attached to the backside of the substrate stack.

In [9] a metallized ZBC substrate (ultra-thin Zirconia Bonded Copper) was used in order to improve the power density with smaller volume and weight. The main disadvantage of standard DBC substrates for high voltage applications is the occurrence of partial discharges at relatively low voltages [10]. Another example of improved trade-off between electrical insulation and thermal performance was investigated in [11], where protruding patterns in the ceramic were found to improve the electrical insulation compared with plain ceramic of the same total thickness. However, this study did not explicitly address cooling performance. On the contrary, Schnur [12] and Sharma [13] investigated the use of di-electric liquid to cool power electronic modules, but focused on the thermal aspects rather than on electrical insulation. Their approach is based on a textured copper baseplate to improve heat exchange with the fluids. For high voltage modules an electrical insulating ceramic substrate is beneficial. Due to high breakdown field and excellent thermal conductivity ($170\,\mathrm{W\,m^{-1}\,K^{-1}}$), aluminium nitride (AlN) ceramic is preferred compared to ceramic materials such as alumina or silicon nitride [14].

The present work investigates a novel packaging solution for high-voltage semiconductors that enables both efficient cooling and good insulation, while drastically reducing the size and complexity of power electronic modules. A dielectric fluid is used as both a coolant and an insulator to relieve some of the constraint of the solid insulation layers, and a ceramic structure provides mechanical support, internal insulation and heat exchange surface. This packaging approach is presented in section II. It is then optimized by the means of Computational Fluid Dynamics (CFD) modelling (section III) and the predictions are compared with experimental results (section IV).



(a) Traditional module packaging

(b) Novel embedded packaging

Fig. 1: Schematic comparison between the traditional and the novel power module packaging

II. Integrated cooling system

Fig. 1 shows a comparison between the traditional power module/cooler structure and that proposed in this paper. In the traditional structure (Fig. 1a), the chip is attached onto a Direct Bonded Substrate (DBC), whose ceramic layer ensures electrical insulation. This DBC is then soldered onto a thick metal baseplate (for mechanical strength), and this baseplate is screwed onto a water-cooled cold-plate through a layer of thermal interface material.

The proposed structure (Fig. 1b) does away with most of these layers by integrating the liquid cold-plate directly into the ceramic layer. With this packaging, a dramatic reduction in size and complexity of power electronics modules is achieved. Furthermore, the thermal path from the semiconductor device to the coolant is reduced, which can lead to a better cooling performance.

A. Selection of dielectric liquid

In the proposed design, the electrical insulation relies not only on the ceramic, but also on the dielectric cooling fluid. A dielectric fluid with good thermal and electrical properties must therefore be selected. An ideal coolant has high heat capacity, high thermal conductivity, low viscosity and low GWP value (Global Warming Potential, expressed with CO_2 as a reference). Furthermore, a fluid with high electrical insulation is required, as well as with a permittivity matching that of the cold plate ceramic (AlN) so that the electric field is uniformly distributed over the ceramic/fluid domain.

Based on the performance data of the chips ($9.1\,\mathrm{mm} \times 9.1\,\mathrm{mm}$), a heating power of $\dot{Q} = 125\,\mathrm{W}$ is assumed. The target values are a maximum junction temperature $T_j \leq 100\,^{\circ}\mathrm{C}$ with a maximum pumping power $W_{pump} \leq 1.25\,\mathrm{W}$. The coolant has a maximum inlet temperature of $T_{in} \leq 40\,^{\circ}\mathrm{C}$. With these data, the target thermal resistance can be calculated: $R_{th} = \Delta T/\dot{Q} \leq 0.48\,\mathrm{K/W}$. Table I summarizes the requirements.

It is a challenge to find a liquid meeting these requirements with both good thermal properties and electrical insulation. The thermal properties of three possible candidates are listed in Table II, together with those of water and water/glycol mixture as a reference (these are standard coolants as they offer high thermal performance, but are electrically conductive). The electrical properties of theses coolants are shown in table III. Because of its acceptable thermal properties, high boiling temperature and low GWP value, "Novec 7500" (3M) is selected for this work.

TABLE I: Electrical and thermal requirements

- Electrical properties
  - Electrical resistivity: $9.0{\times}10^5\,\Omega\mathrm{m}$
  - Relative Permittivity: matching that of AlN $\epsilon \approx 8-9$)
- Thermophysical properties
  - Operating junction temperature T_o: −55 °C to 175 °C
  - Generated heat: $\dot{Q} = 125\,\mathrm{W}$
  - Die size: $9.1\,\mathrm{mm} \times 9.1\,\mathrm{mm}$
  - Thermal resistance junction to case: $R_{th} < 0.48\,\mathrm{K/W}$
  - Target junction temperature: $T_j \leq 100\,^{\circ}\mathrm{C}$
  - Maximum fluid inlet temperature: $T_{in} = 40\,^{\circ}\mathrm{C}$
- Pumping capacity
  - Pumping capacity per die: $W_{pump} \leq 1.25\,\mathrm{W}$ (1 % of dissipated power, arbitrary)
- Environmental requirements
  - Global Warming Potential: $GWP \leq 200$, Non-toxic, Non-flammable

TABLE II: Thermal properties of some dielectric coolants compared with Water and water/glycol mixture

Fluid	Sp. heat $c_p[\mathrm{W/(kgK)}]$	Viscosity $\nu[\mathrm{m^2kg}]$	conductivity $\lambda[\mathrm{W/(mK)}]$	Boiling $T_b[^{\circ}\mathrm{C}]$
Novec 7300	1166	0.92	0.0625	98
Novec 7500	1151	0.98	0.0625	128
Trafosynth 2	2000	13.5	0.13	249
Water/Glycol	3424	0.11	0.404	110
Water	4135	0.65	0.63	100

TABLE III: Electrical properties of some dielectric coolants

Fluid	Permittivity $\epsilon[-]$	Diel. Strength $[kV]$	Resistivity $[M\Omega m]$	GWP $[-]$
Novec 7300	6.1	26.7	10^3	210
Novec 7500	5.8	35	2.2	100
Trafosynth 2	3.7	60	230	< 1

TABLE IV: Geometry parameters of the pin-fin structures

Design parameter	Interval
Diameter d in mm	$1 \geq d \leq 2$
Length h in mm	$2 \geq h \leq 6$
Diameter d_{jet} in mm	$5 \geq d_{jet} \leq 8$
AlN thickness t in mm	$1 \geq t \leq 5$
Volumetric flow $\dot{V}$ in l/min	$1 \geq \dot{V} \leq 5$

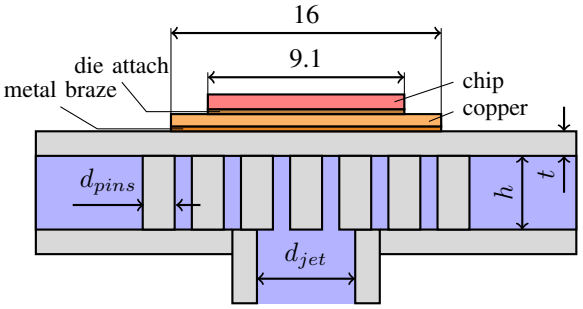
B. Cooler design

Considering the low pumping power requirements and the technical possibilities and limitations related to the manufacturing of a ceramic heatsink, two cooling concepts are investigated: jet impingement and channel flow. The first is depicted in Fig. 2, with an inlet located at the bottom of the heatsink, under the chip, causing the liquid to impinge on the top internal surface of the heatsink. Both left and right sides of the heatsink remain open and serve as outlets. The second concept (channel flow) has a similar internal structure, with the inlet located on one side and the outlet at the other.

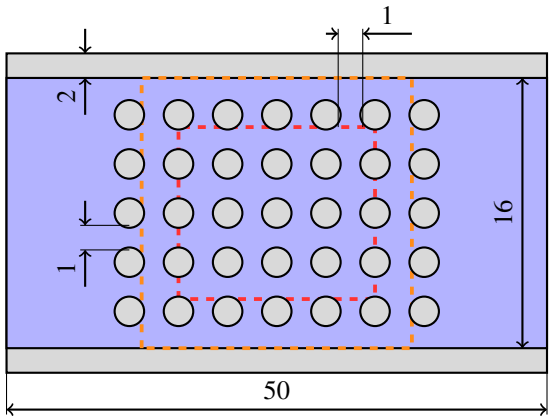
In order to increase the heat transfer area and generate turbulence in the system, pin-fins are needed in the cooling channel. Circular pin-fin structures are selected because they are easier to manufacture. The geometry parameters, which are used in the CFD simulation, are shown in Tab. IV (the parameter names refer to Fig. 2). The pin spacing is considered constant, at 1 mm. The material properties of each material used in the structure from Fig. 2 are presented in table V.

TABLE V: Materials properties

Material	Specific heat c_p[W/(kgK)]	Thermal cond. λ[W/(mK)]	Density ρ[kg/(m^3)]	Thickness b[µm]
Chip (4H-SiC)	700	370	2330	500
Die Attach (Ag)	230	100	2100	50
Cu	375	394	8960	300
Metal braze (AgCuTi10)	304	361	9490	10
AlN	710	170	3260	1500



(a) CAD parameter of the jet impingement cooling concept



(b) Cross section in middle of the channel (bottom view)

Fig. 2: Structure considered for the design, showing the design parameters

III. CFD Optimization

A. CFD model

Ansys CFD is used for the simulations presented here, and Fig. 3 summarizes the work-flow of the CFD simulations, which are run automatically. The model geometry from Fig. 2 is generated, considering a parameter set within the ranges listed in Tab. IV. The model is then meshed using Ansys automatic meshing algorithm, which generates an unstructured grid. The parameters of the mesh (mesh size, number and size of layers) are set in advance by the user. Then, the defined boundary conditions and solver-setup are defined (number of iterations, residual target, material properties, turbulence model). A constant power loss of 125 W is specified on the chip as a boundary condition. The other boundary conditions are a constant volumetric flow at the inlet and zero-pressure at the outlet. For all interface regions, a conservative flow boundary condition is applied. The walls are defined as adiabatic, i.e. no heat is released into the environment through them.

Once the model has been prepared, the ANSYS CFD solver is run. When the calculations are complete, an output file is generated with all the required outputs (T_j, R_{th}, W_{pump}). A new model is then automatically generated using another parameter set, and the process is repeated until all ranges from Tab. IV have been explored.

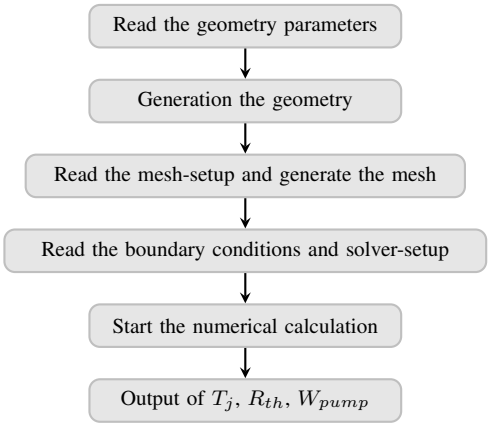


Fig. 3: Procedure for the CFD simulation

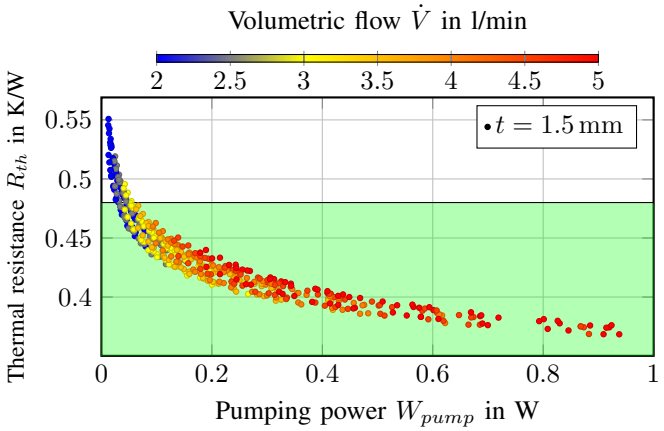


Fig. 4: Thermal resistance as a function of pumping power for all configurations considered (CFD simulations, for Novec 7500).

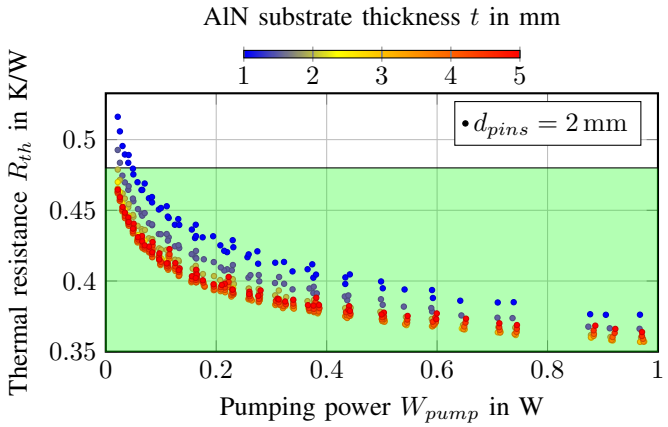
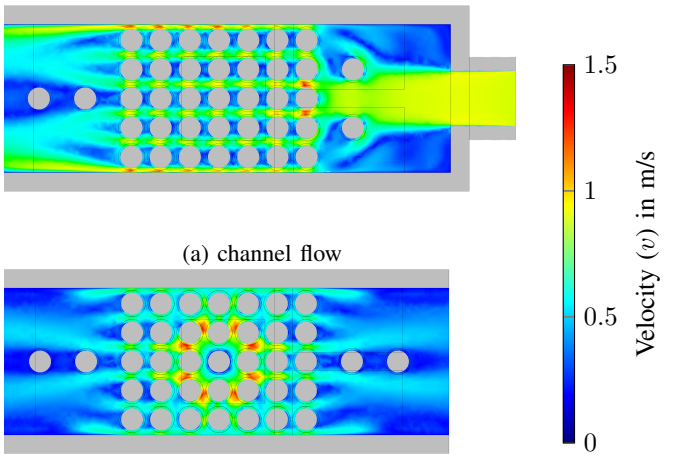


Fig. 5: Thermal resistance as a function of pumping power, for different values of AlN thickness t (CFD simulations, for Novec 7500).



(a) channel flow

(b) jet impingement

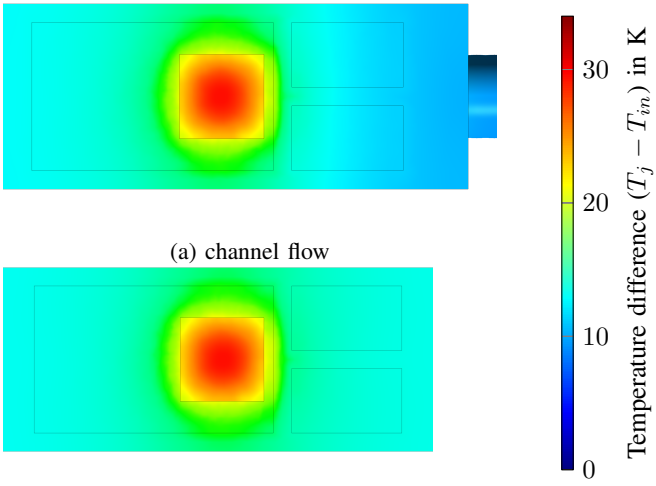
Fig. 6: Velocity distribution at the middle of the channel for both cooling concepts at 2 l/min

B. CFD results

The thermal resistance of the various configurations investigated is plotted in Fig. 4 as a function of pumping power. The green area in the figure is the target area ($R_{th} \leq 4.8\,\mathrm{K/W}$ & $W_p \leq 1.25\,\mathrm{W}$). Every point in the figure presents a simulation with different parameters from Tab. IV and constant AlN thickness ($t = 1.5\,\mathrm{mm}$). As can be expected, increasing pumping power results in a higher flow rate and better cooling. The dataset exhibit a clear Pareto-optimal front.

An other parameter of influence is the AlN ceramic thickness t. Fig. 5 shows the thermal resistance dependencies on the ceramic thickness. These simulations were done with one pin diameter ($d_{pins} = 2\,\mathrm{mm}$) to reduce the number of simulations. The thermal resistance decreases as AlN thickness increases, due to the heat spreading effect offered by the ceramic. However, a very thick ceramic (thicker than 3 mm) yields no further improvement (and can even result in a small degradation) in thermal resistance. Therefore, for the experiments, two thicknesses are investigated: 1.5 mm (to explore thin designs) and 3 mm (thermal optimum with our design and cooling fluid). The other parameters selected as a result for this optimization process are $t = 1.5/3\,\mathrm{mm}$, $d_{jet} = 7.5\,\mathrm{mm}$, $d_{pins} = 2\,\mathrm{mm}$, $h = 6\,\mathrm{mm}$.

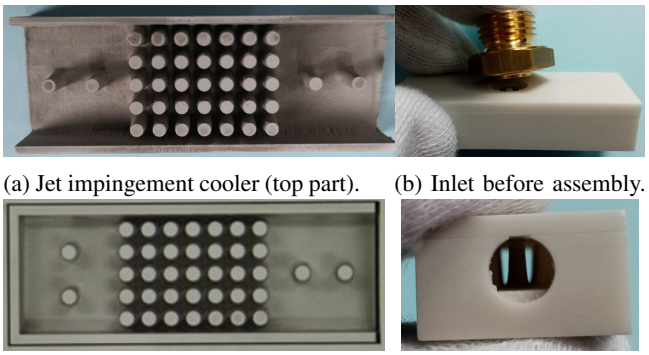
Velocity distribution maps are presented for these designs in Fig. 6. In the case of jet impingement, the coolant hits the surface under the chip vertically, causing higher velocity there and more turbulence, which improves the heat transfer coefficient. Furthermore, the shorter path of the fluid from the inlet to the outlet as well as the splitting of the flow rate (as there are two outlets) causes a dramatic decrease in the pressure drop ($\Delta p \sim \dot{V}^2$) when compared with the channel flow configuration. As a consequence, pumping power is expected to be significantly lower for the jet impingement configuration at a given flow-rate. A comparison between the temperature distributions for both coolers is shown in Fig. 7 for a flow-rate of $2\,\mathrm{L\,min^{-1}}$. However, because of the lower pressure drop caused in the jet cooler, the pumping power it



(a) channel flow

(b) jet impingement

Fig. 7: Temperature distribution in the system for channel flow and jet impingement cooling concept at 2 l/min flow rate



(a) Jet impingement cooler (top part). (b) Inlet before assembly.

(c) Channel flow cooler (top part). (d) Inlet without fitting.

Fig. 8: Heat sinks and cooler fabrication

requires is much lower than that of the channel flow cooler.

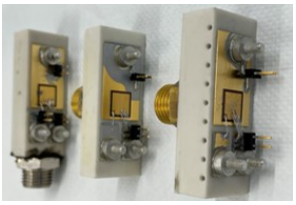
IV. Experimental study

A. Preparation of the test vehicles and test setup

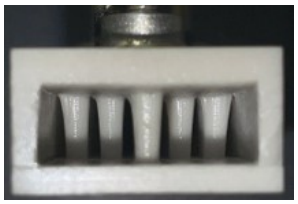
Three test vehicles are produced for experimental tests (one channel flow cooler, and two impingement coolers with different ceramic thicknesses).

Metallised ceramic (AlN) coolers are fabricated by CeramTec. Two ceramic parts (a flat bottom and a top part – Figs 8a and c – which is structured to form pins) are joined together to form a single unit cooler. Copper metallizations (for the chip interconnects) and a brass fitting (forming the inlet) are then attached to the ceramic cooler. A $9.1 \times 9.1\,\mathrm{mm}^2$ IGBTs is then sintered on the largest metal pad and wire-bonded with thick Al wedge bonds. Finally, connectors are soldered on the metal pads for the electrical connection to the outside world. Fig. 9 shows the populated test vehicles.

The test vehicles are then connected to a test setup comprising a fluid loop and a thermal analyzer (Phase 12B, Analysis Tech) for the measurement of R_{th}. A photograph is given in

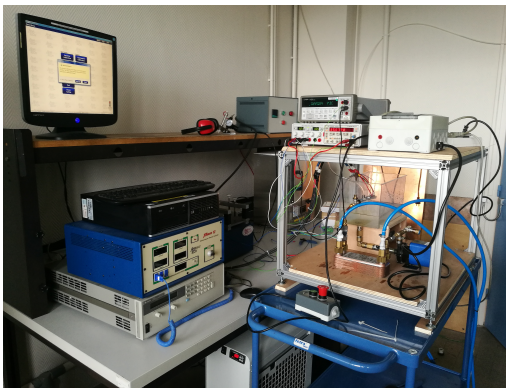


(a) The three prototypes.

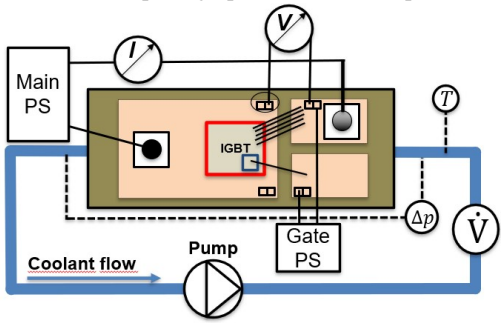


(b) Side view showing the pins.

Fig. 9: The three prototypes: channel flow, jet impingement with two AlN thicknesses (1.5 mm and 3 mm);



(a) A photograph of the test setup



(b) schematic of the test setup

Fig. 10: Test setup

Fig. 10a and the schematic in Fig. 10b (the connections of the thermal analyzer are not detailed here). A special care is given to the design of the cooling loop to avoid elastomeric materials which may react with Novec 7500 (copper piping, compression fittings, magnetic coupled pump…)

B. Test results

A comparison between measured and simulated thermal resistances as a function of pumping power is shown in Fig 11. It can be seen that the jet impingement cooler has better cooling performance as it exhibits lower thermal resistance and pumping power. Although the 1.5 mm and 3 mm jet coolers have comparable pressure drop/flow-rate characteristics (not shown here), the thermal resistance is lower for the 3 mm test vehicle because of the better heat spreading it offers, resulting in a larger solid-liquid exchange surface.

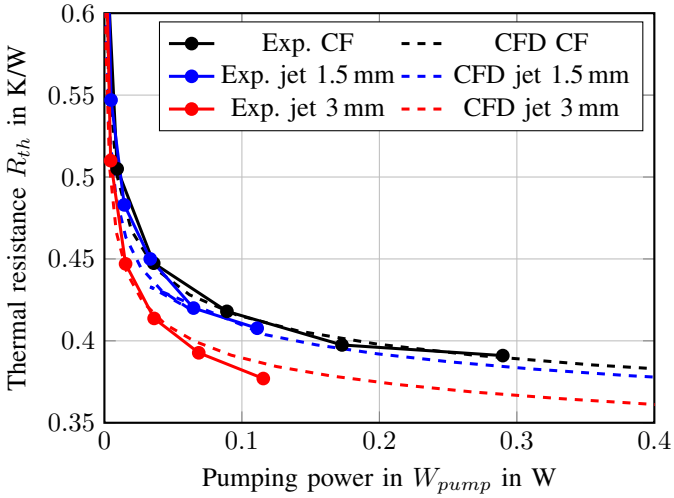


Fig. 11: Temperature distribution in the AlN. "Exp.": experimental result; "CFD": simulation result; "CF": Channel flow configuration.

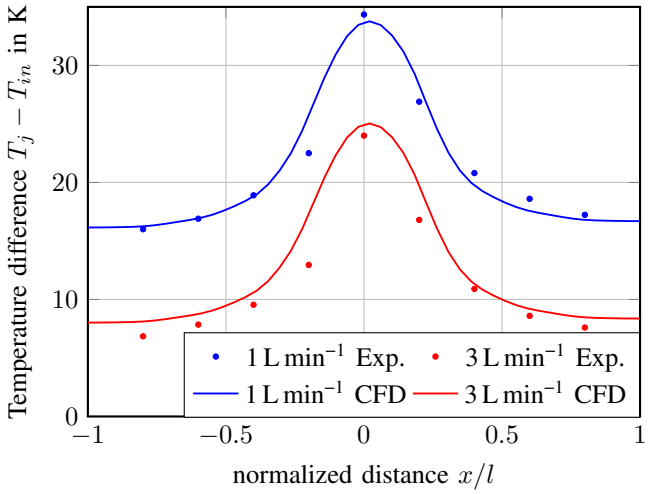


Fig. 12: Temperature distribution in the AlN for the jet cooler ($t = 3mm$) experimentally ("Exp.") and numerically ("CFD")

A second comparison between measurement and simulation results is presented in Fig. 12. Thermocouples are inserted in the ceramic (mounting holes are visible in the rightmost cooler in Fig. 9a) and the measured temperatures are compared to simulation predictions, showing a very good agreement.

V. Conclusion and Outlook

In this work, an integrated cooling system, compatible with the requirements of high voltage power electronics is introduced. A single-chip cooling structure is optimized using CFD simulation, and three prototypes are built. Simulation and experimental results are in good agreement, and show that the demanding requirements ($\Delta T \leq 60\,°\mathrm{C}$ for a 125 W power dissipation over a $9.1 \times 9.1\,\mathrm{mm}^2$ chip area) can be met. Because of its lower pressure drop and higher fluid velocity, the jet impingement structure is found to be more efficient than the channel flow structure. Furthermore, a thick ceramic layer (up to 3 mm) is found to be beneficial because of the increased heat spreading effect it offers.

Acknowledgment

The work presented in this paper has been undertaken as part of the research project "ARCHIVE", funded by the Bundesministerium für Bildung und Forschung (BMBF) and the Agence Nationale de la Recherche (ANR).

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