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A Novel Power Delivery Method for Asynchronous Loads in Energy Harvesting Systems

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Abstract

DC/DC conversion has been an integral part of the power delivery chain in energy harvesting systems because the conventionally targeted synchronous computation load demands stable Vdd, which cannot in general be supplied by power harvesters directly. However, asynchronous computation loads, in addition to their potential power-saving capabilities, can be made tolerant to a much wider range of Vdd variance. This may open up opportunities for much more energy efficient methods of power delivery to be adopted. This paper presents in-depth investigations into the behavior and performance of different power delivery methods driving both asynchronous and synchronous load for the first time. A novel power delivery method, which employs a capacitor bank for adaptively storing the energy from power harvesters depending on load and source conditions, is developed. Its advantages, especially when driving asynchronous loads, are demonstrated through comprehensive comparative analyses.

Keywords-Switched Capacitor DC/DC converter; Capacitor Bank; Energy Harvesting; Piezoelectric Element.

I. Introduction

Energy harvesting (EH) is becoming a more popular method of generating energy for computation systems, especially in the case of remote and mobile systems [1]. Diverse energy conversion methods are being investigated for generating electric energy in EH devices, including for instance solar cells, thermogenerators, and piezoelectric generators [2]. EH are fundamentally different from conventional power supply methods in a number of ways. For instance, in EH systems the available energy can be viewed as infinite, with newer energy always available during the lifetime of the system, but instantaneous power is often unpredictable and nondeterministic, depending on the environment. This has motivated various techniques in trying to smooth the power flow, including temporarily storing harvested energy in components such as rechargeable batteries and off-chip supercapacitors

[3], which have a number of disadvantages [4]. Therefore, directly delivering energy generated by harvesters to the computational load might be an alternative in some applications [5]. In this work, we focus on the case where power from the EH device is directly delivered to the load on-chip without intermediate off-chip storage, targeting extreme miniaturization for future applications.

The output voltage of EH devices (e.g. piezoelectric transducers [6]) typically depend on the designs of the devices and the conditions of the environment from which energy is harvested. It usually does not coincide with the correct Vdd level for the load electronics. DC/DC converters are normally needed to convert the voltage from EH devices to suitable Vdd levels for the load electronics. For extreme miniaturization, the DC/DC unit should be constructed onto the same chip as the computational load, which makes many existing DC/DC designs unsuitable. For this purpose the best existing DC/DC solution is the switched capacitor DC/DC converter (SCC) which may have high conversion efficiency and can be fabricated on chip [7].

For synchronous computational loads, relatively stable power supplies are needed with minimum (5% to 10%) voltage variation allowed [8]. DC/DC converters may pass on the instability in the EH voltage when off-chip intermediate storage is not used, potentially leading to the load system needing to be switched off or switched into sleep mode [9]. To increase power output stability, certain DC/DC converter designs can be dynamically switched among a number of different conversion rates at the expense of frequent mode switching. For example, variable power supply may cause frequent switching operations within SCCs [10].

Asynchronous computational loads in general can, on the other hand, tolerate wide voltage variations. This makes them good candidates for use in EH systems with direct power delivery, provided a proper Vdd range can be obtained. However, the overall performance of a combination of asynchronous loads and EH + DC/DC power delivery chain remains poorly

studied. Additionally, since typical DC/DC converter designs target synchronous loads, whether they are suitable for asynchronous loads is unknown. There may also exist other solutions to voltage conversion between EH devices and asynchronous loads.

A. Contributions and Organization

This paper concentrates on power delivery methods which deliver power from EH devices to computational loads. A new power delivery method, based on an on-chip capacitor bank block (CBB) is proposed. This method is mainly aimed at providing a degree of flexibility and programmability in the power delivery control so that power can be delivered to the load intelligently under different EH power source and load conditions for either performance or efficiency goals. This method is comparatively investigated with conventional SCCs. The comprehensive analyses across the two different types of power delivery and synchronous and asynchronous loads represent the first attempt to systematically study the issue of on-chip power delivery from EH devices to computational loads. The first demonstration of the validity of intelligent control of power delivery in EH systems is also carried out.

In Section II, the conventional SCC power delivery method is described, and the new CBB method is introduced and described. Sections III and section IV contain detailed descriptions of the environment and objectives of the comprehensive comparative studies, which are described in the following sections. Sections V and VI concentrate on the energy consumption characteristics of the two power delivery methods coupled with different types of loads. Section VII concludes this paper with discussions.

II.   Different Power Delivery Methods

This section describes the two different types of power delivery systems studied in this paper. They are the conventional switched capacitor DC/DC converter (SCC) and the capacitor bank block (CBB) proposed in this section.

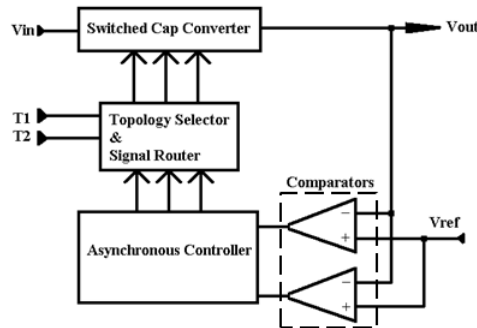## A. Switched Capacitor DC/DC Converter

Figure 1. Switched Capacitor DC/DC Converter [11]

Figure 1 shows the SCC architecture, which consists of a switched capacitor converter, a topology selector & signal router block, an asynchronous controller, and a comparator block [11]. The SCC block is designed to implement 4 different conversion ratios (1/3, 1/2, 2/3 and 1/1). The topology selector & signal router block is employed to generate conversion codes and to make sure that the codes do not cross-overlap. This block is controlled by the asynchronous controller, and contains four conversion code generators, which correspond to the four different conversion ratios. The inputs T_1 and T_2 are conversion ratio select pins, which can enable one of the four conversion ratios. The asynchronous controller manages converting operations by referencing two threshold voltages generated by the comparator block. It is implemented with pure digital asynchronous circuit design to reduce energy consumption. The comparator block, based on current mirror principle to reduce circuit complexity, compares the feedback signal from the SCC output with the signal from the input V_{ref}, which is used as a reference. As long as there is adequate power supplied from V_{in}, the SCC can maintain the required voltage at the output V_{out} from 1.1V down to 0.38V [11].

In Figure 2(A), the structure of the SCC block is shown. The converter consists of a direct switch and two conversion blocks. The direct switch is controlled by the signal S_0 and the two conversion blocks are controlled by the signal S_1 and S_2 respectively. For each

conversion block, a switch connects the input of the conversion block to the power supply and another connects its output to the load. At the output, a capacitor C_{out} is used as the energy storage device receiving the energy delivered from the converter. C_{out} can provide energy to the load as long as the voltage at C_{out} meets the working Vdd of the system. Figure 2(B) describes the conversion block structure. The three capacitors C1~C3 have the same capacitance. K_0 and K_1 are the signals used to control the input and output of the conversion block respectively. The other signals in (B) are generated by the topology selector to implement different conversion ratios. And the whole conversion block structure uses 10 transistors to achieve a simple circuit design.
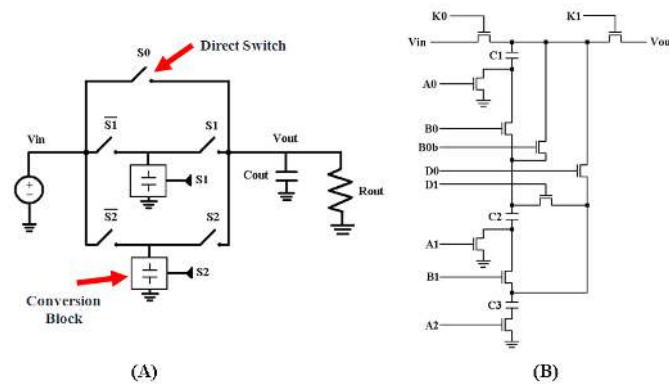

Figure 2. Switched Cap Converter Structure (A) [11] and Conversion Block Structure (B)

Figure 3 shows the working principle of the SCC. The comparator block generates two threshold voltages V_{th1} and V_{th2}. The signals S_0, S_1, and S_2 are generated by the asynchronous controller. In (A), when the system enables the SCC, the direct switch is switched on by the signal S_0. The power supply directly charges C_{out} until the voltage of C_{out} reaches V_{th1}, which corresponds with the working Vdd for the load. In the meantime, both conversion blocks are also connected to the power supply and accumulate energy for converting operations later. In this case, S_0 is set to HIGH. Both S_1 and S_2 are kept to LOW. Once the voltage at C_{out} is beyond V_{th1}, the direct switch is turned off. Due to system latency, an overshot is inevitable after switching off the direct switch. Since the load has strong voltage pull-down ability to the

output of the SCC (V_{out}), V_{out} will fall below V_{th1} shortly. When V_{out} goes across V_{th1}, the controller switches off the power supply of one of the fully charged conversion blocks and connects its output to the load to supply power. In the meantime, the voltage conversion is performed in the block. Since power switching is performed, V_{out} can be driven above V_{th1} again. Because the proper conversion ratio is set according to the working Vdd range of the load, the overshot is assumed to be within the acceptable range. These two conversion blocks take turns to provide energy when V_{out} falls below V_{th1}. If the power supply is inadequate or the power consumption of the load increases, V_{out} may further fall down to V_{th2}, as shown in (B). Once V_{out} reaches V_{th2}, the controller sets S_0 to HIGH and switches on the direct switch immediately to raise V_{out} to V_{th1} rapidly. At the same time, both conversion blocks are connected to the power supply again. If V_{out} cannot be raised to V_{th1}, the system will stay in the charging state until the SCC can accumulate enough energy to start converting operations.
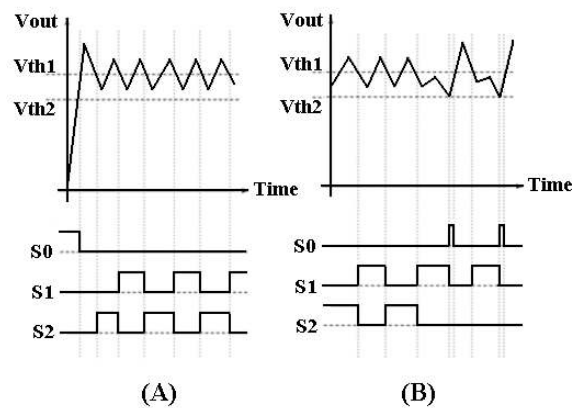

Figure 3. The Switched Capacitor DC/DC Converter Working Principle [11]

B. Proposed Capacitor Bank Block

The proposed CBB power delivery unit contains three main parts: a CBB, a voltage sensor block, and a switching controller, shown in Figure 4. In the CBB, capacitors are used to store the energy separately. In the voltage sensor block, a voltage sensor [12] is used to sense the voltage status in the capacitors. It also contains a selector, which is controlled by the switching

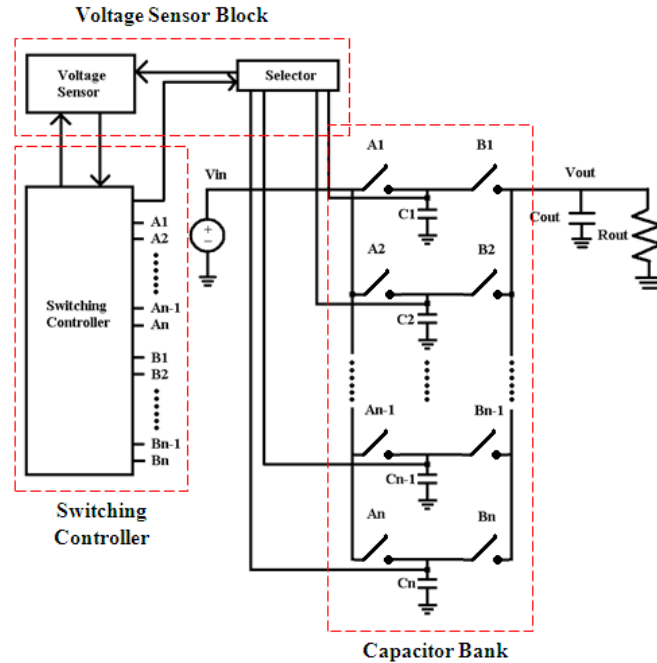controller. The switching controller also controls the switches in the CBB.

Figure 4. Proposed Capacitor Bank Block

The switching controller not only controls the charging and discharging of the capacitors cyclically one after another, but can also choose one of the capacitors to be charged or discharged according to task queue or performance requirements from the load [13]. In this case, the values of the capacitors do not have to be the same. Different sized capacitors in the structure may help increase the efficiency and flexibility of the system. However, for simplicity and ease of comparison, all capacitors are assumed to be the same in the studies in this paper.

Such a CBB power delivery unit distributes the energy from the EH device into multiple capacitors and, with a programmable controller, can be made intelligently controllable to provide load- and source-responsive power delivery with information from the load and EH device to achieve many performance and energy requirements. For instance, as demonstrated in the following sections, overcharging individual capacitors can be avoided, load speed can

be raised or lowered on demand, load initial latency may be reduced, and overall energy efficiency may be maximized. In general, it is targeted at more intelligent power delivery rather than maintaining pre-set Vdd levels.

III. System Design

This section describes the environment in which the SCC and CBB methods will be comprehensively compared in the following sections. This includes models for the power source and computation load, as well as the detailed designs of the SCC and CBB power delivery units.

A. *Piezoelectric Energy Harvesting Circuit Model*

In this paper we use a simple model of a piezoelectric element to represent the EH power source [14]. Shown in Figure 5 (A), this model consists of a sinusoidal AC source and a 4-diode based rectifier. The model is constructed for the Matlab Simulink and Simscape Electrical Elements environment, in which the waveforms shown in Figure 5 (B) are produced. Here $I_P(t)$ is the AC generated by the piezoelectric element. $V_P(t)$ is the voltage at C_P and $i_O(t)$ is the variable DC (with obvious gaps between pulses) flowing through the load.

Current-technology piezoelectric transducers can achieve wide working frequency ranges. For instance, air-coupled ultrasonic piezoelectric transducers have the frequency range 0.3-2.5 MHz [15] and special piezoelectric crystals 1-200 MHz [16]. The 1 MHz working frequency assumption is in line with these technologies. Years ago, a low-power wireless sensor system used approximately 700 uW of power. Recently, the average power of most wireless sensor systems has fallen below 100 uW and some applications are even targeted at a few microwatts or less [17]. Therefore, for the power supply with constant 1.2 V, the variable DC with peak values 10 uA, 100 uA, and 1 mA are considered as sparse case, moderate case, and adequate case respectively. For the simulation in Matlab, the variable DC

supply data with three different peak values of 10 uA, 100 uA, and 1 mA are recorded in
Workspace. The frequency is 1MHz and the period of each variable DC EH pulse is 1 us.
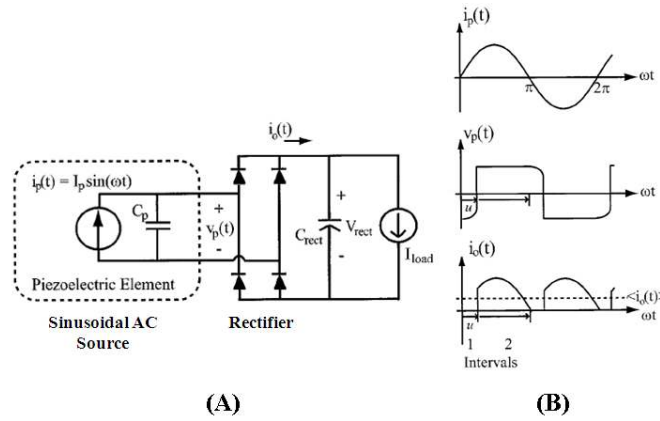

Figure 5. Piezoelectric energy Harvesting Circuit Model [14]

B. System for Comparative Studies

The structure of the entire system (Figure 6) consists of a piezoelectric EH circuit as the
power supply, a power delivery block and a load. Two types of power delivery blocks, one
based on SCC and other on CBB, will be studied. A self-timed counter from [18] is used as
the load, because this counter has a good linear proportional relationship between its
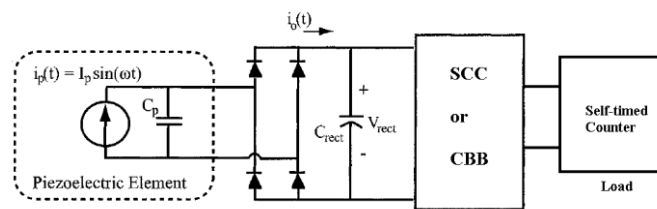computational effort and its numerical count output.

Figure 6. System architecture.

Figure 7 shows the structures of the different power delivery blocks. These structures are
implemented in UMC90nm process technology in Cadence tools. The Ipwlf current source

(Independent Piece-Wise Linear Current Source Based on File) represents the output from the model of the piezoelectric energy harvesting circuit (Figure 5(A)) converted directly to Cadence environment from Matlab results. In the studies, the Vdd of the power delivery block is set to 1 V according to the UMC 90nm-technology library specifications. All capacitors are from Cadence AnalogLib.
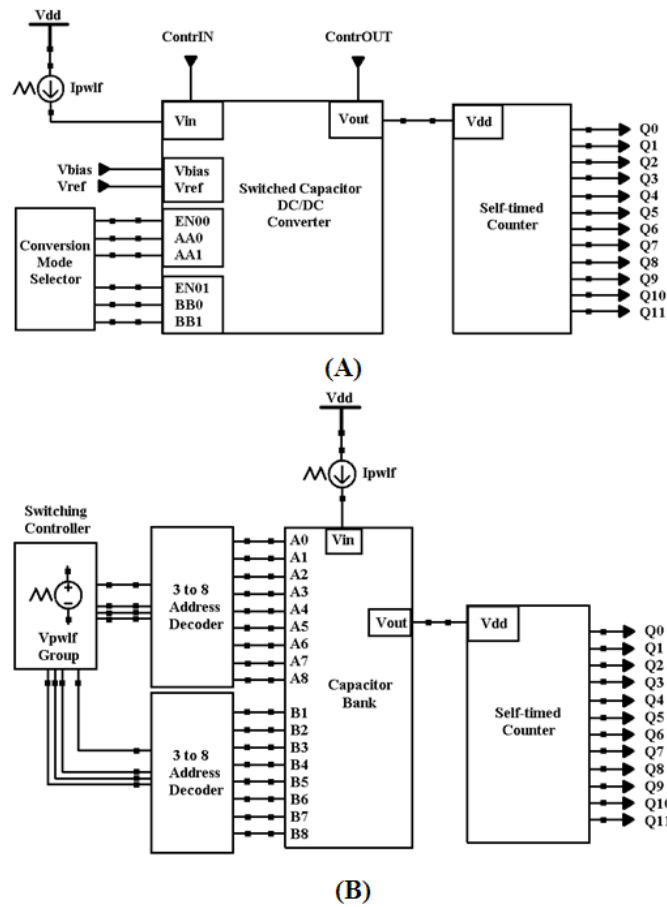

Figure 7. Testing System with Switched Capacitor DC/DC Converter & Capacitor Bank Block respectively

In (A), the SCC power delivery block, a conversion mode selector sets the conversion ratio of the system. In these studies, the SCC is supposed to provide 1 V Vdd to the load, which translates to a 1/1 conversion ratio. By adjusting the inputs V_{bias} and V_{ref}, the output of

the SCC can be calibrated to 1 V. The input pins ContrIN and ContrOUT are introduced to control the input and output of the SCC. In the conversion block, the three capacitors are employed 2pf each (see Figure 2(B)). And the value of C_{out} in both SCC and CBB (see Figure 2(A) and Figure 4) is 10pf.

In (B), the CBB power delivery block, a Vpwlf voltage source (independent Piece-Wise Linear Voltage Source Based on File) block is used. This block consists of 8 Vpwlf voltage sources and has 8 outputs for Charging Enable (1 bit), Discharging Enable (1 bit), and charging & discharging address decoding (6 bits). Two 3-to-8 line address decoders with address latches are used together with the Vpwlf voltage source block. In the capacitor bank, there are 8 10pf capacitors (Figure 4). Both the CBB and SCC are fully self-timed devices.

IV.   Assumptions

The following assumptions are made for the explorative studies in this paper.

A. *Asynchronous Load with SCC*

Asynchronous systems in UMC90nm process technology in general work with Vdd varying from 0.5 V to 1.1 V. Although the self-timed counter used here as load works over a much wider Vdd range, we try to represent a greater class of asynchronous loads by limiting the range and switching the load off when Vdd goes above 1.1 V or below 0.5 V.

B. *Synchronous Load with SCC*

For comparison fairness, we use the same self-timed counter as load in the synchronous load studies. Synchronous systems are usually assumed to be able to tolerate 10% of voltage variation. Therefore, in the studies of synchronous loads, once the load Vdd goes above 1.1 V

or below 0.9 V, the controller of the system switches the power supply off the load. The SCC output is required to be charged up to 1 V before starting to deliver power to the load.

C. Asynchronous Load with CBB

In the CBB, each capacitor is required to be charged to 1 V then discharged onto the load down to 0.5 V, unless otherwise stated. Discharging from 1 V to 0.5 V, the capacitor distributes 75% of the total energy to the load (see Equation 1).

$$E = \frac{1}{2}CV^2 \tag{1}$$

The charging and discharging processes are according to first fully charged first discharging rule. When one capacitor is discharged, the others can be charged. When all capacitor are fully charged to 1 V, the controller will switch off the charging selector. When all capacitors are discharged below 0.5 V and there is no power supply coming, the controller will switch off the discharging selector and load.

V.   System Performance Results

In these studies, for each system composition, three groups of experiments are performed with power supplies in the three different strengths, corresponding to peak values of 100 uA, 10 uA and 1 mA from the EH power source. In each experiment group, the EH current supply profiles are the same (see $i_o(t)$ waveform in Figure 5) and the frequency is 1 MHz.

The resulting output waveforms of SCC and CBB are supplied as Vdd to the load. Other waveforms are also recorded, e.g. S_0, S_1 and S_2 indicate the behaviour of the SCC, voltages of Cap1 to Cap8, and Q_0 to Q_{11} are the output of the self-timed counter serving as load. In each experiment, the numbers counted by the counter and the numbers of switching are recorded. Energy consumption and energy delivery efficiency data are derived from the experiments.

Since in each group, the energy supplied by the EH is the same over the same time period, energy delivery efficiency as seen from the load can be derived from the number of switching in the load in a given time period. The self-timed counter load has the characteristic that it counts when it has sufficient power and each count can be treated as the basic quantity of computation in these experiments. The ultimate metric here is thus how many counts the load can do given some amount of energy from the EH power supply.

A. Systems working with Moderate Power Supply

- Computation Performances and Switching Times

In this group, the EH supply peak value is set to 100 uA. Figure 8 shows that, within 2 us, the number counted by the asynchronous load with SCC in (B) is the largest. Within the first period, it gets 783 counts. And it achieves 1053 counts at the end of the second period. The synchronous load with SCC in (A) gets smallest counts within two periods, 499 for the first period and 719 for the second period. The asynchronous system with CBB ranks in the middle, shown in (C).

In the case where the EH stops after 2us, the power delivered from SCC falls rapidly. The SCC will stop working when its output voltage is below 0.9 V. And the synchronous load needs to be switched off anyway. However, the asynchronous load with SCC can still continue computation in a very short time from the small amount of energy stored at C_{out} (see Figure 2(A)). The asynchronous load works until the voltage at C_{out} is below 0.5 V. On the other hand, the asynchronous load with CBB can achieve a large amount of computation after the EH stops at 2us. The energy generated by the harvester has been stored in 6 capacitors separately within 2 us and the capacitors can provide power to the load one after another. At 2 us, Cap1, Cap2 and Cap3 are still fully charged and Cap6 is charged to 0.67 V when the EH supply stops, shown in (C). In this case, CBB allows the asynchronous load to continue working for another 1.4 us and the system stops working only when all capacitors are discharged below 0.5 V. And the asynchronous load with CBB gets 1056 counts after 2us.
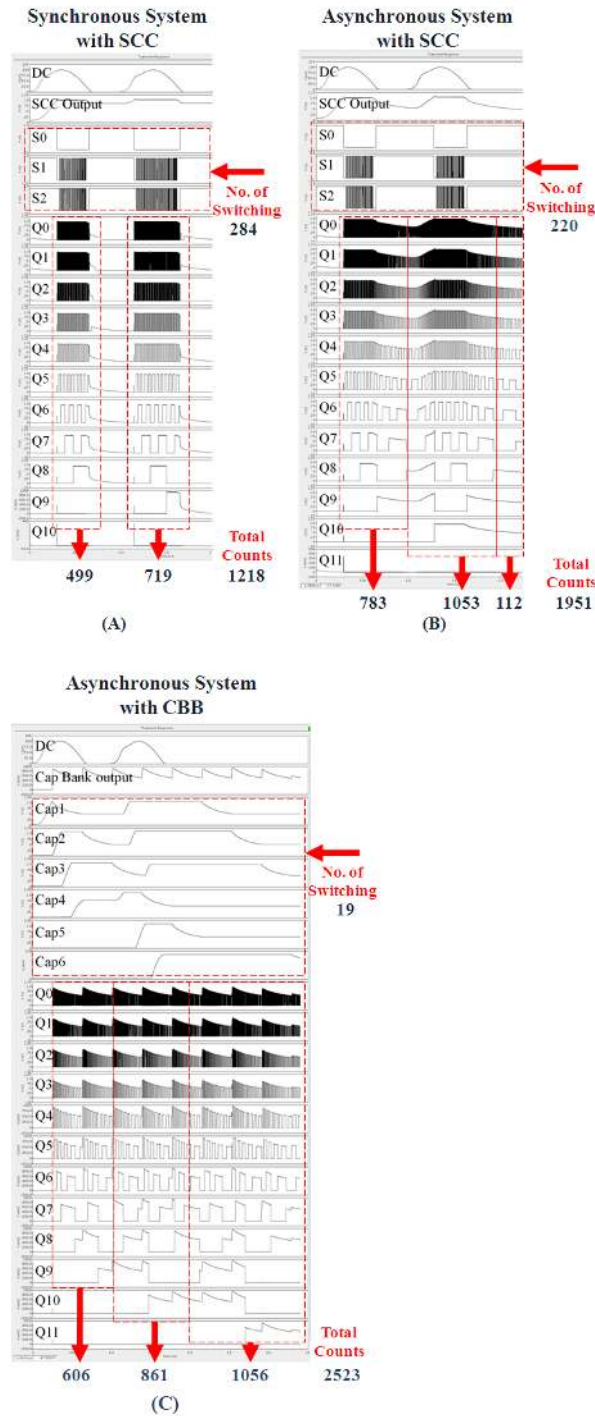
Figure 8. The Counter performances in Terms of Synchronous system with SCC (A), Asynchronous System with SCC (B) and Asynchronous System with CBB (C).

In terms of total numbers of counts, the asynchronous load with CBB achieves the largest amount of computation (2523), which is approximately 29% more than that of asynchronous load with SCC (1951) and 207% more than that of synchronous load with SCC (1218). The numbers of switching within the power delivery unit are also indicative of the efficiency of the power delivery method, as switchings in the power delivery unit itself expends energy which becomes unavailable for the load. The internal numbers of switching is 19 for CBB with asynchronous load, 284 for SCC with synchronous load and 220 for SCC with asynchronous load.

- Energy Consumption of Switching and Control

Table 1 shows the energy consumption data. The synchronous load with SCC has longer working time than the asynchronous load with SCC in the second period (shown in Figure 8 (A) and (B)). The former therefore consumes more energy. Since the asynchronous load with CBB only has 19 internal switchings in the whole process, it consumes a significantly smaller amount of energy. However, in terms of energy consumption per switching, although the SCC has two more complicated conversion blocks, the energy per switching of SCC is lower than that of the CBB. In terms of control energy consumption, because the asynchronous load with CBB employs the Vpwlf source group and two 3-to-8 line address decoders as the control method (shown in Figure 7 (B)), the energy consumption for the control operation is smallest in the comparison. Since SCC employs a topology selector & signal router block, an asynchronous controller and a comparator block (see Figure 1), the control block is more complex than that of the CBB. Therefore, the control energy consumed by the systems using SCC is significantly higher than that of the asynchronous load with CBB. Additionally, the asynchronous load with SCC consumes less energy than synchronous load with SCC in control operation.

Table 1. Energy Consumed for Switching and Control

	Synch System with SCC	Asynch System with SCC	Asynch System with CBB
Energy Consumed for Switching (pJ)	156	133	15
Switching Times	284	220	19
Energy Consumed per Switching (pJ)	0.55	0.6	0.79
Energy Consumed for Control (pJ)	307	229	34

- Energy Delivery Efficiency

Energy delivery efficiency data is shown in Table 2. The total counts performed by the loads with different delivery methods are also shown. The load energy consumption of the asynchronous load with CBB is the largest because the system achieves largest amount of total counts. Since the synchronous load with SCC gets the smallest amount of counts in total, the counter in the system consumes the smallest amount of energy. The total energy from the piezoelectric EH circuit model within 2us is the same for all systems.

Table 2. Energy Delivery Efficiency of Different Systems

	Synch System with SCC	Asynch System with SCC	Asynch System with CBB
Total Counts	1218	1951	2523
Self-timed Counter (pJ)	28.2	34.4	36.3
Harvested Energy (pJ)	73.9	73.9	73.9
Energy Delivery Efficiency	38.2%	46.5%	49.1%

Power delivery efficiency is normally calculated with the method [19] in Equation 2, which compares the power delivered by the converter with the power delivered to the converter. This may not be useful for variable power supply systems. The power supply from the piezoelectric EH circuit is highly time-variant. As a result the "efficiency" calculated from Equation 2 can vary over a wide range. Power delivery units with storage such as SCC

and CBB can deliver an output even with input at 0. In such cases the "efficiency" would be
infinity which clearly does not provide a useful metric.

$$EFF_{DCDC} = \frac{(I_{OUT})(V_{OUT})}{(I_{IN})(V_{IN})}(100\%) \tag{2}$$

For such systems it is more meaningful to talk about energy delivery efficiency, shown in
Equation 3. And this is what's shown in Table 2. The order of energy delivery efficiency is
CBB at 49.1% leading SCC with asynchronous load at 46.5% and SCC with synchronous
load at 38.2%.

$$EFF_{DCDC}' = \frac{Energy_{WORKLOAD}}{Energy_{HARVESTED}}(100\%) \tag{3}$$

- Improving Computation for Asynchronous Load with CBB

The CBB method makes it possible to control the charging and discharging of individual
capacitors in the bank in an intelligent and flexible manner. CBB switching algorithms
exploiting this facility may be developed to improve the energy delivery performance over
the mechanical FIFO charging to full, discharging to 0.5 V rule. We explore this with a
simple experiment. In this experiment, Cap1 is only charged to 0.7 V rather than fully
charged to 1V before charging is moved to Cap2. This is to allow power delivery to the load
quickly instead of obligating waiting until Cap1 is fully charged. The results in Figure 9
clearly demonstrate the usefulness of this flexibility. The "partial charging Cap1 to 0.7V"
algorithm saves 20 ns of load waiting time and ultimately delivers 80 more counts in 1 us. By
deploying the "partial charging Cap1 to 0.7 V" algorithm, (B) did 7 times CBB switching,
one more than (A) with 6 times. In this case, average voltage at the output of CBB in (B)
(from 0.22 us to 1 us) is 0.741 V, compared that in (A) (from 0.24 us to 1 us) 0.693 V. The
higher average voltage at the output of CBB leads to higher counting performance.
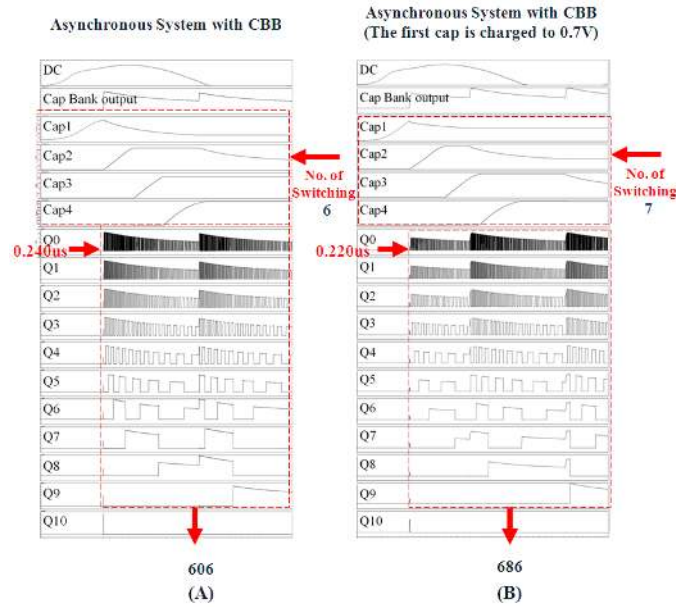
**Figure 9. The Counter Performance of Asynchronous System with CBB in Terms of Charging the Cap1
to 1 V (A) and charging the Cap1 to 0.7 V (B)**

- Energy Consumption of Switching and Control

Table 3 shows the energy consumed within 1 us for this experiment. In total load switching energy consumption, the system with the new charging method consumes 7.08 pJ, which is approximately 2.7% more than the system with normal charging method (6.89 pJ). In control energy consumption, the former consumes 11.3 pJ, which is 39% more than the latter (6.9 pJ).

Table 3. Energy Consumed for Switching and Control

	Asynch System with CBB	Asynch System with CBB (Computing Performance Improved)
Energy Consumed for Switching (pJ)	6.89	7.08
Switching Times	6	7
Energy Consumed per Switching (pJ)	1.15	1.01
Energy Consumed for Control (pJ)	6.9	11.3

- Energy Delivery Efficiency

Table 4 shows the energy delivery efficiency of the asynchronous load with CBB with different charging methods. Therefore, the energy delivery efficiency of the system using the new charging method (34.1%) is significantly higher than that of the system with the normal charging method (27%). The investigation is performed only to 1 us, with unspent energy in the capacitors at the end. The numbers are thus not comparable with those in Table 2.

Table 4. Energy Delivery Efficiency of Different Systems

	Asynch System with CBB	Asynch System with CBB (Computing Performance Improved)
Total Counts	606	686
Self-timed Counter (pJ)	10	12.6
Harvested Energy (pJ)	37	37
Energy Delivery Efficiency	27%	34.1%

B. Systems working with Sparse Power Supply

- Computation Performances and Switching Times

In this section we study systems with peak EH current output of 10 uA. Figure 10 shows the computation performances of synchronous load with SCC and asynchronous load with CBB. Because of the very limited power input, both systems can only switch on the load for a very short period. The synchronous load with SCC starts counting when the fourth EH pulse comes (3.583us) and then stops because the Vdd of the load going below 0.9 V. This on/off process is repeated when the next EH pulse comes. In the asynchronous load with CBB, Cap1 is fully charged when the third EH pulse comes (2.413us). Then, the fully charged capacitor is discharged immediately. In the mean time, charging moves to Cap2 and it is charged to 0.83 V at the end of the fifth EH pulse.

In the case where after the fifth EH pulse there is no more power coming, the synchronous load with CBB counts to 573, which is approximately three times more than that of the synchronous load with SCC (198).
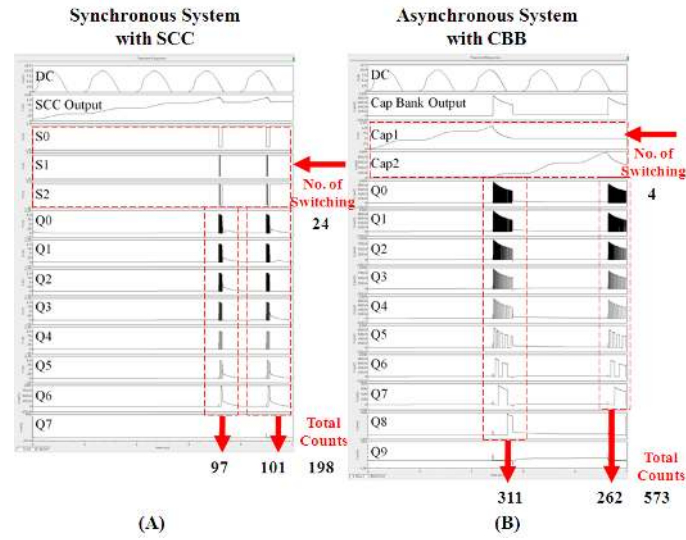
Figure 10. The Counter Performances in Terms of Synchronous System with SCC (A) and Asynchronous System with CBB (B)

- Energy Consumption of Switching and Control

Table 5. Energy Consumed for Switching and Control

	Synch System with SCC	Asynch System with CBB
Energy Consumed for Switching (pJ)	54.1	1.51
Switching Times	24	4
Energy Consumed per Switching (pJ)	2.25	0.38
Energy Consumed for Control (pJ)	277	9.97

In Table 5, the energy consumption for switching is compared for synchronous load with SCC and asynchronous load with CBB. The synchronous load with SCC consumes significantly more energy than asynchronous load with CBB due to frequent switching in the SCC. And the synchronous load with SCC has much higher energy consumption per switching than the asynchronous load with CBB. The more complex control block in the SCC means that the energy used for control by the SCC is considerably higher.

- Energy Delivery Efficiency

Table 6 shows the energy delivery efficiency performance in terms of synchronous load with SCC and asynchronous load with CBB. The energy delivery efficiency advantage by the CBB over the SCC is the same as the advantage in the total counts, i.e. twice.

Table 6. Energy Delivery Efficiency of Different Systems

	Synch System with SCC	Asynch System with CBB
Total Counts	198	573
Self-timed Counter (pJ)	5.04	10.6
Harvested Energy (pJ)	18.5	18.5
Energy Delivery Efficiency	27.2%	57.3%

C. Systems working with Adequate Power Supply

- Computation Performances and Switching Times

In this group of experiments, the EH power supply is assumed to be able to deliver high amounts of current with a peak value of 1mA. In this case, the performance achieved by the synchronous load with SCC is significantly increased. The synchronous load with SCC gets 821 counts within 1us with 149 internal SCC switchings. Compared with synchronous load with SCC, the asynchronous load with CBB gets 757 counts within 1us, but the capacitors retain a lot of unspent energy at the end of this period.

However, if after 1 us the EH stops, the synchronous system with SCC cannot work without power supply, but the case is very different in the CBB. At 1 us, Cap3 to Cap7 are still fully charged and Cap 8 is charged to 0.47 V. The asynchronous load can work for a further 1.88 us to deliver 1512 more counts. In the whole process there are 15 switchings within the CBB, which is 10% of the number for the synchronous load with SCC.
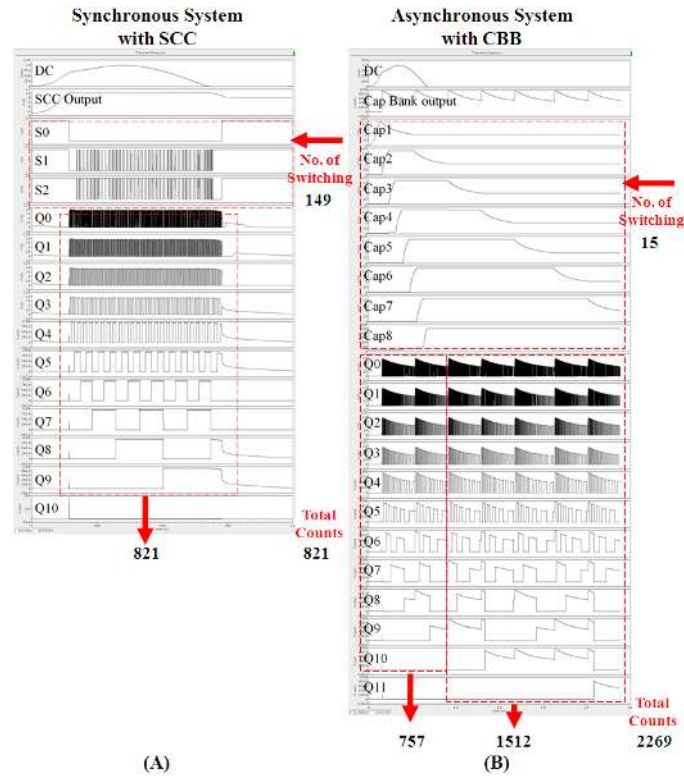
Figure 11. The Counter Performances in Terms of Synchronous System with SCC (A) and Asynchronous System with CBB (B)

- Energy Consumption of Switching and Control

Table 7. Energy Consumed for Switching and Control

	Synch System with SCC	Asynch System with CBB
Energy Consumed for Switching (pJ)	90.5	35.3
Switching Times	149	15
Energy Consumed per Switching (pJ)	0.61	2.35
Energy Consumed for Control (pJ)	158	25.3

Table 7 shows the energy consumption of switching and control comparison. For switching energy, as before the SCC system has a higher number of switching but a lower per switching energy than the CBB system. The result of per switching energy is exactly opposite

of that in Table 5. The SCC system also has higher control energy consumption than the CBB system.

- Energy Delivery Efficiency

Table 8 shows that although asynchronous load with CBB achieves 2269 counts, which is approximately 2.8 times that of synchronous load with SCC, the former consumes 33.8pJ, only 1.8 times that of the latter. This is unsurprising as the former has higher energy delivery efficiency.

The energy delivery efficiency of all experimental systems become lower when EH supply is increased, with the highest efficiency corresponding to peak current of 10 uA and lowest corresponding to 1 mA. We will, in the future, investigate this phenomenon with heavier computational loads which may be able to draw higher power at higher Vdd.

Table 8. Energy Delivery Efficiency of Different Systems

	Synch System with SCC	Asynch System with CBB
Total Counts	821	2269
Self-timed Counter (pJ)	18.7	33.8
Harvested Energy (pJ)	369	369
Energy Delivery Efficiency	5.1%	9.2%

VI.   Energy Consumption Analysis

The energy consumption of each component is obtained and converted into average energy consumption over 1 us in this study.

The synchronous load with SCC structure has five main components: SCC, asynchronous controller, comparator block, conversion ratio selector, and self-timed counter, as shown in Figure 1 and Figure 7 (A). Figure 12 shows the average energy consumption for the five components working with EH supply peak values of 10uA, 100uA, and 1mA. The

comparator block consumes the largest amount of energy, followed by the SCC, the asynchronous controller and self-timed counter. The conversion ratio selector consumes negligible amounts of energy.
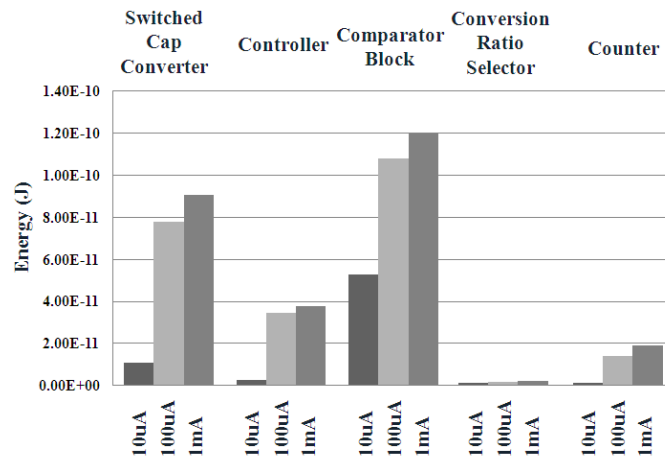

Figure 12. Average Energy Consumption for Each Component in Synchronous System with SCC Working with Sparse, Moderate, and Adequate Power Supplies
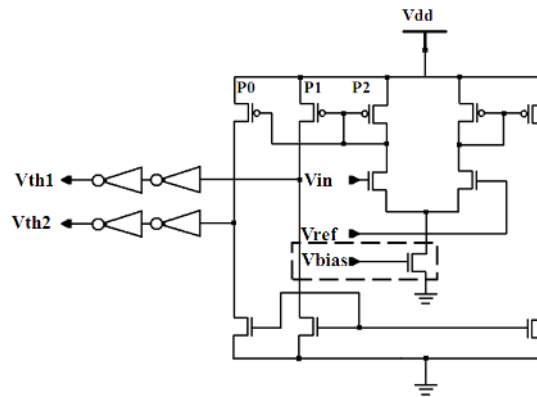

Figure 13. Comparator Block Structure inside of SCC [11]

In the comparator block, the relatively high energy consumption may be caused by the input of V_{bias}, shown in Figure 13. The transistor connected to V_{bias}, is connected to GND, and the energy consumption of the comparator is mainly decided by V_{bias}. In these

experiments, V_{bias} has to be maintained at least above 0.35 V to generate stable 1 V power supply at the output of SCC for a 1/1 conversion ratio.

The asynchronous load with CBB structure also contains five main components: charging and discharging selectors, switching block in CBB, CBB itself, self-timed counter, and Vpwlf voltage source block, as shown in Figure 7 (B). Figure 14 shows that the self-timed counter consumes the highest amount of energy in the whole system except for the case of the 1mA peak EH current, where the switching block consumes slightly more energy. Comparing the two systems it is clear that the CBB method delivers proportionally more energy to the load than the SCC method, which consumes a large majority of the energy running itself.
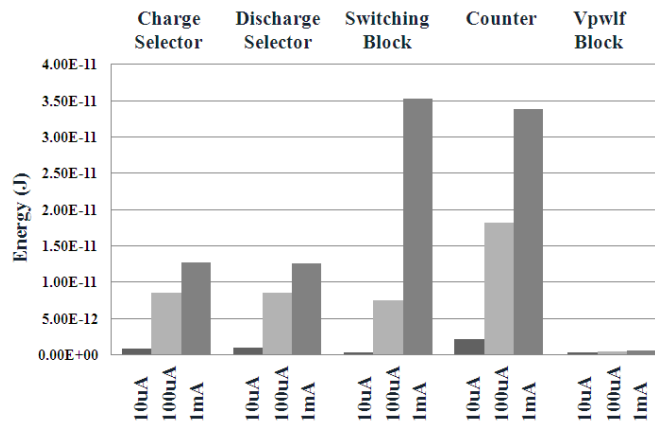

Figure 14. Average energy consumption for each component in asynchronous system with CBB working with sparse, moderate, and adequate power supplies

VII. Discussions and Conclusion

The results in the previous sections show that both the SCC and CBB systems as constructed and working under these specific conditions have quite low energy delivery efficiency compared with normal DC/DC converters working under ideal conditions. For instance, buck DC/DC converters with stable power supply can have approximately constant converter efficiencies between 75% and 95% [19].

However, EH systems tend to have highly time-variable power supply. Power delivery units based on techniques targeting a relatively stable power source cannot maintain high conversion efficiency under such radically variable power source. This is confirmed by the data from the standard SCC and a relatively dumb CBB.
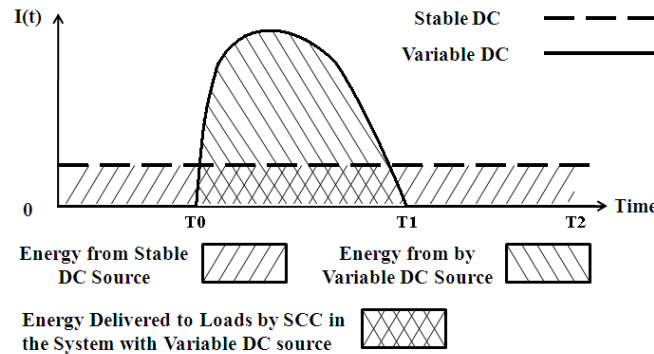

Figure 15. Energy Distribution from Stable DC Source and Variable DC Source

Figure 15 compares the stable DC source with a variable EH output curve. Suppose the voltage of each power supply is the same and from 0 to T_2, the total energy provided by the stable DC source is the same as that provided by the variable DC source. Based on this assumption, by employing SCC, the system with stable DC power supply can enable the load to work as long as the stable power is available. The working period of the system is from 0 to T_2. The efficiency lost in the SCC is mainly caused by the SCC resistance and circuit leakage. Therefore, it is possible to achieve very high energy delivery efficiency.

Given the variable EH supply, however, power from the supply is non-zero only from T_0 to T_1. A system with the same SCC and load has to wait until enough energy is accumulated for the load to start working. In fact, when the variable current continues rising, the power provided by the source is too high at the input of the SCC. As SCC has to maintain the constant power supply at the output, the surplus energy from the source is not passed to the load. Some of this is stored in the capacitors in the SCC but most of this stored energy will

not be made available to the load once the EH supply ends, because of the SCC switching algorithm which is focused on a pre-set conversion ratio.

The CBB is not designed for working with stable power inputs and is a relatively poor performer in this situation, but it makes it possible to store the energy from the EH source when the latter provides more power than can be consumed by the load. This stored energy can then be maximally delivered to the load when less is available from the EH source.

A CBB with the basic mechanical FIFO charging and discharging sequence is demonstrated to be superior to an SCC in almost all working conditions and in some cases far superior, with a highly variable EH supply. The advantage of additional flexibility in the charging and discharging algorithm is demonstrated with a small example in this paper (Figure 9).

The CBB needs a voltage sensor to implement precise charging and discharging cycles and sophisticated switching algorithms. The multiple capacitors in the CBB, potentially of different values, provide a degree of flexibility and programmability for the CBB method which, if fully exploited, will further improve energy delivery efficiency.

Asynchronous loads, which are becoming more common for energy conscious design because of their low-power and energy-adaptive characteristics, can in general work under a wide Vdd range. This wide working Vdd range remains unexploited by designs of power delivery devices which are currently still focused on maintaining stable and known Vdd values.

The CBB method represents the first attempt at developing appropriate power and energy delivery units suitable for loads which can tolerate and work well under highly variable Vdds and energy sources which cannot maintain constant outputs. The methodology is simple, based on charging and discharging capacitors in a group, and produces devices which can be implemented on chip, potentially advantageous for extreme miniaturization. It also provides

enough flexibility for intelligent control aimed at maximizing performance or energy efficiency as well as other quantifiable goals. The initial successes reported in this paper shows that alternative power delivery methods such as CBB should be further explored and intelligent control for such systems further investigated.

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