A Novel Reconfigurable OFDM Based Digital Modulator

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Abstract— **Digital modulation is the first step in the digital communication system (DCS). The choice of modulation scheme among BPSK, QPSK, 8-QAM and 16-QAM are made based on the performance criterion such as bit-error-rate (BER) and bandwidth (BW) utilization. Hence the operating range of the DCS is improved by incorporating all the four modulation schemes in architecture. In this paper, a reconfigurable digital modulator is proposed for OFDM based DCS with more hardware efficiency (data rate per number of gates used in the architecture) by concurrent operation of different modulation schemes. Complex reconfiguration control logic is developed to maintain less idle period between the modes which is observed as maximum of 4 clock periods. The proposed reconfigurable modulator is implemented on Cyclone-II family of EP2C20F484C7 FPGA chip, which utilizes 34 logic elements (less than 1%), consumes 78.73 mW of power at 200MHz clock frequency.**

Keyword- Digital communication systems (DCS), Digital modulation, OFDM, Reconfigurable systems and FPGA

I. INTRODUCTION

The application of OFDM in wireless communication devices is inevitable. The multicarrier modulation communication (MCM) gives better error characteristics due to orthogonal subcarriers which carries the information, though these are overlapping and yet do not interfere [1, 2] and maximum utilization of bandwidth [2]. Digital modulation techniques like BPSK, QPSK, 8-QAM and 16-QAM were giving different spectral efficiency, which leads to the different OFDM-based wireless communication standards. When the channel is noisy and no constraints on the channel bandwidth, BPSK would be the best choice. But the compromise is on spectral efficiency. The channel is less prone to noise; more data can be packed by QAM [3]. Another performance metric, bit error rate (BER) has to be as low as possible. Though the BPSK guarantees lowest BER possible, bandwidth usage can be doubled in QPSK and its further more in the QAM. As these schemes use more symbols, they enjoy lesser bandwidth, but at the expense of correct receiver prediction (high BER) [4].

Considering the facts discussed a reconfigurable digital modulation unit is proposed in this paper, which can modulate the given bit stream in to another using any one of four forms. It will be capable of performing BPSK, QPSK, 8-QAM or 16-QAM modulation using the same hardware. The hardware utilization efficiency is maximized by operating the modulation process in parallel, which is the key requirement for the modern MIMO wireless communication systems. While performing one modulation, if some hardware units are free, this system architecture will also allow us to perform modulation on another data stream in parallel. The proposed architecture will allow us to move from one modulation scheme to other, which is higher in terms of symbols to represent the information. These combinations can be selected by the user.

II. PREVIOUS WORK

The Modulation scheme plays a very vital role in deciding of hardware implementation of a OFDM transmitter/receiver. The number of IFFT/FFT operational units required was decided by the modulation scheme. A transmitter with BPSK requires an N-point IFFT unit, N is chosen as per the wireless standard specification. Therefore the modulation scheme chosen is actually a trade-off between the design complexity and signal performance. This paper plans a new form of implementation for the M-QAM modulator.

The flexible digital modulator was using look-up tables (LUTs) to implement the various modulation schemes [5], a unique group of LUTs would be used for each modulation schemes. The binary bit stream of length *n* passed through an *n*-bit serial-to-parallel converter to determine a symbol. Every point in a constellation diagram represents a symbol which has a unique bit representation [6]. The symbols for different modulation schemes can be expressed as:

- Each symbol for QPSK is determined as b1*2 + b0 and then mapped using a LUT.

- Each Symbol for 8-QAM is determined as b2*4 + b1*2 + b0.
- Each Symbol for 16-QAM is determined as b3*8 + b2*4 + b1*2 + b0.

During the formation of modulator blocks, it was found that one modulation scheme can be represented as a sub set of higher modulation technique as given in Fig. 1. Two points of QPSK constellation matches with that of one BPSK. Again QPSK can be called as 4-QAM as it uses a sub-portion of the QAM constellation. Similarly 8-QAM is a part of 16-QAM, and 16-QAM forms a sub-part of higher order QAM. The significance of highlighting a subpart from the whole constellation, is that, if we have the resources to produce 16-QAM, we should also be capable of producing 8-QAM, QPSK and BPSK same resource. Similarly, a hardware that can produce higher order QAM can also produce 16-QAM.

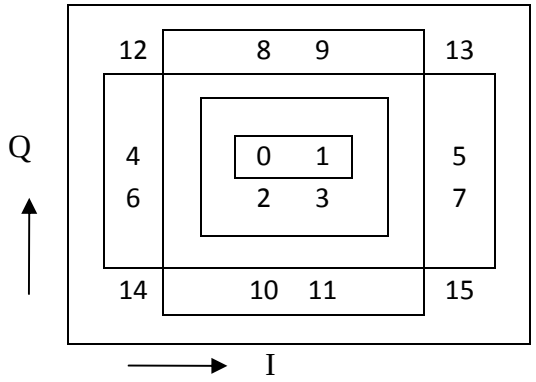

Fig 1: The constellation diagram for the scalable modulator (BPSK to 16-QAM)

The 8-QAM, QPSK, or BPSK can use the constellation points of 16-QAM and of higher level QAMs. Making this happen will result to one LUT for all the modulation schemes, unlike conventional implementation which uses different LUTs for every modulation scheme. This single LUT will store all the possible values which a particular modulation scheme may require to map the bits into symbols to be transmitted.

III. DESIGN OF DIFFERENT MODULATION SCHEMES

The requirements of different modulation schemes are explained in this section. A shift register can be used for the implementations and the effects on sampling rate are analysed as follows:

A. Binary Phase Shift Keying (BPSK)

The BPSK unit has one input and one output. The output pattern is similar to the input with one clock delay. So the BPSK modulator can be realized as unit buffer as shown in Fig.2 (a).

B. Quadrature Phase Shift Keying (QPSK)

The QPSK has one serial input line and two parallel output lines. The two output lines are termed as in-phase (I) and quadrature phase (Q) as in [7]. After two bits have been serially clocked into the QPSK modulator, on the third clock a combination of two parallel bits are obtained at the output lines. This can be realized using serial-in parallel-out (SIPO) shift register as shown in Fig.2 (b). The output of QPSK is sampled at a frequency equal to half of the input bit rate. Since output bits are two, there are four possible combinations, each of which is called a symbol.

C. QPSK with an amplitude modulation (QAM) in one dimension (8-QAM)

Extending the above concept of QPSK and amplitude modulation, a 8-QAM can be realised. A SIPO shift register having one serial input and three parallel outputs is used for the implementation. The amplitude modulation can be either in I axis or Q axis. Correspondingly the implementations are resulted as shown in Fig.2 (c) and (d). Since the QPSK has eight possible constellation symbols and the output sampling rate is one-third of input bit rate [9].

D. QPSK with an amplitude modulation in two dimensions (16-QAM)

A similar realization has been extended to QPSK with an amplitude modulation in two dimensions. Now a 4-bit SIPO shift register is required for the implementation as shown in the Fig. 2 (e). This has one serial input and four parallel outputs, I0, Q0, I1, and Q1. Since it has sixteen possible constellation symbols at its output and is sampled at one-fourth of the input bit rate.

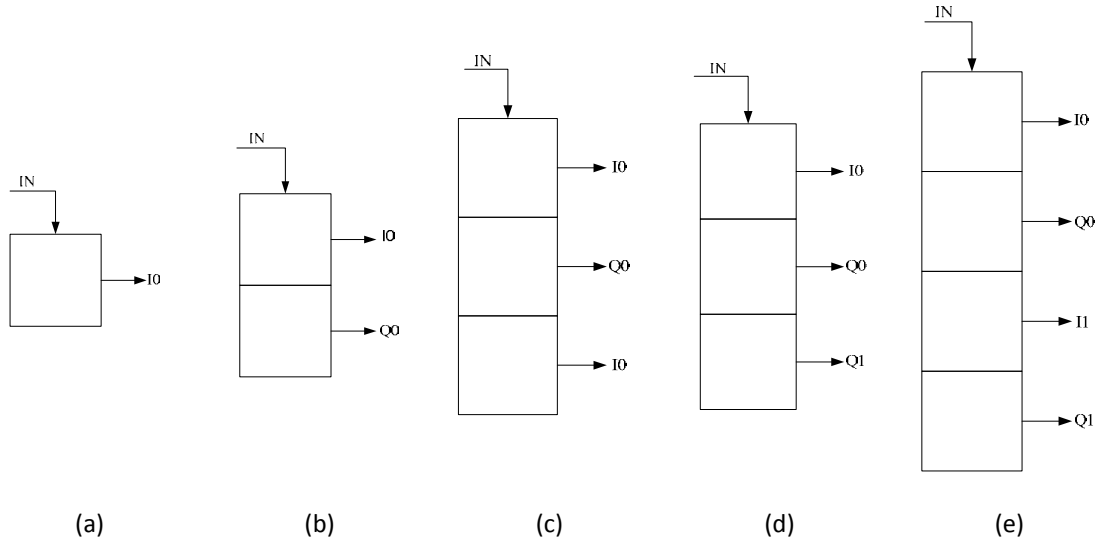

Fig 2: SIPO shift register implemented as digital modulator
(a) BPSK, (b) QPSK, (c) 8-QAM- Amplitude modulation in I, (d) 8-QAM- Amplitude modulation in Q, (e) 16-QAM

IV. PROPOSED ARCHITECTURE

The proposed architecture is scalable digital modulator for OFDM applications which can convert the given bit stream in to output bit stream using any one of the four modulation techniques: BPSK, QPSK, 8-QAM, 16-QAM. In contrast to the previous architecture the concurrent functioning of the modulation operations were implemented to enhance the hardware utilization efficiency. This has resulted in the complex control strategies. This chapter explains the design of proposed architecture. The top module of the scalable modulator with possible inputs {IN1, IN2, IN3, IN4}, outputs {I0, Q0, I1, Q1}, clock, Reset and control signals {C2, C1, C0} are shown in Fig. 3.

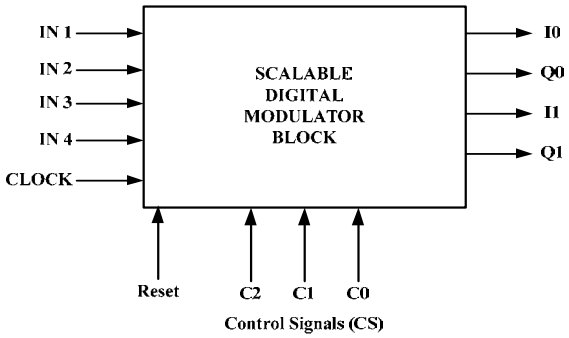

Fig 3: Top module – inputs, outputs, clock and control signals

The different input-output mappings according to the intended modulation scheme were controlled by three control signals. The eight combinations results in eight distinct modes of operations. The asynchronous control signals {C2, C1, C0} are generating enable signals {CL11, CL22, CL33, CL44, CL1, CL2, CL3} for the tri-state buffers. The data flow in the architecture is controlled by tri-state buffers and the OR gates. The D-flip-flops helps to maintain the synchronized data flow in the four modulation schemes (BPSK, QPSK, 8-QAM, 16-QAM). The Table I illustrates eight modes, respective control signals and its input output pin map.

A) Control Logic Signal Block:

The truth table presented in Table II, illustrates all possible control signals and its corresponding tri-state buffer enable signals. Therefore it ensures concurrent operation of more than one modulation schemes and isolation of any input signal applied to a node which is not an input node.

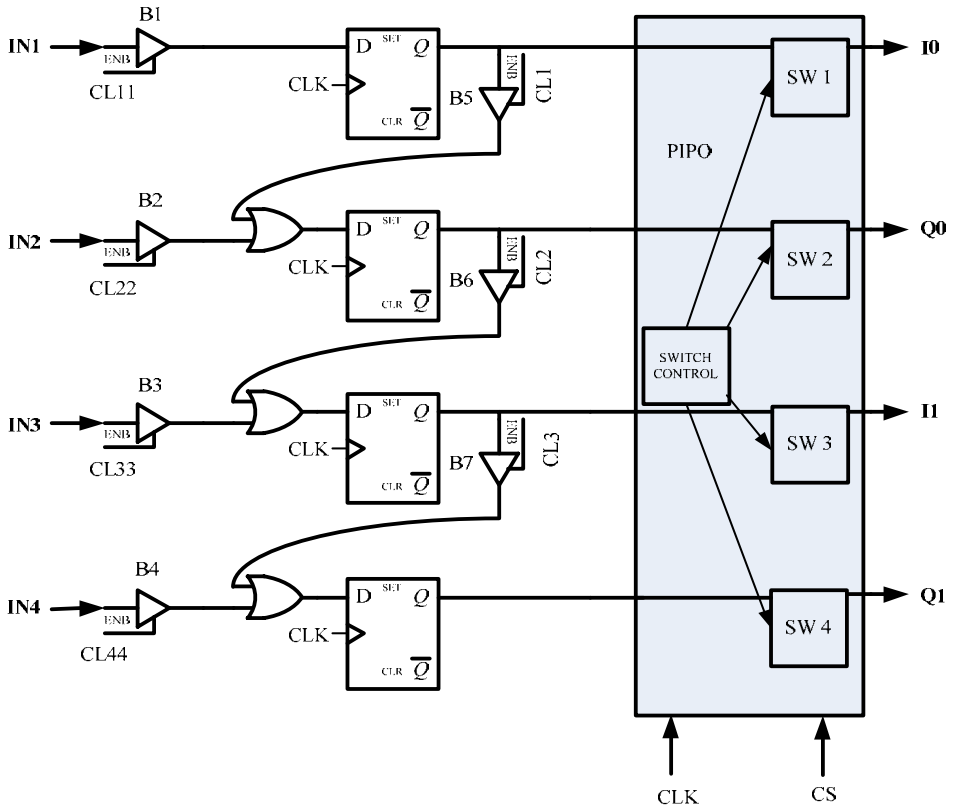

Fig 4: Proposed architecture of scalable modulator

TABLE I: DESCRIPTION OF MODES – control signals and input and output pins assigned

CS			Mode	Mode of operation	Input	Output
C2	C1	C0				
0	0	0	0	BPSK 1	IN 1	I0
				BPSK 2	IN 2	Q0
				BPSK 3	IN 3	I1
				BPSK 4	IN 4	Q1
0	0	1	1	BPSK 1	IN 1	I0
				BPSK 2	IN 2	Q0
				QPSK-2	IN 3	I1
						Q1
0	1	0	2	QPSK 1	IN 1	I0
						Q0
				QPSK 2	IN 3	I1
						Q1
0	1	1	3	BPSK-1	IN 1	I0
				8-QAM	IN 2	Q0
						I1
						Q1

CS			Mode	Mode of operation	Input	Output
C2	C1	C0				
1	0	0	4	16-QAM	IN 1	I0
						Q0
						I1
						Q1
1	0	1	5	BPSK-1	IN 1	I0
				QPSK-2	IN 2	Q0
						I1
				BPSK-4	IN 4	Q1
1	1	0	6	QPSK-1	IN 1	I0
						Q0
				BPSK-3	IN 3	I1
				BPSK-4	IN 4	Q1
1	1	1	7	8-QAM	IN 1	I0
						Q0
						I1
				BPSK	IN 4	Q1

For example if the 16-QAM is in operation then the input is received through IN1 and the other inputs are isolated. The control logic signal block is illustrated in Fig. 5. Consider an example where input control signal CS is given as {C2, C1, C0} = 3'b000. The CS block will activate the following signals CL11, Cl22, CL33, CL44 as high while CL1, CL2, CL3 will be activated to low. The CL11, CL22, CL33, CL44 will activate all the buffers B1, B2, B3 and B4. At the same time CL1, CL2, CL3 will deactivate the buffers B5, B6, B7 and the high impedance state of the buffers isolates the D-latches in the data flow. Thus all the four input signals can now undergo BPSK modulation technique.

TABLE II: TRUTH TABLE FOR CONTROL LOGIC (CL)

User input (CS)			Control Logic – outputs						
C2	C1	C0	CL1	CL2	CL3	CL11	CL22	CL33	CL44
0	0	0	0	0	0	1	1	1	1
0	0	1	0	0	1	1	1	1	0
0	1	0	1	0	1	1	0	1	0
0	1	1	0	1	1	1	1	0	0
1	0	0	1	1	1	1	0	0	0
1	0	1	0	1	0	1	1	0	1
1	1	0	1	0	0	1	0	1	1
1	1	1	1	1	0	1	0	0	1

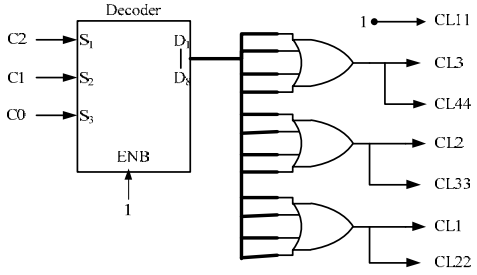

Fig 5: Schematic view of Control Logic Block

B) D Flip Flops:

The D flip flops are introduced to avoid race conditions, provided stability to the values latched at the output and provide isolation from any static and dynamic hazards generated from previous modules. Thus we are able to get a glitch free output.

C) Parallel Input Parallel Output (PIPO):

PIPO module in the proposed architecture is responsible for converting the input to required modulation technique. The function of PIPO is to pass the parallel input data_in x bits to I0, Q0, I1, Q1 bits depending on the control signal CS. The Fig 6 illustrates the PIPO internal structure that is implemented using four controllable switches and a switch control block.

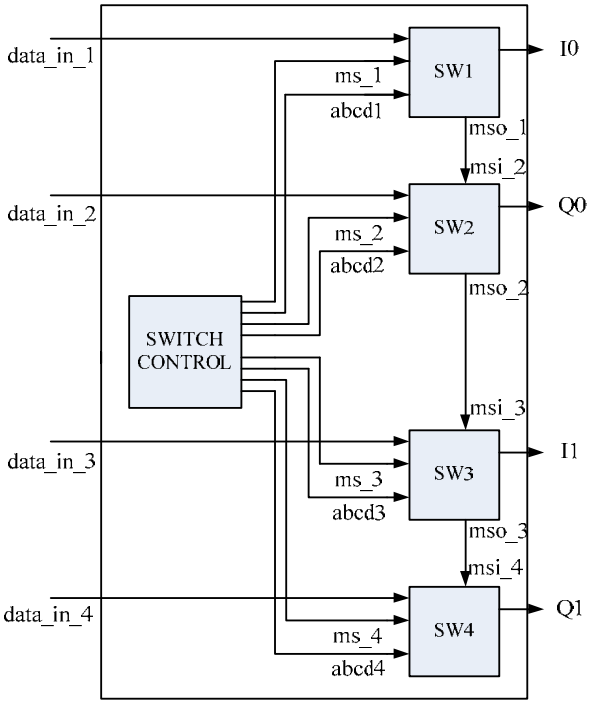

Fig 6: PIPO Internal structure

The four switches are operated in “master/slave”. The signal *ms_x* is selecting a switch as either master by setting *ms_x=1* or slave by *ms_x=0* . There is clock division logic inside the each switch which varies the switching frequency to half/one-third/one-fourth when the modulation changes from BPSK to QPSK/8-QAM/16-QAM especially in master mode. This control signal is derived inside the switch from one of the divided clock signals through the mux. This signal is also passed to the output pin master-slave-output (*mso_x*). In slave mode, the master-slave-input (*msi_x*) becomes the control signal. The eight control signals are defining the current modulation scheme in operation accordingly the 2-bit abcd_x signal is generated. This 2 bit select signal (abcd_x) controls the multiplexer in the SWx and selects the frequency of occurrence of switch control.

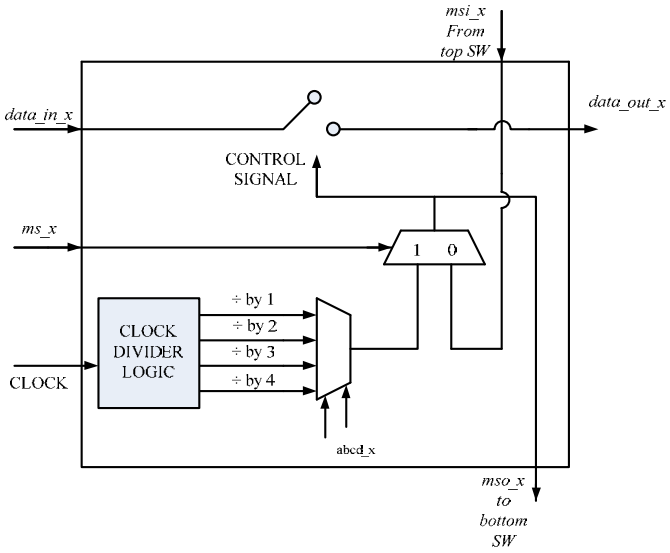

Fig 7: Switch Internal logic

It is clear from the Fig 6, SW1 is always master and the rest of the switches can be either master or slave as per the modulation scheme selected at that time instance. There are many master/slave combinations possible and are shown in Table III. The proper selection of "slave" mode is to provide data flow synchronization for the mode selected and operational currently.

Table III :Switch status in different modes

Mode	**Switch status**			
	SW1	**SW2**	**SW3**	**SW4**
0	Master	Master	Master	Master
1	Master	Master	Master	Slave
2	Master	Slave	Master	Slave
3	Master	Master	Slave	Slave
4	Master	Slave	Slave	Slave
5	Master	Master	Slave	Master
6	Master	Slave	Master	Master
7	Master	Slave	Slave	Master

V. FPGA IMPLEMENTATION:

The proposed architecture was described using Verilog HDL. The design was simulated using ModelSim for the functional correctness. To validate the design, it was synthesized and implemented on Cyclone-II family of EP2C20F484C7 FPGA 90 nm process technology chip using Quartus II. The FPGA chip has 18,752 logic elements, 25 registers, 315 pin outs, internal memory of 234Kbits, 52 embedded multipliers of 9-bit word length, 1.2 V core voltage and 4 internal PLLs. The maximum frequency at which the FPGA chip can be clocked is 402.58 Mhz. The post synthesis gate level simulation of the proposed design was performed to verify the functional correctness and timing requirements after implemented on a specific FPGA chip. The Power Play analyser was used to estimate the power consumption. The Classic Timing analyser was used to estimate the time of execution. The analysis of reconfiguration schedule is conducted and reconfiguration delays are measured and tabulated in Table IV.

Table IV: Reconfiguration schedule of modes in terms of number of clock (C) periods

Current Mode	Next Mode									
		0	1	2	3	4	5	6	7	Reset
	0	-	2C	2C	3C	4C	2C	2C	3C	1C
	1	1C	-	2C	1C	2C	2C	2C	3C	1C
	2	1C	1C	-	1C	2C	1C	1C	1C	1C
	3	2C	2C	2C	-	1C	2C	2C	3C	1C
	4	3C	3C	2C	1C	-	2C	2C	1C	1C
	5	1C	2C	2C	1C	2C	-	2C	1C	1C
	6	1C	2C	2C	3C	4C	2C	-	1C	1C
	7	2C	2C	2C	3C	1C	2C	2C	-	1C
	Reset	1C	1C	1C	1C	1C	1C	1C	1C	-

VI. RESULTS

The proposed reconfigurable digital modulator for OFDM application was implemented on Cyclone II EP2C20F484C7 FPGA chip. The design can convert the given data stream in to constellation symbols using BPSK, QPSK, 8-QAM and 16-QAM methods. Complex control logic was designed and implemented to utilize the hardware maximally by providing parallel operation of more than on modulation schemes. The user provoked reconfiguration was performed with minimal delay to change from one mode to other, which was found to be 4 clock period from the Table IV. The floor plan is presented in Fig 8 and performance parameters of the implementation were tabulated in table V.

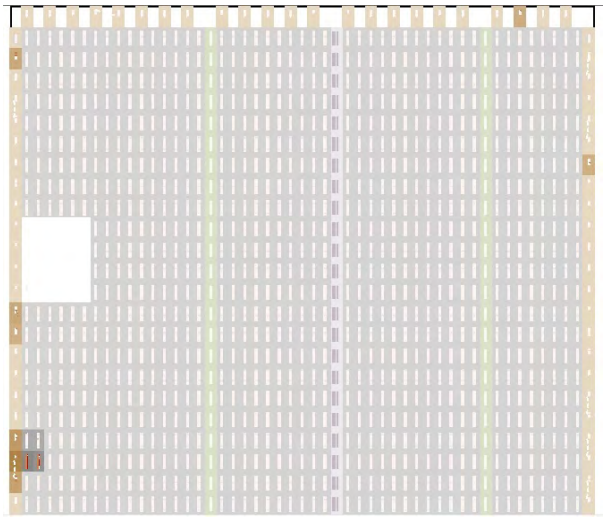

Fig 8: Floor plan view of the implementation

Table V: Performance parameter of the proposed implementation

Performance Parameters	
Design Summary	
Total logic elements	34 / 18,752 (< 1 %)
Total combinational functions	34 / 18,752 (< 1 %)
Dedicated logic registers	25 / 18,752 (< 1 %)
Timing Calculations	
Time (ns)	3.579
Maximum Frequency (MHz)	279.41
Power Calculations	
Total Thermal Power Dissipation (mW) at 200 MHz	78.73

VII. CONCLUSION

The power of reconfiguration was used to improve the operating range of the OFDM application by incorporating four modulation schemes in architecture. By concurrent operation of modulation schemes, the proposed architecture can work for MIMO wireless communication systems. From the Table V, less than 1% of the FPGA resources had been used for the implementation and it works at 200MHz, which is well above the most common wireless standards like WLAN, WiFi, etc.

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