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A novel resonant transition push–pull DC-DC converter

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Abstract

In hard-switched converters, the switching frequency is limited by switching losses and EMI problems. However, high-switching frequency is necessary to reduce the converter size. Hence, soft switching is imperative at high switching frequency to obtain good efficiency. Push–pull converter is a preferred topology at medium power level. This paper proposes a novel resonant transition topology for push–pull converter. The proposed topology uses two additional switches and two diodes when compared to hard-switched push–pull converter. These extra switches introduce freewheeling in the primary circuit and thus enable loss-less switching. In classical push–pull converters, the transformer primary is left open during two sub-intervals in a period making the turn-on of the switch hard. The new circuit topology converts these open circuit intervals into freewheeling ones. With such a modification, all trapped energy in the core is conserved to achieve zero-voltage switching during the entire transition. Switch stress, control and small signal model are similar to hard-switched PWM converter. Idealized analysis and design methodology are explained for the push–pull converter. A prototype–300 kHz, 200 W push–pull converter validates the design method. Dynamic analysis of the push–pull converter is presented. The proposed topology can be extended to half-bridge converter also. Its circuit diagram is presented.

Keywords: Half-bridge converter, push–pull converter, zero-voltage switching and resonant transition.

1. Introduction

Switched-mode power supplies (SMPS) being efficient and compact are extensively used in power conversion processes. The analysis, design and modeling processes have all matured in the past three decades. Most of these developments centered around hard-switching converters, where the switching frequency was limited to a few 10s of kHz. The present direction of evolution in SMPS is towards higher efficiency and higher power density. These twin objectives demand high switching frequency and low overall losses. Soft switching results in practically zero switching losses and extends the switching frequency to 100s of kHz and beyond. The soft-switching converters belong to several families, namely, resonant load [1], resonant switch [2], resonant transition [3] and, more recently, active clamped circuit topologies [4]. The resonant load converters depend on the characteristics of the load to achieve soft switching. The resonant switch converters have additional elements in the

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switch enabling loss-less switching. Resonant transition converters employ the parasitic of the circuit to achieve loss-less switching.

This paper presents novel variant of push–pull DC-DC converter with soft-switching properties. Push–pull converter is a popular power converter at medium power level. It is characterized by circuit intervals when both power transfer switches are off. Such circuits exhibit hard switching and are not readily adaptable to soft switching. The proposed topology uses two additional switches and two diodes. The additional switches introduce free-wheeling intervals in the circuit and enable loss-less switching. The following are the features of the new circuit:

1) Loss-less switching transition for all the switches employed.
2) Switch stress similar to hard-switched PWM converter.
3) Conduction loss is almost the same as hard-switched PWM converter.
4) Control and small signal behavior is similar to hard-switched PWM converter.

2. Proposed push–pull converter and operation

Figure 1 shows the proposed zero-voltage switching (ZVS) push–pull converter. This circuit is obtained from the hard-switched push–pull converter by connecting two switches (S_3 and S_4) and two diodes (D_3 and D_4). The leakage inductance of the transformer is lumped on the secondary side and is represented as L_{lk}. C_1 and C_2 are the snubber capacitors.

Figure 2 indicates the gate pulses V_{g1}, V_{g2}, V_{g3} and V_{g4} for the switches S_1, S_2, S_3 and S_4, respectively. S_3 and S_4 have a duty ratio of nearly 50% (with a small dead time). The dead time (T_d) is also shown in Fig. 2.

Idealized operation of the circuit is explained by a set of six intervals. Figure 3 shows the idealized waveforms of primary switch current, snubber capacitor current and secondary diode currents.

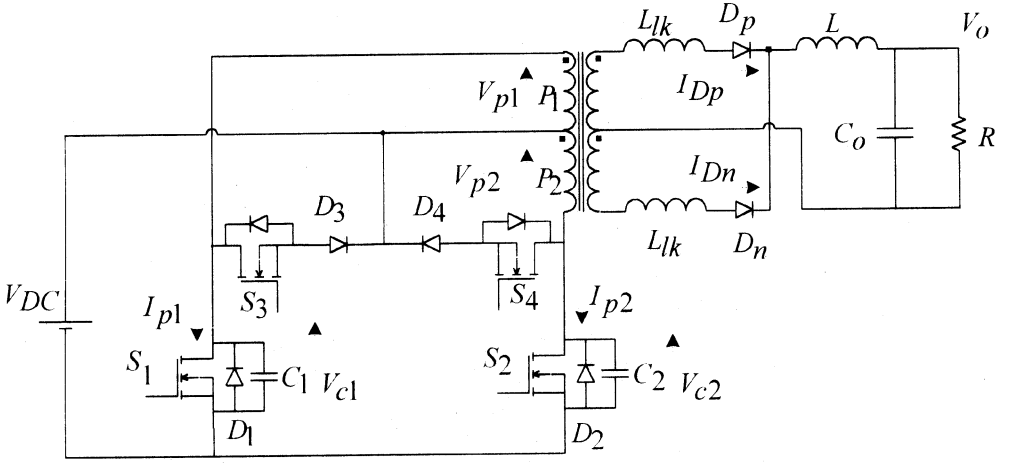

FIG. 1. ZVS push–pull circuit.

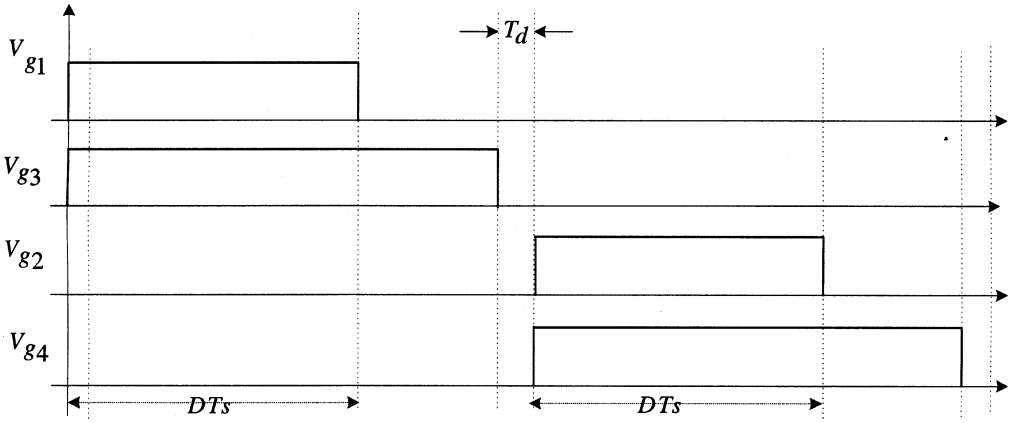

FIG. 2. Control pulses.

The following are the assumptions made during the idealized analysis:

1) Switching devices are ideal.
2) Diodes are ideal.
3) Device output capacitance is neglected. Only the effect of snubber capacitor is considered.
4) Primary leakage inductance effects are neglected.

2.1. *Interval* T_1 ($t_0 < t < t_1$)

In interval T_1, S_3 and S_4 are on. When S_1 is conducting, diode D_3 is reverse biased in the primary circuit. In the secondary circuit diode, D_n is forward biased. This interval is known

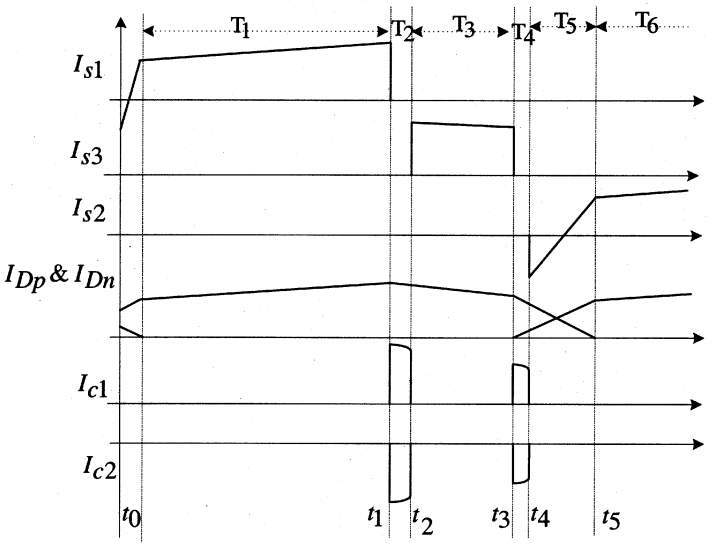

FIG. 3. Idealized waveforms.

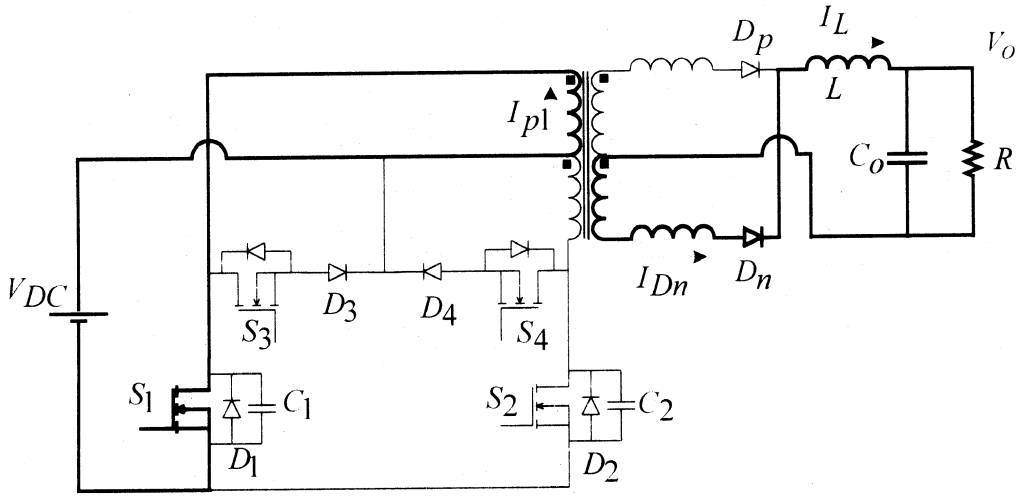

FIG. 4. Conduction path in Interval T_1.

as power transfer interval. During this interval, power is transferred from primary to secondary. Figure 4 shows the conduction path.

2.2. *Interval* T_2 ($t_1 < t < t_2$)

Interval T_2 begins when S_1 is turned off. The snubber capacitor C_1 assists the turn-off process of S_1. As the turn-off process is capacitor assisted, the turn-off process is low-loss switching transition. The magnetizing current and reflected current charge C_1 from 0 to V_{DC} and discharge C_2 from $2V_{DC}$ to V_{DC}. Although S_3 is on, D_3 is still reverse-biased because the voltage V_{C1} has not reached V_{DC}. In the secondary circuit, D_n takes the load current. This

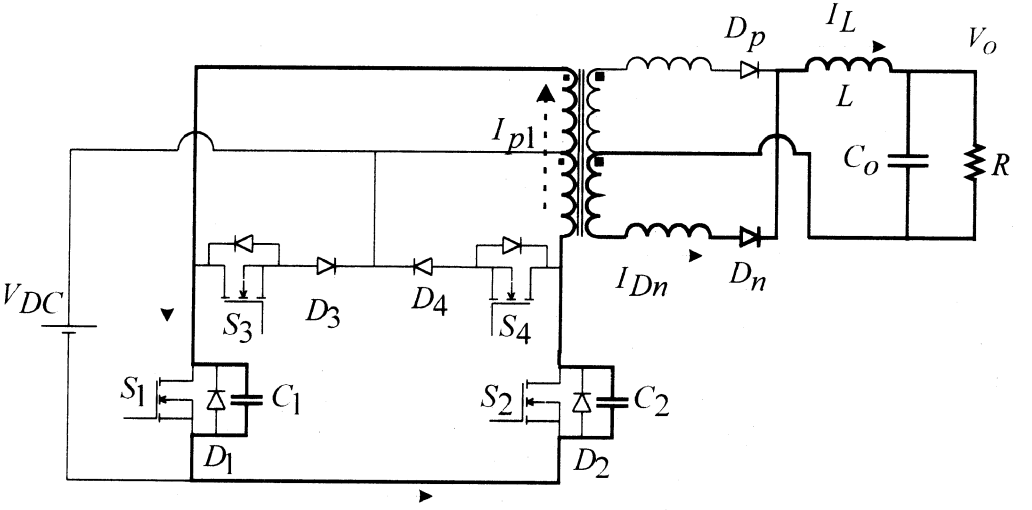

FIG. 5. Conduction path in Interval T_2.

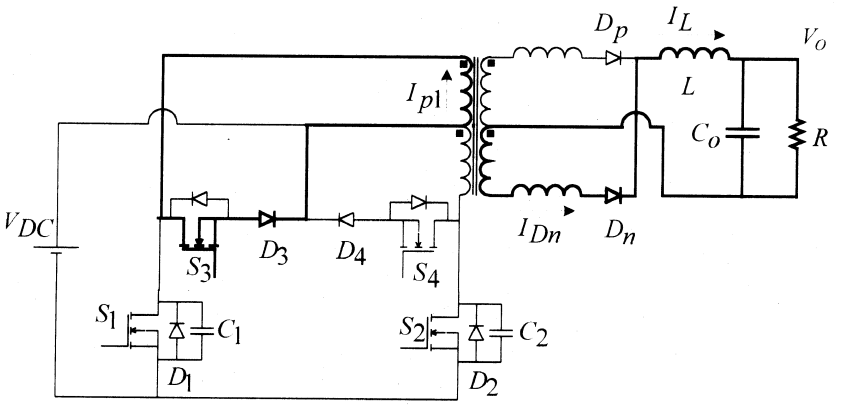

FIG. 6. Conduction path in Interval T_3.

interval is known as resonant transition-I interval. Figure 5 shows the conduction path in interval T_2.

2.3. *Interval* T_3 ($t_2 < t < t_3$)

Interval T_3 begins when C_1 is charged to V_{DC}. As C_1 is charged to V_{DC}, D_3 is forward-biased. The magnetizing current and reflected current I_{P1} freewheel through S_3 and D_3. This interval is known as freewheeling interval. The leakage inductance L_{lk} ensures that only D_n takes the load current. Figure 6 shows the conduction path.

2.4. *Interval* T_4 ($t_3 < t < t_4$)

At the start ($t = t_3$) of this interval, S_3 is switched off. The magnetizing current and reflected current charge C_1 from V_{DC} to $2V_{DC}$ and discharge C_2 from V_{DC} to 0. This interval is known as resonant transition-II interval. Figure 7(a) shows the conduction path. From the figure it is clear that reflected current and magnetizing current discharge C_2. So magnetizing induc-

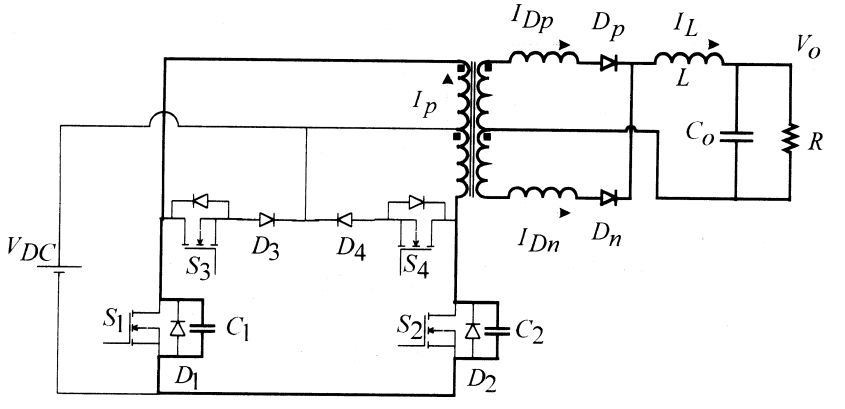

FIG. 7(a). Conduction path in Interval T_4.

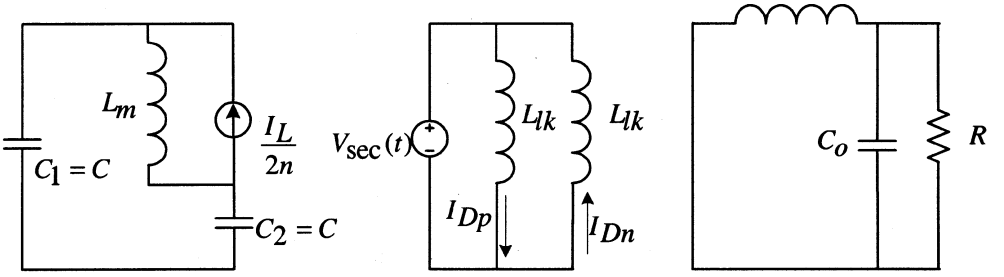

FIG. 7(b). Equivalent circuit for Interval T_4.

tance and leakage inductance have to be designed to discharge C_2. In the secondary circuit, the load current starts shifting from D_n to D_p.

Figure 7(b) shows the equivalent circuit for interval T_2. It clearly shows that the secondary circuit is short-circuited. During interval T_4, load current shifts from D_n to D_p. Figure 7(c) shows the equivalent circuit during interval T_2. During interval T_2, the secondary circuit D_n takes the load current.

2.5. *Interval* T_5 ($t_4 < t < t_5$)

Interval T_5 begins when C_2 is discharged fully. As C_2 is discharged, the magnetizing current and reflected load current forward bias D_2. The magnetizing current and reflected load current (I_{p2}) flow through D_2. When current is flowing through D_2, S_2 and S_4 are turned on. Thus, zero-voltage switching of device S_2 is achieved. This interval is known as ZVS interval. When S_2 is on, D_4 is reverse-biased in the primary circuit. When the primary current direction changes its direction, S_2 takes the current from D_2. At the end of this interval, D_n blocks fully and takes the full load current. The time of interval T_5 is decided by the leakage inductance. Figure 8 shows the conduction path.

2.6. *Interval* T_6 ($t > t_5$)

This interval is known as power transfer interval. During this interval, S_2 and S_4 are on in the primary circuit. D_4 is reverse-biased in the primary circuit and D_p is forward-biased in the

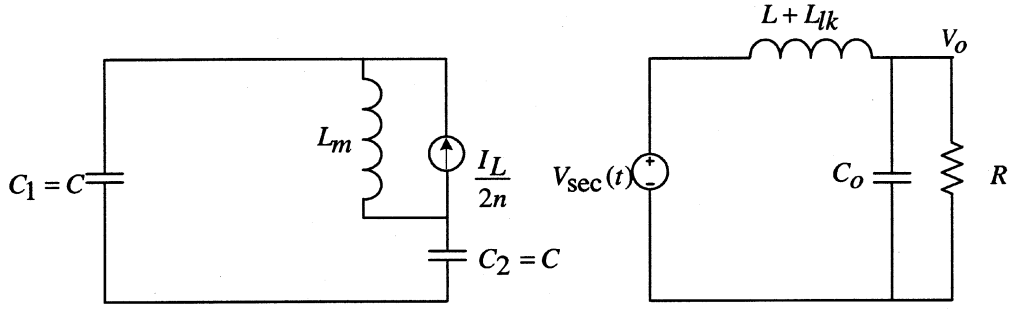

FIG. 7(c). Equivalent circuit for Interval T_2.

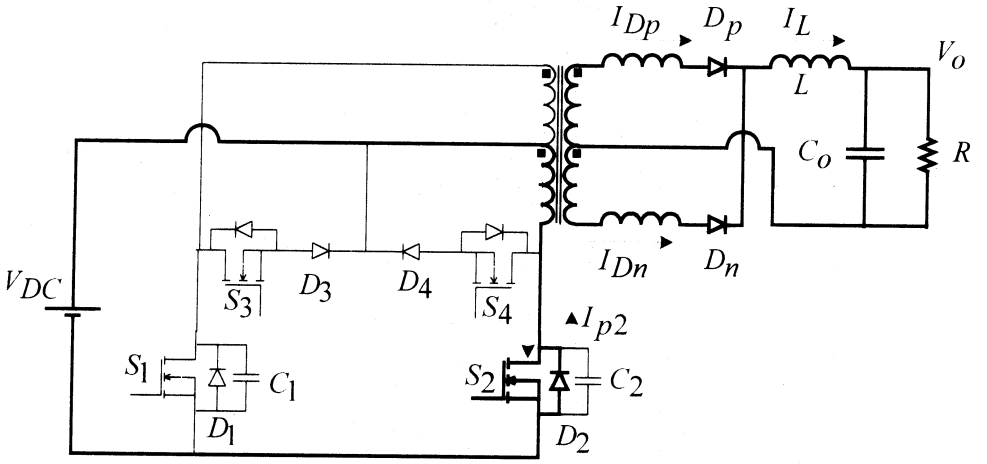

FIG. 8. Conduction path in Interval T_5.

secondary circuit. Figure 9 shows the conduction path. This interval is followed by similar sets of intervals as earlier to achieve ZVS for S_1.

Interval T_6 is the complimentary interval of T_1. Each cycle consists of ten intervals. Currents and voltages at different intervals of the converter are listed in Table I.

3. Designing of ZVS

3.1. *Parameters affecting ZVS*

Various parameters like magnetizing current, leakage inductance of the secondary, leakage inductance of the primary, time delay, load current and device output capacitance affect

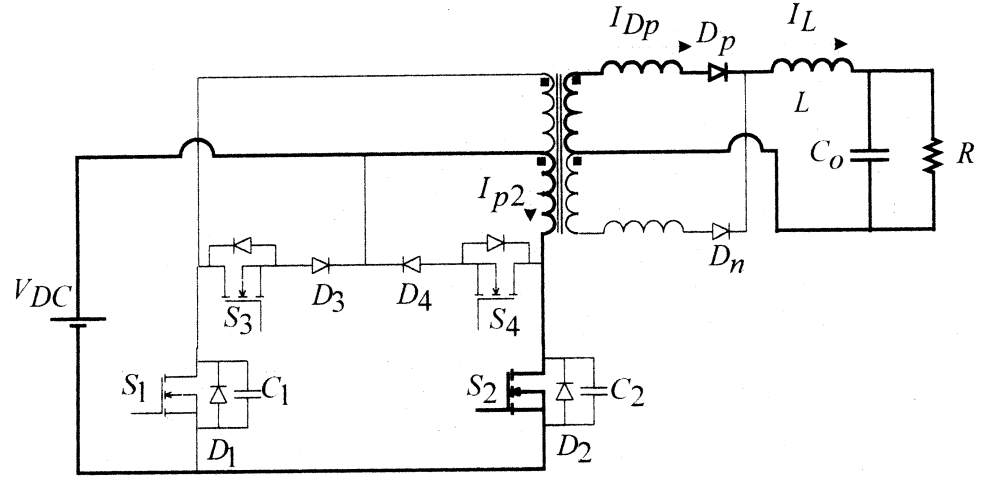

FIG. 9. Conduction path for Interval T_6.

Table I
Voltages and current of zero-voltage switching push–pull converter

Interval	Conducting devices	V_{c1}	V_{c2}	V_{p1}	V_{p2}	I_{Dp}	I_{Dn}	Slope of the Inductor (L) current
T_1	S_1	0	$2V_{DC}$	$-V_{DC}$	$-V_{DC}$	0	I_L	$\left(\frac{1}{L+L_{lk}}\right)\left(\frac{V_{DC}}{n}-V_0\right)$
T_2	C_1, C_2	$V_{c1}(t)$	$V_{c2}(t)$	$V_{c1}(t)-V_{DC}$	$V_{DC}-V_{c2}(t)$	0	I_L	$\left(\frac{1}{L+L_{lk}}\right)\left(\frac{V_{DC}-V_{c1}(t)}{n}-V_0\right)$
T_3	S_3, D_3	V_{DC}	V_{DC}	0	0	0	I_L	$\left(\frac{1}{L+L_{lk}}\right)(-V_0)$
T_4	C_1, C_2	$V_{c1}(t)$	$V_{c2}(t)$	$V_{c1}(t)-V_{DC}$	$V_{DC}-V_{c2}(t)$	$I_L-I_{Dn}(t)$	$I_{Dn}(t)$	$-\frac{V_0}{L}$
T_5	D_2, S_2	$2V_{DC}$	0	V_{DC}	V_{DC}	$I_L-I_{Dn}(t)$	$I_{Dn}(t)$	$-\frac{V_0}{L}$
T_6	S_2	$2V_{DC}$	0	V_{DC}	V_{DC}	I_L	0	$\left(\frac{1}{L+L_{lk}}\right)\left(\frac{V_{DC}}{n}-V_0\right)$
T_7	C_1, C_2	$V_{c1}(t)$	$V_{c2}(t)$	$V_{c1}(t)-V_{DC}$	$V_{DC}-V_{c2}(t)$	I_L	0	$\left(\frac{1}{L+L_{lk}}\right)\left(\frac{V_{DC}-V_{c2}(t)}{n}-V_0\right)$
T_8	S_4, D_4	V_{DC}	V_{DC}	0	0	I_L	0	$\left(\frac{1}{L+L_{lk}}\right)(-V_0)$
T_9	C_1, C_2	$V_{c1}(t)$	$V_{c2}(t)$	$V_{c1}(t)-V_{DC}$	$V_{DC}-V_{c2}(t)$	$I_L-I_{Dn}(t)$	$I_{Dn}(t)$	$-\frac{V_0}{L}$
T_{10}	D_1, S_1	0	$2V_{DC}$	$-V_{DC}$	$-V_{DC}$	$I_L-I_{Dn}(t)$	$I_{Dn}(t)$	$-\frac{V_0}{L}$

ZVS. The choice of the various parameters is a trade-off between switching loss and conduction loss. The following section elaborates on the various parameters affecting ZVS.

3.2. *Magnetizing current*

Magnetizing current aids ZVS and is in the direction of discharge device output and snubber capacitance (Fig. 10). A higher value of magnetizing current is good from the ZVS point of view, but it increases the conduction loss and peak current.

3.3. *Leakage inductance of the secondary side*

Leakage inductance of the secondary side aids ZVS. It also limits the rate of reversal of reflected current in the primary circuit. Higher value of leakage inductance means more energy is available to discharge the device output capacitance and snubber capacitance. But increasing its value decreases the effective duty ratio. Hence utilization of the installed components is less. Further, leakage inductance resonates with junction capacitance of diode and causes severe ringing. Figure 11 shows the secondary voltage current through diode and rectified voltage. It is clear that the effective duty cycle reduces with the increase in leakage inductance.

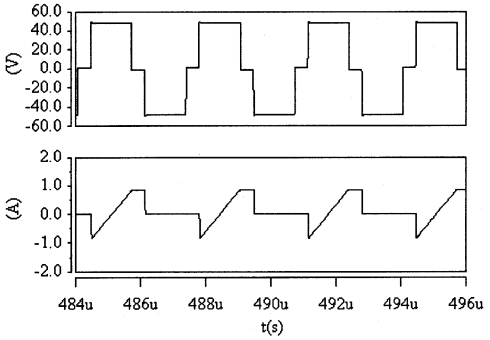

FIG. 10. Voltage across one half of the primary winding and magnetizing current.

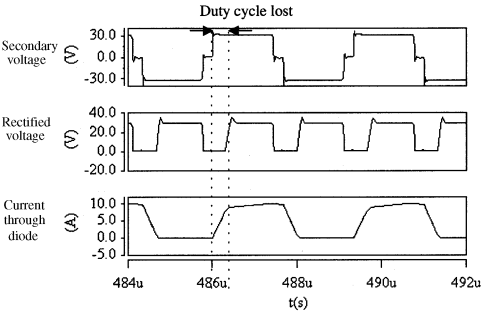

FIG. 11. Simulation waveforms with secondary leakage inductance = 1.2 *m*H.

3.4. *Snubber and device output capacitors*

Snubber capacitance and device output capacitance are together called the effective capacitance. Increasing the value of effective capacitance reduces the turn-off switching loss. Further, it will reduce any voltage spike that is caused during turn-off transition. But higher value of effective capacitance demands more energy to be stored in magnetizing and leakage inductance.

3.5. *Time delay*

Figure 12 shows the voltage across S_2, current through S_2 and current through the effective capacitance C_2 during ZVS instant. The operation of the circuit during ZVS is explained through three sub-intervals, which are referred to as t_1, t_2 and t_3 in Fig. 12. Interval T_4 (resonant transition-II) is the same as the sub-interval t_1. During this sub-interval (t_1), the capacitance (C_2) discharges from V_{DC} to 0. If the switch is turned on during this sub-interval, t_1 results in hard switching. The time of discharge of the capacitor depends only on the reactive elements (leakage inductance and effective capacitance). During the sub-

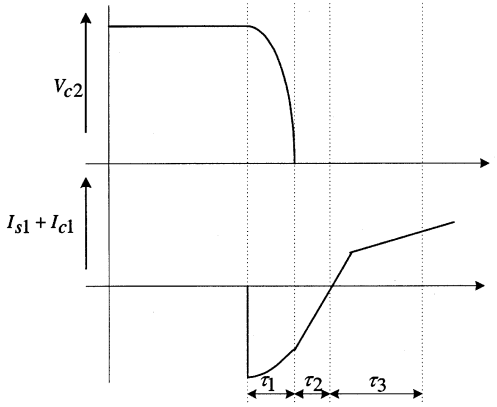

FIG. 12. Idealized waveforms during ZVS.

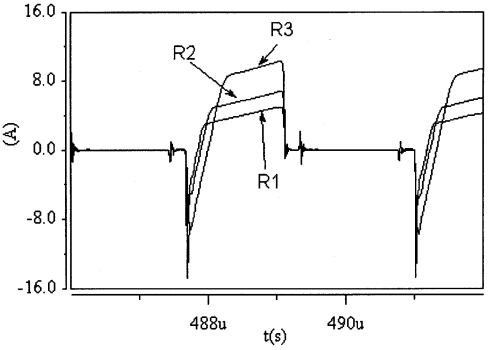

FIG. 13. Switch current during ZVS transition. (for different values of load resistance, $R1 > R2 > R3$).

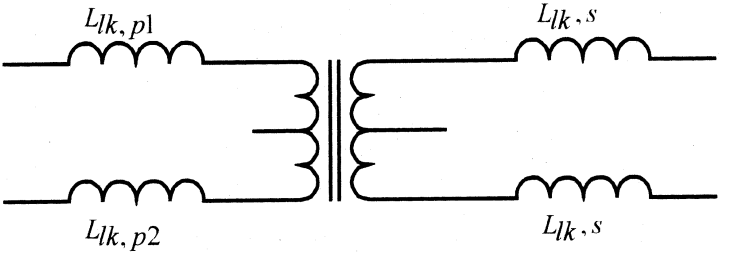

FIG. 14. Leakage inductances of the push–pull transformer.

interval (t_2), the body diode of the switch conducts. As the body diode of the switch is conducting during this sub-interval (t_2) ZVS can be achieved by turning on the switch. The time of the sub-interval (t_2) depends on the reflected current. Higher load current increases the sub-interval t_2. This is shown in Fig. 13 through simulation results. If the switch is not turned on during the sub-interval (t_2), the effective capacitance charges again and results in hard switch. So, the time delay of the circuit should be above t_1 and below (t_1 + t_2).

3.6. *Leakage inductance of the primary*

Figure 14 shows the various leakage inductances in the push–pull transformer. Primary leakage inductances are represented as $L_{lk,p1}$ and $L_{lk.p2}$ and secondary ones as $L_{lk,s}$. During the transition of intervals from T_2 to T_3 and T_4 to T_5, the magnetizing current and reflected current shift their path from full primary winding to one half. So the energy trapped in the primary leakage inductance causes ringing in the waveforms. Snubber circuits need to be used to reduce ringing. It is advantageous to have very low value of primary leakage inductance.

3.7. *Design procedure*

The following two important parameters decide the ZVS:

1. Energy available in leakage (secondary leakage inductance) and magnetizing should be sufficient to discharge the device output and snubber capacitance.
2. Sufficient time delay should be available to discharge the device output capacitance.

Figure 15 shows the equivalent circuit of push–pull converter during interval T_4.

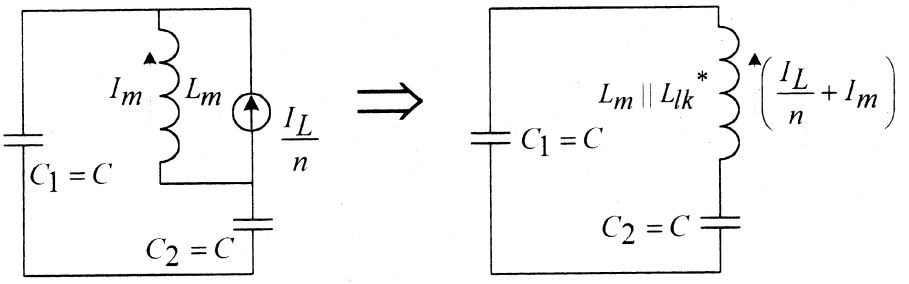

FIG. 15. Equivalent circuit in the primary side during Interval T_4.

The following equations are used to design the leakage inductance, magnetizing inductance and time delay.

Equation 1 gives the condition to achieve ZVS. The condition is,

$$V_{DC} \le i(0)\sqrt{\frac{L}{2C}};\ \ i(0) = I_m + I_{\text{refl}}\,. \tag{1}$$

From eqn (2) the minimum time required to discharge the effective capacitance can be determined.

$$v = \sqrt{\frac{2}{LC}}; \qquad T = p\sqrt{2LC} \ \text{ is the total time period.} \tag{2}$$

$$\therefore \text{ the time taken to discharge the snubber capacitance } T_d = \frac{T}{4} \tag{3}$$

$$\therefore \text{ Minimum time delay} = \frac{p}{2\sqrt{2}}\sqrt{LC}\,. \tag{4}$$

The following steps need to be followed while designing the reactive elements (leakage inductance and snubber capacitor) for ZVS push–pull converter.

Step 1: Based on switching frequency and device characteristics, select the time delay and effective capacitance (output capacitance and snubber capacitance).

Step 2: Calculate L from eqn (4) which is approximately equal to L^*_{lk} because magnetizing inductance L_m is much higher than the leakage inductance.

Step 3: If eqn (1) is not satisfied with the value of the leakage inductance, then magnetizing current has to be increased to satisfy the equation.

3.8. *ZVS limit*

From the above design procedure (eqn 1) it is understood that ZVS is dependent on load and magnetizing currents. At lightly loaded condition, it is difficult to achieve ZVS because the energy stored in the leakage inductance and magnetizing inductance may not be sufficient to discharge the effective capacitance prior to the turn-on of the switch. When the load current is high, the reflected current in the primary is more. So it is easy to achieve ZVS at higher load currents. So, for a wider ZVS range more energy has to be stored in leakage and magnetizing inductance. Wider ZVS range suffers from the disadvantage of higher conduction loss. Hence, selecting the ZVS range is a trade off between conduction and switching losses.

4. Design and development of a 300 kHz/200 W push–pull converter

Based on the design methodology proposed in the paper a prototype of resonant transition push–pull converter has been developed. The following are the *I*/*O* specifications of the power supply:

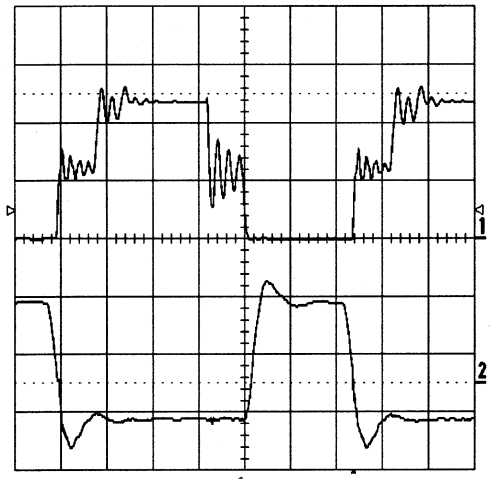

FIG. 16. Voltage across S_1 and control pulse of S_1. (Ch-1–V_{c1} and Ch-2 control pulse of S_1) Scale: V_{c1}–40 V/div, 0.5 *m*s/div, V_{g1}–10 V/div, 0.5 *m*s/div.

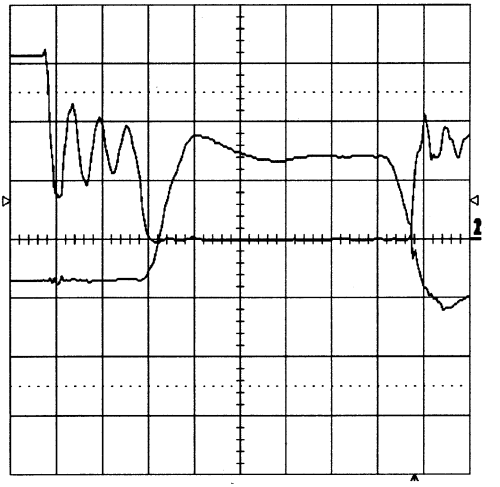

FIG. 17. Voltage across S_1 and control pulse for S_1. (Ch-1–V_{c1} and Ch-2 control pulse for S_1) Scale: V_{c1}–30 V/div, 0.2 *m*s/div, V_{gl}–10 V/div, 0.2 *m*s/div.

Input voltage: 48 V
Output voltage: 20 V
Output power: 200 W
Switching frequency: 300 kHz.

4.1. *Experimental results*

Figure 16 shows the voltage across S_1 and the control pulse for S_1. The leakage inductance between the two primary windings is responsible for the ringing in the V_{c1} (voltage across switch S_1) waveform (Fig. 16). Figure 17 shows the voltage across S_1 and control pulse for S_1 during turn-on. It is clear from the figure that the voltage across the device falls just before applying the control pulses. This indicates the ZVS of the switch S_1 during turn-on. Figure 17 is the expanded time scale of Fig. 16. Figure 18 shows the voltage across S_2 and control pulse of S_2. The leakage inductance between the two primary windings is responsible for the ringing in V_{c2} (voltage across switch S_2) waveform (Fig. 18). Figure 19 shows the voltage across S_2 and control pulse of S_2 during turn-on. The voltage across the device falls just before applying the control pulses. This indicates the ZVS of the switch S_2 during turn-on. Figure 19 is the expanded time scale of Fig. 18. Figure 20 shows the voltage across the synchronous rectifier S_6. Additional inductance, which is added to aid ZVS, oscillates with the junction capacitance of the body diode of S_6. From Fig. 20 it is clear that the peak of the ringing voltage is twice that of the nominal voltage. This is a drawback of the proposed topology.

Rajapandian has proposed a technique [6], in which the energy associated with the ringing is fed back to the source instead of dissipating it in the snubber circuits. Figure 21 shows the voltage across the synchronous rectifier S_5.

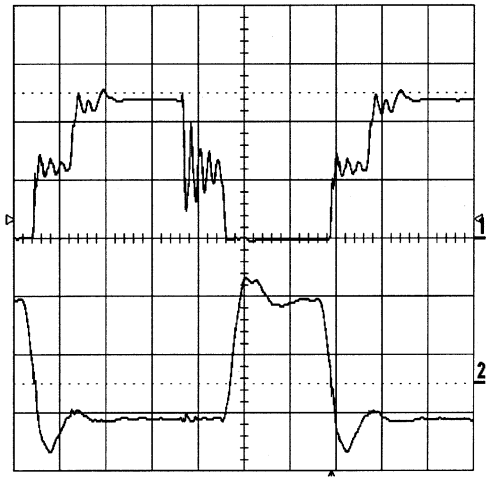

FIG. 18. Control pulses for S_2 and voltage across S_2. (Ch-1–V_{c2} and Ch-2 control pulse of S_2) Scale: V_{c2}–40 V/div, 0.5 *m*s/div, V_{g2}–10 V/div, 0.5 *m*s/div.

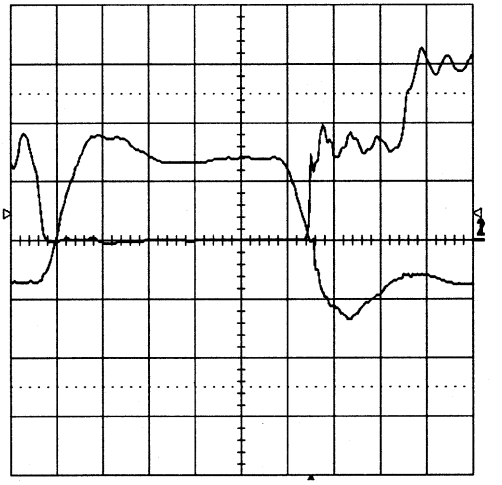

FIG. 19. Voltage across S_2 and control pulse for S_2. (Ch-1–V_{c2} and Ch-2 control pulse of S_2). Scale: V_{c2}–30 V/div, 0.2 *m*s/div, V_{g2}–10 V/div, 0.2 *m*s/div.

5. Dynamic analysis of ZVS push–pull converter

The small signal dynamic model of push–pull converter is similar to PWM hard-switched converter. This is validated by measuring the small signal characteristics of the push–pull converter using frequency response analyzer.

The additional leakage inductances, which are introduced to achieve ZVS, are of small value when compared to the filter inductor. It is assumed that the filter inductor absorbs these leakages inductances. So the converter function remains the same as the hard-switched PWM converter.

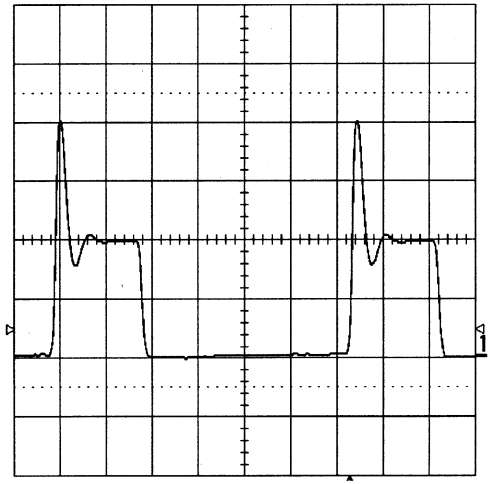

FIG. 20. Voltage across the synchronous rectifier S_6.

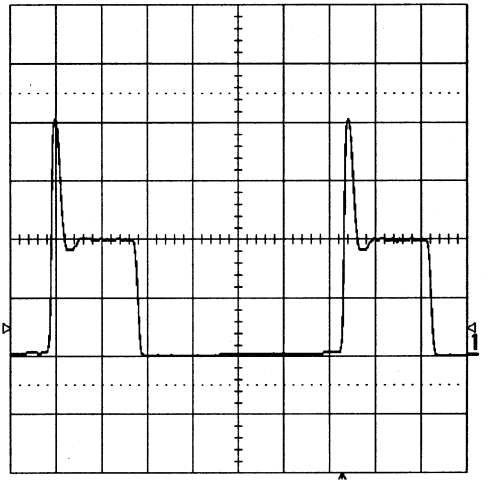

FIG. 21. Voltage across the synchronous rectifier S_5.

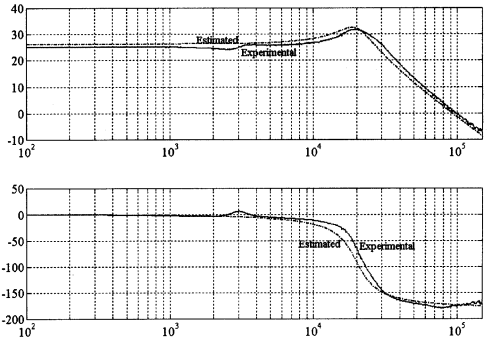

FIG. 22. Control gain characteristic of ZVS push–pull converter.

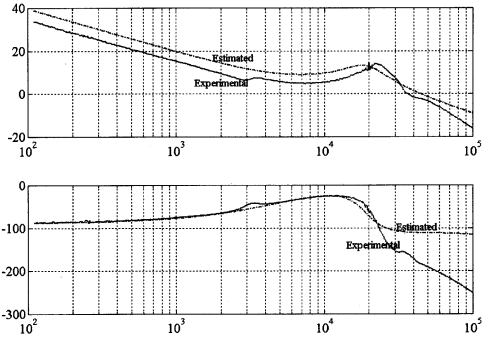

FIG. 23. Measured and estimated loop gain characteristics of push–pull converter.

The control transfer function of the converter is of the form,

$$G(S) = \frac{\hat{V}_0}{\hat{d}} = \frac{2 \times n \times V_{DC}}{s^2 LC + s\frac{L}{R} + 1}(1 + sCR_{ESR}) \tag{5}$$

where L is the filter inductor and leakage inductance, C, the filter capacitor, R, the load resistor, and R_{ESR}, the ESR of the filter capacitor.

Figure 22 shows the measured and estimated control characteristics of the push–pull converter. Figure 23 shows the measured and estimated loop gain of the push–pull converter. The frequency response analyzer used for measuring the loop gain gives reliable measurement up to 30 kHz. The experimental and estimated results almost match in our region of interest.

6. Efficiency plot

As the energy associated with the secondary leakage inductance is more the secondary snubber loss is also greater. By using the Rajapandian technique [6], the secondary snubber loss can be reduced. Figure 24 gives the plot of efficiency vs load current.

Synchronous rectifiers are used in the ZVS push–pull converter to achieve high efficiency. It is interesting to see that the drives for the synchronous rectifier device are practically the same

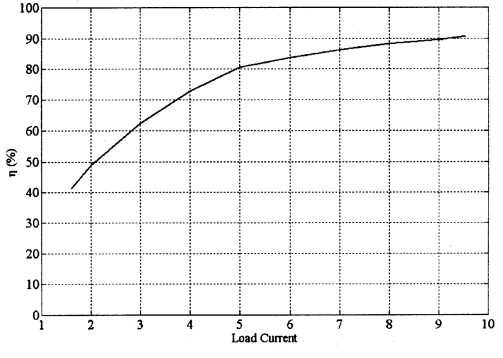

FIG. 24. Efficiency vs load current.

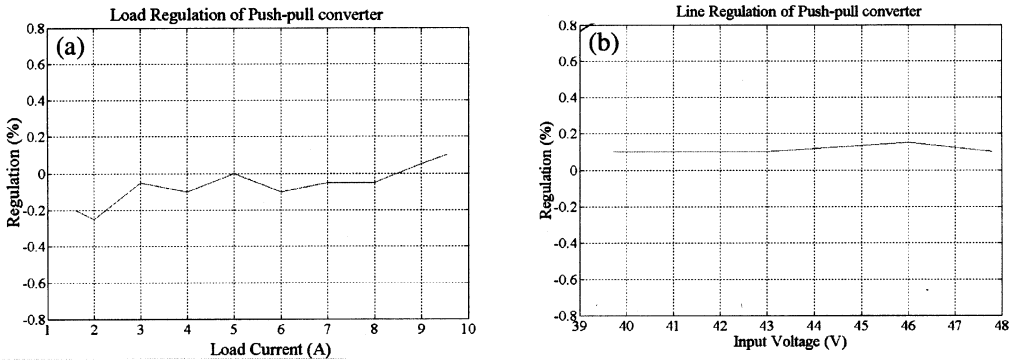

FIG. 25. (a) Load and (b) line regulations of ZVS push–pull converter.

as the additional switches. Line and load regulations of the power supply are within ± 0.2% (Fig. 25). Figure 26 shows the output voltage waveform.

7. Extension to half-bridge converter

This topology can be extended to half-bridge DC-DC converter also. The control technique is the same as the push–pull converter. Figure 27 shows the circuit diagram of the half-bridge converter. As in push–pull converter, two additional switches and two additional diodes are used to achieve ZVS. In push–pull converter, the primary inductance causes ringing the voltage waveforms, whereas in half-bridge converter the primary leakage inductance also aids the ZVS. Hence, the voltage waveforms will be free from ringing.

8. Conclusions

The objective of the paper is to develop an improvised push–pull converter suitable for soft switching. The improvised push–pull converter uses two additional switches and two diodes. The additional switches introduce freewheeling intervals in the circuit and thus enable lossless switching. In classical push–pull converter, the transformer primary is left open

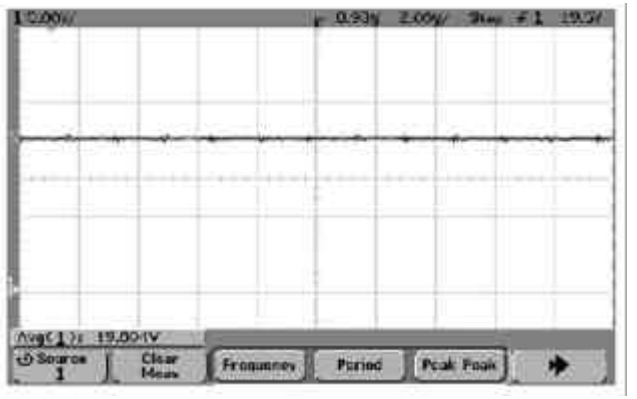

Fig. 26. Output voltage waveform of ZVS push-pull DC converter.

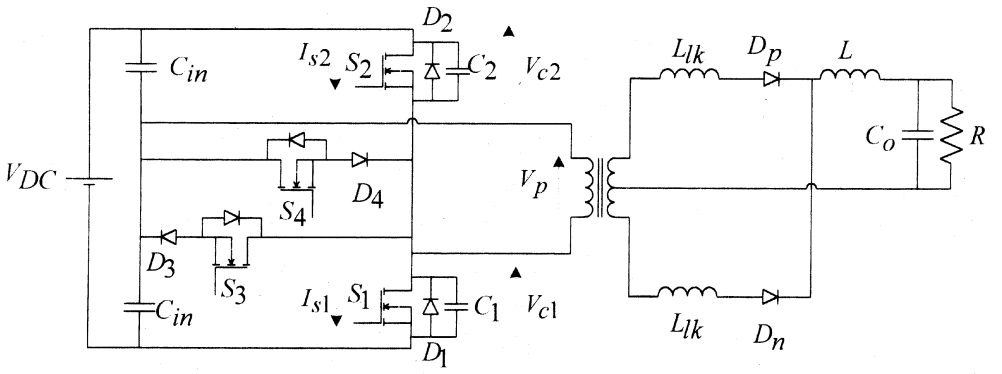

FIG. 27. ZVS half-bridge converter.

during two sub-intervals in a period. On account of this feature, the turn-on of the switch in these converters is always hard. The new circuit topology converts these open circuit intervals into freewheeling intervals with such a modification. All trapped energy in the core is conserved to achieve ZVS during the transition. The following are the features of the new circuit:

1) Loss-less switching transition for all the switches employed.
2) Switch stress similar to hard-switched PWM converter.
3) Control and small signal behavior similar to hard-switched PWM converter.
4) ZVS range of the converter is dependent on the load current. In order to have wider range of ZVS, additional inductance is added to the secondary of the transformer. The inductance that is added to aid ZVS resonates with the junction capacitance of the diode and produces ringing in the secondary voltage waveforms. This is a drawback of this topology.

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