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A Novel Reversible Full Adder Circuit for Nanotechnology Based Systems

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Abstract: Reversible computation is of major interest in low power design and nanotechnology-based systems. A reversible logic gate has the same number of inputs and outputs and a one-to-one correspondence between the inputs and the outputs. In this study, we propose a new 4*4 reversible logic gate, MKG. The MKG gate can be used to implement all Boolean functions. It also can be used to design efficient adders. One of the prominent functionalities of the MKG gate is that it can work singly as a reversible full adder unit, which is a versatile and widely used element in digital design. Thus, the proposed reversible full adder contains only one gate. It is shown that the proposed reversible full adder is better and optimized in terms of number of reversible gates, number of garbage outputs and number of constant inputs with compared to the existing counterparts.

Key words: Reversible logic, reversible gate, reversible full adder, reversible computing, quantum computing

INTRODUCTION

Conventional logic is irreversible. Irreversible circuits unavoidably generate heat due to information loss during the computation. R. Landauer has proved that the amount of energy (heat) dissipated for every irreversible bit operation is at least KTln2 joules, where $K = 1.3806505*10^{-23}\ m^2\ kg^{-2}\ K^{-1}$ (joule $Kelvin^{-1}$) is the Boltzmann constant and T is the temperature in degrees Kelvin (Landauer, 1961; Parhami, 2006). For room temperature T the amount of energy dissipated is small (i.e., $3*10^{-21}$) but it is not negligible (Chowdhury *et al*., 2006). In 1973, Bennett proved that KTln2 energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs (Bennett, 1973; Hayes, 2006). Reversible logic allows the reproduction of the inputs from the outputs. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. Thus, reversible logic circuit allows computation with arbitrarily small energy dissipation. Reversible logic gates do not loose information. In addition, reversible logic gates have the same number of inputs and outputs and a one-to-one correspondence between input and output vectors. We can always uniquely determine the input vectors from the output vectors. Furthermore, reversible logic circuits are of major interest in optical computing, low power CMOS design, quantum computing and nanotechnology based systems. It is not possible to realize quantum computing without reversible logic. All gates in a reversible logic circuit must be reversible (Vasudevan *et al*., 2004; Gu *et al*., 2005). Neither feedback nor fan-out is allowed in reversible logic circuits (Parhami, 2006; Perkowski *et al*., 2001). Consequently, synthesis of reversible logic circuits is different from irreversible logic synthesis.

A reversible logic circuit using reversible logic gates should have the following features (Perkowski and Kerntopf, 2001):

- Use minimum number of reversible logic gates
- Use minimum number of garbage outputs
- Keep the length of cascading gates minimum
- Use minimum input constants

The output that is not used for further computations is called garbage output (Thapliyal and Srinivas, 2005). The word constant-input refers to the inputs that were added to an n*k function to make it reversible (Saiful Islam and Rafiqul Islam, 2005).

In this research, a new reversible logic gate, MKG is introduced. We demonstrate that a versatile and widely used element, the full adder circuit, can be built with only one MKG gate. The proposed reversible full adder is then compared with the existing reversible full adders. It is shown that the proposed reversible full adder is better than the existing counterparts.

MATERIALS AND METHODS

Basic reversible logic gates: A set of reversible logic gates is needed to design reversible logic circuits. An N*N reversible logic gate can be represented as:

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$$I_V = (I_1, I_2, I_3, \ldots, I_N)$$
$$O_V = (O_1, O_2, O_3, \ldots, O_N)$$

Where, I_V and O_V are input and output vectors. Several reversible logic gates have been proposed. Among them are Feynman Gate (FG) (Feynman, 1985), Toffoli Gate (TG) (Toffoli, 1980), Fredkin Gate (FRG) (Fredkin and Toffoli, 1982), New Gate (NG) (Azad Khan, 2002) and New Toffoli Gate (NTG) (Peres, 1985; Hasan Babu *et al*., 2003a).

One of the most important reversible logic gates is the Feynman Gate, also known as controlled NOT Gate (1-CNOT). Logically, the Feynman Gate can be described by the equations: P = B and Q = A⊕B, where A is control bit and B is the data bit. A 2*2 Feynman Gate is shown in Fig. 1. Input variables are A and B, output variables are P and Q.

Feynman Gate is the most suitable gate for a single copy of a bit. A 0 in the second input will copy the first input in both outputs of the gate (Fig. 2). Thus, Feynman Gate is suitable for single copy of bit since it is not producing any garbage output (Hasan Babu and Chowdhury, 2005).

A 3-input, 3-output Toffoli Gate, also known as controlled-NOT (CCNOT) is shown in Fig. 3. It implements the logic functions: P = A, Q = B and R = AB⊕C. A 3*3 Toffoli Gate has two control inputs, which are copied to the first and second outputs. It has one other input that is complemented if all control inputs are 1 s and is directly copied to the third output otherwise (Parhami, 2006).

A 3-input, 3-output Fredkin Gate is shown in Fig. 4, respectively. It can be represented as:

$$I_V = (A, B, C)$$
$$O_V = (P = A, Q = A'B \oplus AC, R = A'C \oplus AB)$$

Where, I_V and O_V are input and output vectors. A 3*3 Fredkin Gate, also known as controlled permutation gate has one control input that is copied to the first output. The second and third inputs are directly copied to the outputs if the control input is 0 and are swapped otherwise. Fredkin Gate is a conservative gate, that is, the Hamming weight of its input is the same as the Hamming weight of its output.

A 3-input, 3-output New Gate (NG) is shown in Fig. 5, respectively. It can be represented as:

$$I_v = (A, B, C)$$
$$O_v = (P = A, Q = AB \oplus C, R = A'C' \oplus B')$$

Where, I_v and O_v are the input and output vectors.

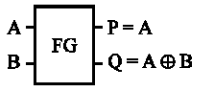

Fig. 1: Feynman gate

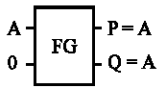

Fig. 2: FG gate as copying output

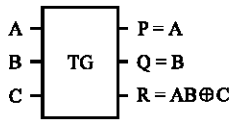

Fig. 3: Toffoli gate

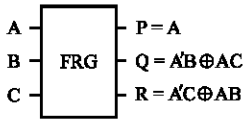

Fig. 4: Fredkin gate

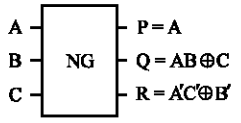

Fig. 5: New gate

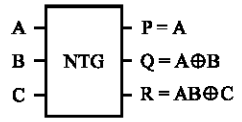

Fig. 6: New Toffoli gate

A 3-input, 3-output Peres Gate (PG), also known as New Toffoli Gate (NTG), combining Toffoli Gate and Feynman Gate is shown in Fig. 6, respectively. It can be represented as:

$$I_v = (A, B, C)$$
$$O_v = (P = A, Q = A \oplus B, R = AB \oplus C)$$

Where, I_v and O_v are the input and output vectors. NTG gate does the transformation produced by a Toffoli Gate followed by a Feynman Gate.

Table 1: Truth table of the proposed reversible MKG gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	1	0
0	1	0	1	0	0	0	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	1	1
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	0

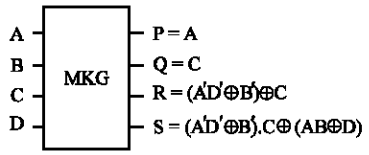

Fig. 7: Proposed reversible MKG gate

New 4*4 reversible logic gate: This study proposes a new reversible logic gate, MKG. The proposed MKG gate is shown in Fig. 7, respectively. Gate width of the proposed MKG gate is four. In the other words, MKG is a 4-input, 4-output reversible logic gate. The MKG gate can be represented as:

$$I_v = (A, B, C, D)$$
$$O_v = (P = A, Q = C, R = (A'D' \oplus B') \oplus C$$
$$S = (A'D' \oplus B').C \oplus (AB \oplus D))$$

Where, I_v and O_v are the input and output vectors. The corresponding truth table of the MKG gate is depicted in Table 1, respectively. It can be verified from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined.

The MKG gate is a two-through gate, which means that two of the input variables are also outputs. MKG gate can be used for implementing arbitrary functions. It can implement all Boolean functions. The NAND and the NOT functions can be simultaneously implemented on MKG (Fig. 8a). The NOR function can be obtained as shown in Fig. 8b. The EX-OR function and the AND function can be implemented as shown in Fig. 8c. The EX-NOR function can be implemented as depicted in Fig. 8d. The implementation of the MKG gate as OR function is shown in Fig. 8e.

New reversible full adder circuit: A versatile arithmetic building element, the full adder, can be built using only one reversible MKG gate. Before the discussion of the proposed reversible full adder circuit, consider the logical expressions for each output of a full adder:

Table 2: Truth table of full adder circuit

Inputs			Outputs	
A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

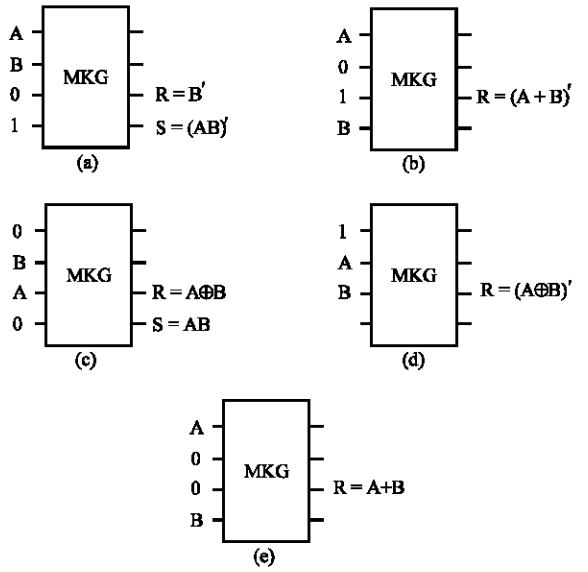

Fig. 8: Proposed MKG gate can implement all Boolean functions. (a) NAND and NOT gates, (b) NOR gate, (c) XOR and AND gates, (d) XNOR gate and (e) OR gate

$$Sum = A \oplus B \oplus C$$
$$C_{out} = (A \oplus B).C_{in} \oplus AB$$

The corresponding truth table of a full adder is shown in Table 2, respectively.

Several researchers have proposed reversible full adder circuits (Azad Khan, 2002; Bruce *et al*., 2002; Khlopotine *et al*., 2002; Hasan Babu *et al*., 2003a, 2004; Thapliyal and Srinivas, 2005; Saiful Islam and Rafiqul Islam, 2005). One of the prominent functionalities of the MKG gate is that it can work singly as a reversible full adder unit. If $I_v = (A, B, C_{in}, 0)$, then the output vector becomes: $O_v = (P = A, Q = C_{in}, R = Sum, S = C_{out})$. Thus, we have both of the required outputs. Implementation

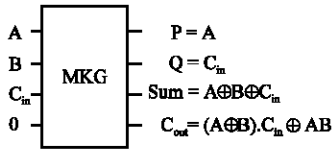

Fig. 9: Proposed MKG gate as reversible full adder

of the proposed MKG gate as the reversible full adder is shown in Fig. 9, respectively. The proposed reversible full adder circuit uses only one reversible logic gate. It produces only two garbage outputs. It requires only one constant input and it needs only one clock cycle to perform the operations.

RESULTS AND DISCUSSION

The proposed reversible full adder circuit performs better than the existing counterparts. An experimental result will comprehend it clearly. Table 3 compares our proposed reversible full adder circuit with the existing full adder designs.

One of the major constraints in reversible logic is to minimize the number of reversible gates used. In this study we used only one reversible logic gate, so we can state that the proposed reversible full adder circuit is optimal in terms of number of reversible logic gates.

Another significant criterion in designing a reversible full adder is to lessen number of garbage outputs. Every output of the gate that is not used as a primary output or as input to other gate is called garbage output. A heavy price is paid for every garbage bit. It has been proved that a reversible full-adder circuit requires at least two garbage outputs to make the output combinations unique, which is the primary condition for a reversible circuit (Hasan Babu *et al*., 2003b). The proposed reversible full adder circuit produces two garbage outputs, so it is optimal in term of number of garbage outputs.

Another important parameter is to lessen number of constant inputs. The word constant-input refers to the inputs that were added to an n*k function to make it reversible. It has been proved that a reversible full adder requires at least one constant input (Saiful Islam and Rafiqul Islam, 2005). Our proposed reversible full adder circuit requires only one constant input, so it is optimal in term of number of constant inputs.

This work requires only one clock cycle, so we can state that it is also optimal in term of required clock cycles, which is one of the main factors of a circuit.

Only one of the existing circuits (Thapliyal and Srinivas, 2005) has all these optimal properties similar to our proposed full adder circuit (Table 3). Our proposed circuit is better than (Thapliyal and Srinivas, 2005) in term of hardware complexity.

Thus, the propounded reversible full adder requires less logical calculations than (Thapliyal and Srinivas, 2005), keeping other properties constant. So, Our proposed circuit is better than the full adder circuit presented in (Thapliyal and Srinivas, 2005).

The reversible full adder circuit in (Azad Khan, 2002) requires three reversible gates (two 3*3 New Gates and one 2*2 Feynman Gate) and produces three garbage outputs. It requires two constant inputs and three clock cycles. Its total logical calculation is T = 5α+4β+6δ. The design in (Bruce *et al*., 2002) requires four reversible Fredkin Gates and produces three garbage outputs. It requires two constant inputs and four clock cycles. Its total logical calculation is T = 8α+16β+4δ. The proposed full adder using MKG in Fig. 9 requires only one reversible gate (one MKG gate) and produces only two garbage outputs. It requires only one constant input and one clock cycle. Its total logical calculation is T = 5α+3β+3δ. Thus, our proposed full adder design is also better than the previous full adder designs of (Azad Khan, 2002; Bruce *et al*., 2002) in all the terms.

Table 3: Comparative experimental results of different reversible full adder circuits

				Hardware complexity	
Full adder composition	No. of gate	No. of garbage output	No. of constant input	Total clock cycle	Total logical calculation
Present study	1	2	1	1σ	5α+3β+3δ
Existing circuit (Saiful Islam and Rafiqul Islam, 2005)	2	2	1	2σ	4α+2β
Existing circuit (Thapliyal and Srinivas, 2005)	1	2	1	1σ	6α+3β+3δ
Existing circuit (Hasan Babu *et al*., 2003a)	2	2	1	2σ	4α+3β+3δ
Existing circuit (Hasan Babu *et al*., 2003b, 2004)	3	2	1	3σ	4α+3β+3δ
Existing circuit (Azad Khan, 2002)	3	3	2	3σ	5α+4β+6δ
Existing circuit (Bruce *et al*., 2002)	4	3	2	4σ	8α+16β+4δ
Existing circuit (Perkowski *et al*., 2001; Khlopotine *et al*., 2002)	4	2	1	4σ	4α+2β

σ = Unit Clock Cycle, α = A two input EX-OR gate calculation, β = A two input AND gate calculation, δ = A NOT calculation, T = Total logical calculation, So, for (Thapliyal and Srinivas, 2005): T = 6α+3β+3δ, For our proposed full adder circuit: T = 5α+3β+3δ

The design in (Saiful Islam and Rafiqul Islam, 2005) requires two reversible Perse Gates and produces two garbage outputs. It requires one constant input and two clock cycles. Its total logical calculation is T = $4\alpha+2\beta$. The design in (Hasan Babu *et al*., 2003a) requires two reversible gates (one 3*3 New Gate and one 3*3 New Toffoli Gate) and produces two garbage outputs. It requires one constant input and two clock cycles. Its total logical calculation is T = $4\alpha+3\beta+3\delta$. The reversible full adder circuit in (Hasan Babu *et al*., 2003b) requires three reversible gates (one 3*3 New Gate, one 3*3 Toffoli Gate and one 2*2 Feynman Gate) and produces two garbage outputs. It requires one constant input and three clock cycles. Its total logical calculation is T = $4\alpha+3\beta+3\delta$. The design in (Khlopotine *et al*., 2002) requires four reversible gates (two 3*3 Toffoli Gates and two 2*2 Feynman Gates) and produces two garbage outputs. It requires one constant input and four clock cycles. Its total logical calculation is T = $4\alpha+2\beta$. Thus, the proposed reversible full adder using MKG in Fig. 9 requires less gates and clock cycles than (Saiful Islam and Rafiqul Islam, 2005; Hasan Babu *et al*., 2003a, 2004; Khlopotine *et al*., 2002), though it requires a few more logical calculations. Those extra logical calculations do not hamper on a circuit since the extra logical calculations occurs in parallel with other logical calculations. The full adder circuits presented by Saiful Islam and Rafiqul Islam (2005) Hasan Babu *et al*. (2003a, 2004) and Khlopotine *et al*. (2002) are not optimal in terms of number of gates and required clock cycles, but our propounded reversible full adder circuit is optimal. Hence, the new reversible full adder design using MKG gate is also better than the existing designs of Saiful Islam and Rafiqul Islam (2005) Hasan Babu *et al*. (2003a, 2004) and Khlopotine *et al*. (2002).

Thus, we can state that the proposed reversible full adder circuit is better than all the existing counterparts and it has the desirable properties.

CONCLUSION

In this study, we proposed a novel 4*4 reversible logic gate called MKG. It can implement all Boolean functions. It also can be used to design efficient adders. We also have designed a new reversible full-adder circuit that requires only one reversible MKG gate and produces two garbage outputs. Table 3 shows that the proposed reversible full adder is better than the previous reversible full adders. The proposed reversible full adder circuit using MKG gate can be used for designing large reversible systems, which is the necessary requirement of nanotechnology based systems and quantum computers, because quantum computers must be built from reversible components.

REFERENCES

Azad Khan, M.D.M.H., 2002. Design of full adder with reversible gate. International Conference on Computer and Information Technology, Dhaka, Bangladesh, pp: 515-519.

Bennett, C.H., 1973. Logical reversibility of computation. IBM J. Res. Dev., 17: 525-532.

Bruce, J.W., M.A. Thornton, L. Shivakumariah, P.S. Kokate and X. Li, 2002. Efficient adder circuits based on a conservative logic gate. Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI 02), April, Pittsburgh, PA, USA., pp: 83-88.

Chowdhury, A.R., R. Nazmul and H.M.D. Hasan Babu, 2006. A new approach to synthesize multiple output functions using reversible programmable logic array. Proceeding 19th International Conference on VLSI Design (VLSID), 3 (7): 311-316.

Feynman, R., 1985. Quantum mechanical computers. Optics News, 11: 11-20.

Fredkin, E. and T. Toffoli, 1982. Conservative logic. Int. J. Theor. Phys., 21: 219-253.

GU, M., G. Yang, X. Song and J. Sun, 2005. On synthesis of 3*3 reversible logic functions. Int. J. Comput. Math., 82 (4): 385-390.

Hasan Babu, H.M.D., M.D. Rafiqul Islam, A.R. Chowdhury and S.M.A. Chowdhury, 2003a. On the realization of reversible full adder circuit. International Conference on Computer and Information Technology, Dhaka, Bangladesh, 2: 880-883.

Hasan Babu, H.M.D., M.D. Rafiqul Islam, S.M.A. Chowdhury and A.R. Chowdhury, 2003b. Reversible logic synthesis for minimization of full adder circuit. Proceeding of the EuroMicro Symposium on Digital System Design (DSD), Belek Antalya, Turkey, pp: 50-54.

Hasan Babu, H.M.D., M.D. Rafiqul Islam, S.M.A. Chowdhury and A.R. Chowdhury, 2004. Synthesis of full adder circuit using reversible logic. Proceedings 17th International Conference on VLSI Design (VLSI Design), Mumbai, India, pp: 757-760.

Hasan Babu, H.M.D. and A.R. Chowdhury, 2005. Design of a reversible binary coded decimal adder by using reversible 4-bit parallel adder. VLSI Design, Kolkata, India, pp: 255-260.

Hayes, B., 2006. Reverse engineering. Am. Sci., 94 (2): 107-111.

Khlopotine, A., M. Perkowski and P. Kerntopf, 2002. Reversible logic synthesis by gate composition. Proceedings of IWLS, pp: 261-266.

Landauer, R., 1961. Irreversibility and heat generation in the computing process. IBM J. Res. Dev., 5 (3): 183-191.

Parhami, B., 2006. Fault tolerant reversible circuits. Proceeding 40th Asilomar Conference Signals, Systems and Computers, October, Pacific Grove, CA, pp: 1726-1729.

Peres, A., 1985. Reversible logic and quantum computers. Phy. Rev., A 32: 3266-3276.

Perkowski, M., A. Al-Rabadi, P. Kerntopf, A. Buller, M. Chrzanowska-Jeske, A. Mishchenko, M. Azad Khan, A. Coppola, S. Yanushkevich, V. Shmerko and L. Jozwiak, 2001. A general decomposition for reversible logic. Proc. RM, Starkville, pp: 119-138.

Perkowski, M. and P. Kerntopf, 2001. Reversible logic. Invited tutorial. Proc. EURO-MICRO, Sep, Warsaw, Poland.

Saiful Islam, M.D. and M.D. Rafiqul Islam, 2005. Minimization of reversible adder circuits. Asian J. Inform. Technol., 4 (12): 1146-1151.

Thapliyal, H. and M.B. Srinivas, 2005. Novel reversible TSG gate and its application for designing reversible carry look ahead adder and other adder architectures. Proceedings of the 10th Asia-Pacific Computer Systems Architecture Conference (ACSAC). Lecture Notes of Computer Science, Springer-Verlag, 3740: 775-786.

Toffoli, T., 1980. Reversible computing. Tech. Memo MIT/LCS/TM-151, MIT Lab. Comput. Sci.

Vasudevan, D.P., P.K. Lala and J.P. Parkerson, 2004. Online testable reversible logic circuit design using NAND blocks. Proceeding Symposium on Defect and Fault Tolerance, pp: 324-331.