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Research Article

A Novel Scan Architecture for Low Power Scan-Based Testing

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Test power has been turned to a bottleneck for test considerations as the excessive power dissipation has serious negative effects on chip reliability. In scan-based designs, rippling transitions caused by test patterns shifting along the scan chain not only elevate power consumption but also introduce spurious switching activities in the combinational logic. In this paper, we propose a novel area-efficient gating scan architecture that offers an integrated solution for reducing total average power in both scan cells and combinational part during shift mode. In the proposed gating scan structure, conventional master/slave scan flip-flop has been modified into a new gating scan cell augmented with state preserving and gating logic that enables average power reduction in combinational logic during shift mode. The new gating scan cells also mitigate the number of transitions during shift and capture cycles. Thus, it contributes to average power reduction inside the scan cell during scan shifting with low impact on peak power during capture cycle. Simulation results have shown that the proposed gating scan cell saves 28.17% total average power compared to conventional scan cell that has no gating logic and up to 44.79% compared to one of the most common existing gating architectures.

1. Introduction

Nowadays, design-for-testability (DFT) techniques have become an inseparable consideration for testing modern microelectronic designs as they play an important role in the improvement of the test quality and reducing the test application time in the VLSI digital circuits. The next generation of deep submicron circuits will rely not only on the low power VLSI design but also on the DFT methods targeting low power testing.

Full scan design has become one of the most popular structured DFT methods and is widely used in testing of sequential circuit since it has solved the difficulties in control and observation of the internal nodes of circuit by providing external access to all storage elements of the design. However, from the view point of power dissipation, scan-based architectures are very expensive as each scan test pattern contributes to a shift operation with high power consumption [1]. Moreover, since there is less correlation among scan test patterns generated by an Automatic Test Pattern Generation (ATPG) tool compared to the data during normal mode, high switching activities incurred in capture mode have increased test power drastically over chip power limitations. The elevated power consumption during test application can cause severe problems in the Circuit-Under-Test (CUT). The problem of excessive power consumption during test application can mainly fall into two subproblems: (1) excessive average power consumption and (2) excessive peak power consumption.

Problems due to Excessive Average Power Consumption. Average power consumption is the total distribution of power over time period and is calculated using the ratio of consumed energy to test time [1]. This excessive average power consumption due to testing, in the first place, produces extra heat in CUT which has inevitable role in appearing hot spots, circuit premature destruction, degradation of performance, functional failures, and, as a result, circuit reliability degradation. The main mechanisms which lead to these structural degradations are *corrosion* (oxidizing of conductors), *electromigration* (molecular migration of the conductor structure toward the electronic flow), *hot-carrier-induced* defects, or *dielectric breakdown* (loss of insulation of the dielectric barrier) [2]. Excessive average power affects not

only temperature increase but also temperature variations. These temperature variations may induce timing variations during test and, in some cases, may lead to test-induced yield loss [3]. In addition, intensive heat generated by high switching activity during the test process has negative influences on the circuit packaging cost to make the CUT tolerable to higher level temperature.

Problems due to Excessive Peak Power Consumption. Peak power is the highest power value at any given time instant [1]. Often, the time window to define peak power is restricted to one clock period. However, in practice, it was outlined in [1] that restricting the time window to just one clock cycle is not realistic enough since the power consumption within one clock cycle may not be large enough to elevate the temperature over the thermal capacity limit of the chip. As pointed in [3, 4], excessive peak power dissipation comes with a high instantaneous current demand due to *high switching activity* during test application time which may cause power supply noise (PSN). The excessive noise may induce several phenomena as outlined below.

(1) Changing the logic value at some internal nodes of the circuit leads to failing of good dies and consequently unnecessary yield loss.

(2) Ground bounce or voltage droop: by increasing switching activities during test time, voltage glitches may be observed at some signal lines which can change rise/fall time of the gates (timing performance degradation) causing good dies to be declared "fail." Thus, unwanted yield loss happens.

(3) IR-drop is referred to decrease (increase) in the power (ground) rail voltage and is linked to the existence of a nonnegligible resistance between the rail and each node in the CUT.

(4) Cross talk is referred to capacitive coupling between neighboring nets within an IC. By increasing PSN, the voltage at some gates in the circuit is reduced (voltage drop) causing these gate to show higher delays (performance degradation), possibly leading to test fail and yield loss.

Therefore, reducing the switching activities at any instant time mitigates the average power and hence the peak power of the chip [5]. Moreover, peak power and average power reduction during test contribute to enhanced reliability of the test and improvement of yield [6].

For scan-based design, test power concerns include shift power reduction and capture power. Shift power consumption is due to the transitions occurring in scan cells when the adjacent bits in test vector have different values. These transitions not only cause switching activity in scan cells but they are also propagated to the combinational logic through scan cells outputs. Capture power consumption is referred to transitions that happen within scan cells when they have different values before and after capture. However, in some literatures, transitions in combinational part in launch cycles also have been considered as capture power. In general, average power reduction can be accomplished via shift power reduction while peak power reduction can be achieved by reducing capture power since the logic values in many scan cells changes simultaneously during this mode. In scan-based testing, the major portion of the power and energy is dissipated during shift process as reported in [7] since a large portion of the test application time includes shift cycles especially for large industrial designs with long scan chains. So, in our research we have mainly focused on the problem of shift power reduction while capture power also has been taken into account. Although power issue is one of the major concerns in testing of modern VLSI circuits, other parameters such as test application time, area overhead, and fault coverage should not be ignored.

The remainder of the paper is organized as follows. In Section 2, the existing related methods for reducing switching activity in combinational logic and scan chain are reviewed. Section 3 elaborates the proposed gating scan architecture. Simulation results have been presented in Section 4. Finally, Section 5 draws the conclusion.

2. Previous Works

For scan-based designs in particular, there are two sources of power consumption during shift mode. The switching activities happen in the scan chain caused by scan-ripple and the switching activities in the combinational logic due to propagation of rippling transitions in the scan chain. Switching activity in the combinational part contributes to a large portion of the total switching activity in the circuit [11]. One of the most straight-forward ways for shift power reduction is to reduce switching activity in the combinational logic by isolating stimulus path of scan cells from combinational logic during shift cycle because the major source of dynamic power in CUT is the propagation of ripple transitions from the scan cells to the combinational logic during scan shifting. Some authors [7, 12] have tried to gate the stimulus paths of flip-flops to a constant logic "1" or "0" by utilizing gating logic (NOR [7], transmission gate (TG) together with a pull-up or a pull-down transistor [12]) at the scan cells output, thus eliminating spurious switching in logic gates. However, they are able to block only one transient (from "1" to "0" or vice versa) at the first level of the combinational circuit when the circuit mode changes from normal/capture to shift mode. Thus, the unblocked transient still can propagate to the deeper level of the combinational logic, causing many transitions at circuit internal lines before reaching the steady state. Other approaches [13, 14] have experimented the gating logic (MUX [13], extra inverter-base latch [14]) to hold the scan output at the previous logic and completely block any redundant switching activity in the combinational logic during shift mode. An enhanced scan structure has been reported in [11] for delay fault testing. In this method, each scan cell has been augmented into an AND-NOR-based hold latch at the scan cell output to ensure that the scan stimulus paths remain unchanged during shift session. The hold latch has been implemented by a cross-coupled gate of NOR and two AND gates to hold the scan cells' stimulus paths. However, these approaches suffer from large overhead in terms of area and propagation delay.

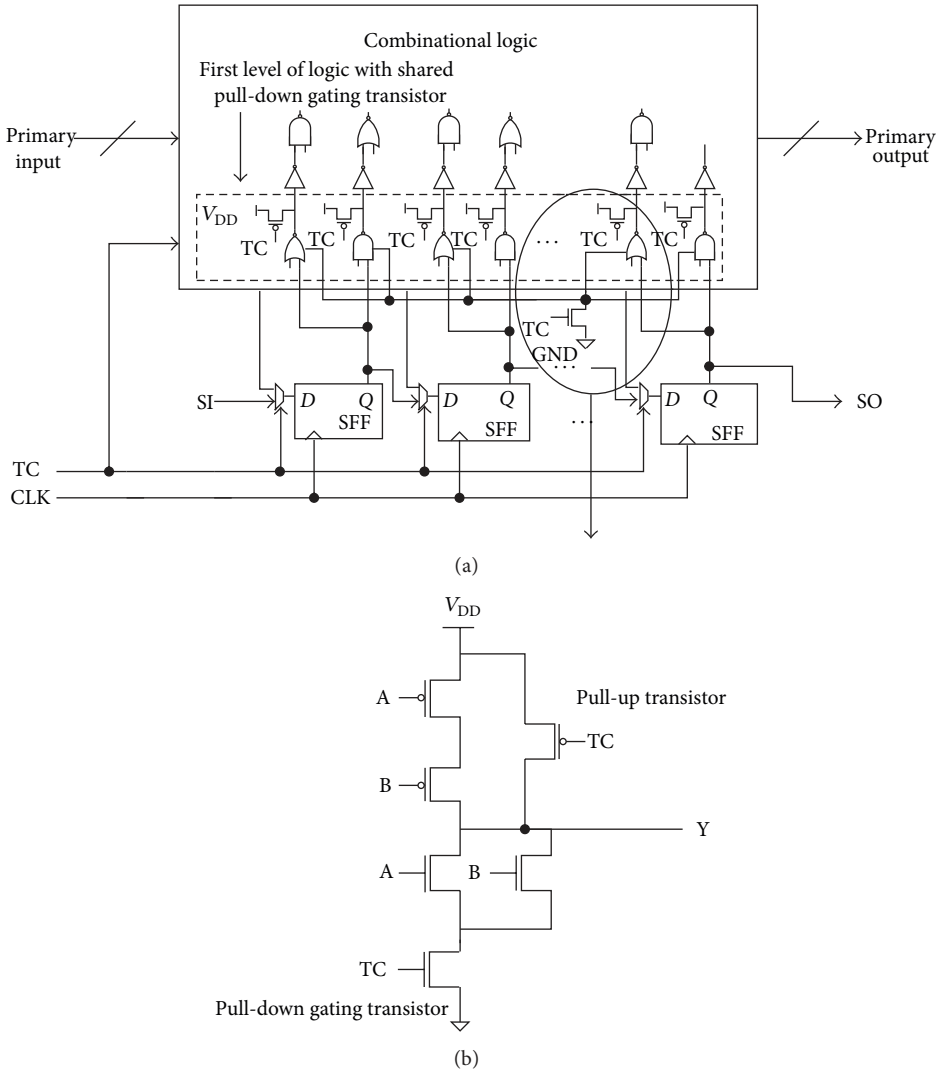

Figure 1: (a) FLS structure [8] and (b) transistor level schema of first level gating in FLS.

The first level supply (FLS) gating scheme proposed by Bhunia et al. [8] has inserted a common pull-down gating transistor to the gates at the first level of logic which are typically connected to the scan chain outputs. In order to prevent the outputs of the first level gates from being floating, they have added another pull-up transistor to force the output to V_{DD}. Both the gating and pull-up transistors are controlled by test control signal (TC). TC is assigned "0" in shift mode such that the first level NOR gate is disabled since it is cut off from the supply. Figure 1 shows FLS structure.

Although FLS scheme has less overhead in terms of area, propagation delay, or even switching activity in gating logic compared with other gating schemes, it is unable to block all transients in the combinational logic because the output of the first level gates is forced to a fixed value, which is similar to NOR and TG gating. Another approach by Bhunia et al. [15, 16] gives an alternative solution for Enhanced Scan in delay fault testing named First Level Hold (FLH) which gates the rippling transition to the combinational logic during shift mode. In addition to two gating pull-up and pull-down transistors, a cross-coupled inverter latch controlled by TC signal has been employed to hold the output of the first level gates during pattern shifting until the next pattern is launched. A local TC signal has been generated for each first level gate to drive the related gating and holding logic. Gating and holding logics inserted to all first level gates in addition to hardware for local TC generation applied to individual gates have large overhead in terms of area and power consumption. All of the mentioned techniques can reduce shift power in combinational logic effectively. However, they suffer from large overhead in terms of area and propagation delay.

In order to eliminate performance degradation due to gating logic, Suhag et al. [17] have reported a modified transistor level design of scan flip-flop for critical paths. The modified scan cell has been implemented with nine extra transistors compared to conventional scan cell to tie the output of scan cell to combinational logic to the constant value "1" and improve the performance on this path. However, nine extra transistors in the scan cell structure result in significant switching activity and peak power elevating with

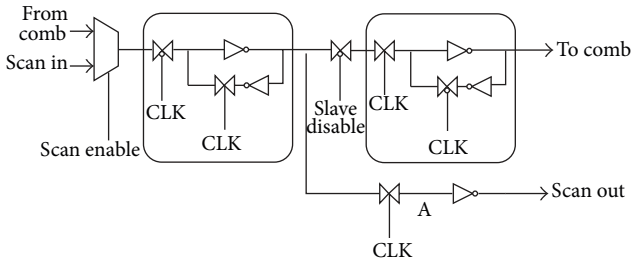

Figure 2: Modified scan flip-flop for low power delay fault testing [9].

severe area overhead. In addition, it is not able to cut off all the redundant switching activity in the combinational logic for the same reason we mentioned earlier about freezing the scan cell output to a constant logic during shifting. Another modified scan flip-flop for low power delay fault testing has been proposed in [9].

As it has been shown in Figure 2, it bypasses the slave latch with an alternative low cost dynamic latch in scan shifting path. Therefore, it can successfully eliminate all transitions to the combinational logic. For the application of stuck-at faults, slave latch is disabled by scan enable signal. However, no evaluation on benchmark circuits or comparison in terms of power consumption, performance, and area overhead to the existing gating methods has been presented.

Partial gating methods [18–22] have been proposed to reduce the full gating penalties in area overhead and performance degradation. By proper selection of scan cells on noncritical paths to be gated and their gating values, they try to maximize shift power reduction with acceptable performance degradation. Most recently reported partial gating methods such as those in [23–26] gate a subset of scan cells not only during shift mode but also during capture mode in order to reduce peak power besides shift power reduction. However, in large industrial designs, scan cells have large fan out cones. Thus, ungated scan cells in partial gating method can still cause a great amount of switching activities in the combinational logic. Moreover, in both existing full gating and partial gating techniques, significant power is consumed in the gating elements themselves, which causes the peak power to increase from 5% to 60% in all the benchmark circuits when the gating overhead was considered [9]. This is due to the large switching activity occurring in the gating logic when scan mode changes to capture mode or vice versa [17]. The missing part of both existing full gating and partial gating methods is that they have limited their approaches only to power reduction in combinational circuits during shift cycles without highlighting much that shift power consumption is also related to total amount of power consumed in scan chain besides combinational logic.

While aforementioned gating methods mainly have tried to reduce the level of switching activity in the combinational part, a few schemes can be found in the literature that have concentrated on reducing the level of switching activity in scan cell. A modified scan element has been presented in [10] to reduce scan cell switching activity. Figures 3(a) and 3(b) demonstrate the conventional and modified scan

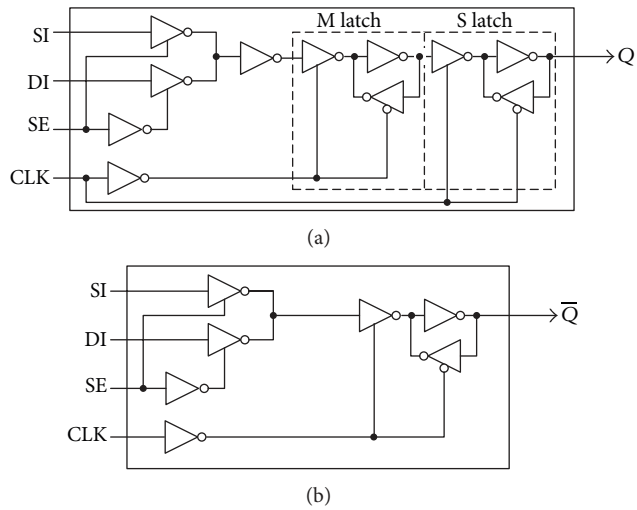

Figure 3: (a) Conventional scan architecture and (b) modified scan architecture [10].

architectures, respectively. As observed from Figure 3(b), master output $\overline{Q}$ of modified scan cell can be utilized instead of Q to form the scan chain which results in three less inverters in the scan output propagation path. In addition, an inverter in the internal multiplexer of scan cell has been removed, which leads to less propagation delay in the input path of the modified scan cell. However, the main drawback of this scheme is that the structure represents a latch instead of flip-flop which makes it an unsuitable element to be employed as a scan cell.

Finally, many previous works have successfully reduced power consumption in both combinational logic and scan chain by using separate methods for each section. In [27], FLS has been applied to the scan partitioning method which activates a part of scan cell at a time to reduce power consumption in scan chain. To overcome the limitation of the existing gating methods, we propose a gating scan architecture with the following contributions.

(i) The main novelty of the proposed gating scan architecture is an integrated solution targeting power reduction in combinational part as well as inside the scan cell itself which, to the best of our knowledge, have not been reported at the same time in any previous works.

(ii) Most of the previous gating methods did not consider the negative impact of the power consumed in the gating logics that result in peak power violation during capture mode. The proposed method can reduce the maximum level of peak power compared to existing gating methods as it will be explained in the next section.

(iii) The proposed gating scan architecture introduces a new short shift path that improves both shift and capture propagation delays as well as power consumption in scan chain during shift mode. This makes shifting at higher frequency possible in those cases

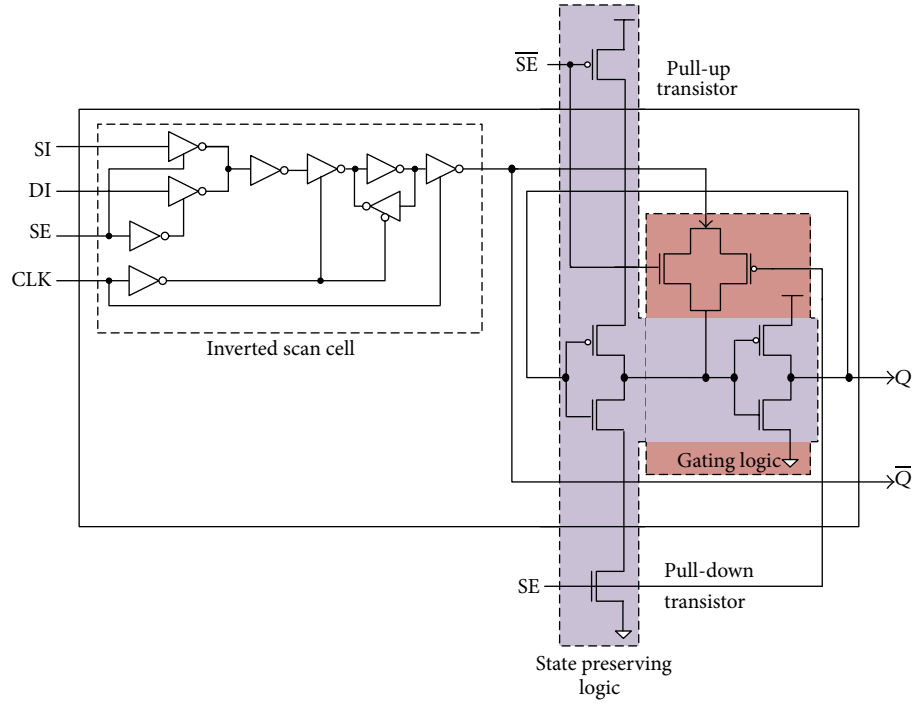

Figure 4: The proposed new gating scan cell structure.

that maximum shift frequency has been bounded by maximum allowable power consumption. Therefore, the proposed gating design improves test application time over existing gating solutions.

(iv) The proposed gating scan cell has minimum impact on the performance degradation due to smaller launch and capture propagation delay compared to existing gating methods. Therefore, in the application of partial gating more scan cells can be gated using the proposed gating scan cell without violating critical path timing and thus higher power reduction is achievable.

3. The Proposed Gating Scan Architecture

We propose a novel gating scan structure for shift power reduction considering both scan chain and combinational part with the following features:

(A) gating redundant transitions from scan cell to combinational logic during shift mode,

(B) reducing switching activity inside the scan cell during shift mode.

In order to achieve the above-mentioned features within an integrated structure, we have modified the slave latch in the conventional master/slave scan cell with state preserving and gating ability. In addition, to achieve second feature, a new shift path has been set up which at the same time speeds up shift and capture process over existing gating methods. Since state preserving and gating logics have been embedded as part of slave latch in the proposed gating scan cell, the area overhead is as low as two transistors that are sharable by several scan cells. The proposed structure contributes to average power reduction in the scan architecture (combinational logic and scan chain) during shift mode while not causing high peak power during capture mode. In gating methods the main source of excessive peak power during capture mode is the switching activities in gating elements when the mode changes from shift to capture mode or vice versa. Excessive peak power can be avoided by reducing the level of switching activity during test [3]. Therefore, the proposed structure is able to control peak power violations by reducing switching activities in other parts of scan cells. A conceptual discussion about our architecture will be presented in the next section in order to preliminarily show the effectiveness of our proposed scan architecture with respect to total average power, propagation delay, and area overhead.

We have improved the modified scan element [10] and named it gating scan cell. According to Figure 4, each gating scan cell consists of three main substructures:

(i) gating logic,

(ii) state preserving logic,

(iii) inverted scan cell.

3.1. Gating Logic. During shift cycle, the rippling transitions cause great switching activities in the scan chain. The propagation of this switching activity into the combinational part contributes to large redundant transitions in the circuit lines. In order to suppress the scan chain transitions from propagating during shift cycles, we have proposed a scan structure which is augmented by a gating logic. For constructing the

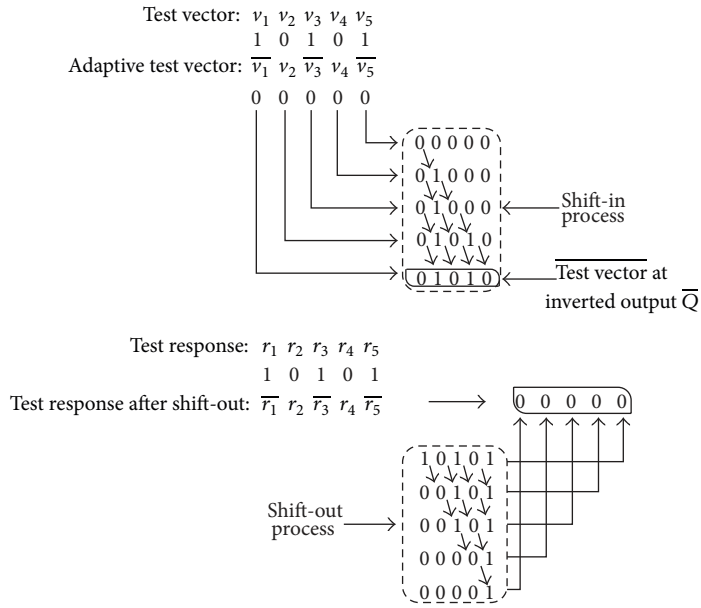

Figure 5: Adaptive scan process.

gating logic, we have utilized a transmission gate and an inverter to gate the scan output to the combinational logic. It uses the transmission gate to cut off the connection between the inverted scan cell output $\overline{Q}$ (used for stitching the scan cells) and the output Q of the scan cells during shift mode. As a result, the switching activities on the $\overline{Q}$ during shift mode does not affect the scan cell output Q which is used for driving the combinational logic. High resistance offered by an inactive transmission gate reduces the leakage current in the transmission gate during shift mode and response capture cycle since the transmission gate is idling in these intervals. In addition, transmission gate is a strong driver to feed the gating logic inverter and pseudo primary inputs during normal/capture mode.

3.2. State Preserving Logic. In order to totally prevent the unnecessary transitions to the combinational logic during shift mode, a state preserving logic has been proposed. It is a feedback structure that refreshes the scan output Q with the previous logic state. The two pull-up and pull-down sleep transistors are active during shift mode which makes the state preserving logic fixes the scan output logic to the same previous logic. However, unlike gating logic, this section is transparent in normal/capture mode of operation since the sleep transistors are inactive. During this mode, the state preserving logic consumes low leakage power since the two sleep transistors cut off the power rail. The two pull-up and pull-down transistors also contribute to active leakage reduction due to stacking effect [28, 29]. These can alleviate the effect of state preserving on peak power during normal/capture mode. The transmission gate and pull-up and pull-down sleep transistors are driven by shift enable signal SE so no extra control signal is required. Sharing the pull-up and pull-down transistors of the state preserving logic among all the scan cells can alleviate the scan chain area overhead.

3.3. Inverted Scan Cell. We have removed part of slave latch in the conventional scan cell and exploited it as the inverted scan cell. The elimination of two by-passed inverters and a transmission gate at the scan new shift path contributes to less switching activities inside the scan cell and consequently in scan chain. On the other hand, this reduces the number of switching activities needed for transferring the data to the scan cell's shift output. This results in average power reduction during shift mode while moderating the effect of gating and state preserving on peak power during capture mode. Although the inverted scan cell has master latch only, the overall scan architecture can still work as flip-flop because the inserted state preserving logic together with gating logic functions as slave latch in addition to their power reduction roles. Due to the shift path with less complexity, the scan chain speed has been accelerated during shifting. The reduced area and propagation delay due to the removal of two inverters and a transmission gate in the scan structure can moderate the area and delay overhead imposed by the augmented gating logic and also state preserving logic.

Eliminating the inverters in the scan cell structure does not affect the correctness of test patterns shifted into scan chain since adaptive test patterns can be used instead of original ones. The correct function of scan chain is achievable by special care of ATPG that generates the adaptive test patterns. The adaptive scan process has been summarized in Figure 5.

Let v_i represent a test pattern to be shifted to a scan cell. The adaptive test patterns are generated such that $\overline{v_i}$ is shifted to the destination of inverted scan cell after shift-in process. $\overline{v_i}$ is inverted to v_i after going through gating logic during test

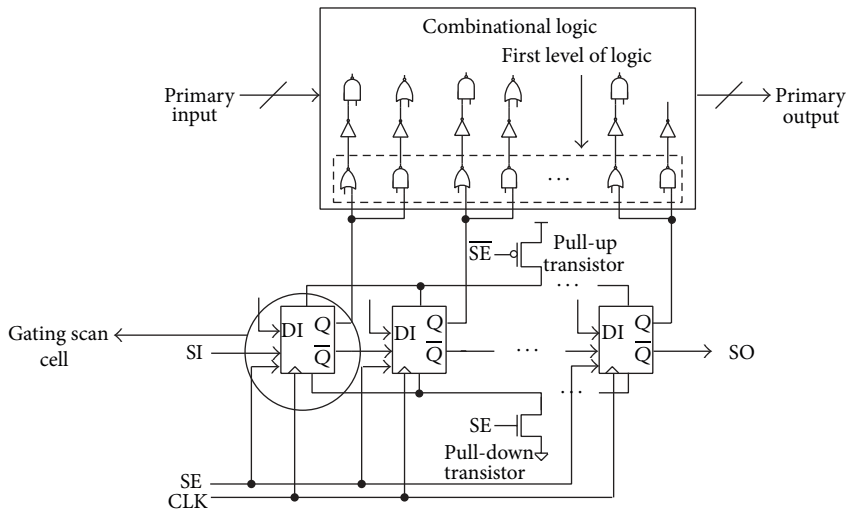

Figure 6: The proposed gating scan chain architecture.

application. Let v_i' be an adaptive test pattern and $1 \le i \le N$, where N is the number of scan cells in a scan chain. $v_i' = v_i$ for even index i and $v_i' = \overline{v_i}$ for odd index i whether N is an odd or even number. Adaptive test pattern formulation is as follows:

$$\begin{aligned} v_i' &= v_i \quad \text{even index } i, \\ v_i' &= \overline{v_i} \quad \text{odd index } i. \end{aligned} \tag{1}$$

Modifications are necessary for test responses after shift-out process since the responses are captured by the inverted scan cells. Let r_i represent the test response of a pseudo output. After being captured by the inverted scan cell, it becomes $\overline{r_i}$. Shifting process of $\overline{r_i}$ is taking place along the inverted scan cells. Let r_i' be the test response that reaches scan-out after shifting where $1 \le i \le N$ and N is the number of scan cells. $r_i' = \overline{r_i}$ for odd index i and $r_i' = r_i$ for even index i when N is an odd number while $r_i' = r_i$ for odd index i and $r_i' = \overline{r_i}$ for even index i when N is an even number. Modifying test pattern formulation is as follows.

For N number of scan cells when N is an odd number, consider the following:

$$\begin{aligned} r_i' &= r_i \quad \text{even index } i, \\ r_i' &= \overline{r_i} \quad \text{odd index } i. \end{aligned} \tag{2}$$

For N number of scan cells when N is an even number, consider the following:

$$\begin{aligned} r_i' &= r_i \quad \text{odd index } i, \\ r_i' &= \overline{r_i} \quad \text{even index } i. \end{aligned} \tag{3}$$

Therefore, inversion needs to be performed on r_i' when $r_i' = \overline{r_i}$ to retrieve the correct test response for response comparison.

Figure 6 illustrates the proposed scan chain architecture in full gating DFT method. In the application of partial gating, $\overline{Q}$ output of either proposed gating scan cells or conventional scan cells should be used to form the scan chain for correct test pattern shifting operation. The area overhead imposed by proposed gating structure is only two extra transistors per several scan cells.

Similar to [9], our proposed method could eliminate all the transitions to the combinational logic. However, the difference between the proposed method and [9] is that we have replaced a part of slave latch with state preserving and gating logic and control it by scan enable (SE) signal which can result in two advantages compared to this method:

(1) less switching activity inside the proposed scan cell due to

(A) state preserving logic that is controlled by SE in the proposed gating scan cell, which causes less switching activity compared to the one controlled by clock,

(B) four less numbers of transistors in the scan cell structure;

(2) two pull-up and pull-down transistors have been used to control the state preserving, which can be shared among several scan cells. Thus, area overhead is reduced.

4. Experimental Results and Comparisons

To verify the effectiveness of the new gating scan cell architecture in terms of power and propagation delay over existing gating methods, we have conducted experiments to compare the proposed scan cell with the conventional scan cell, partial MUX gating scan cell, NOR gating scan cell, FLS, and modified scan cell reported in [9] which is one of the latest low power scan cells for gating. The initial simulations were performed using the Berkeley Predictive Technology Model (PTM) 45 nm CMOS technology (BSIM4) [30] in

Table 1: Comparison of total power consumption during shift and normal/capture mode.

	Prop. scan cell	FLS scan cell		Partial MUX gating scan cell		NOR gating scan cell		Modified scan cell		Conventional scan cell	
	Power con. (W)	Power con. (W)	% imp. over	Power con. (W)	% imp. over	Power con. (W)	% imp. over	Power con. (W)	% imp. over	Power con. (W)	% imp. over
Ave. total power	1.5352$E-06$	2.6251$E-06$	41.51	2.5276$E-06$	39.26	2.7807$E-06$	44.79	1.8385$E-06$	16.49	2.1370$E-05$	28.17

Table 2: Comparison of average power consumption during shift mode.

		Prop. scan cell	% imp.	FLS scan cell	% imp.	Partial MUX gating scan cell	% imp.	NOR gating scan cell	% imp.	Modified scan cell	% imp.
Avg. power (W)	Shift cycle #1	1.7915$E-06$	37.16	3.4209$E-06$	−19.98	2.8857$E-06$	−1.21	3.5642$E-06$	−25.01	1.9972$E-06$	29.94
	Shift cycle #2	1.7880$E-06$	37.42	3.4172$E-06$	−19.59	2.8920$E-06$	−1.21	3.5699$E-06$	−24.93	1.9930$E-06$	30.25
	Shift cycle #3	1.7953$E-06$	37.14	3.4261$E-06$	−19.94	3.5013$E-06$	−22.58	3.5683$E-06$	−24.92	1.9920$E-06$	30.25
	Shift cycle #4	1.7947$E-06$	37.15	3.4282$E-06$	−20.04	3.5004$E-06$	−22.57	3.5680$E-06$	−24.94	1.9918$E-06$	30.25

HSPICE by applying random patterns with the supply voltage of 1.0 Volt at room temperature. Since the main purpose of these primary experiments is to evaluate the proposed gating scan cell structure as the basic unit in the proposed gating scan chain in terms of power and propagation delay, all of the comparison parameters have been measured for the scan cell structure by applying random patterns and without considering combinational part. Due to the compact architecture of the gating scan cell with state preserving and gating logic, scan cells in FLS, partial MUX gating, and NOR gating schemes have been considered as a consistent entity with their gating structures. Table 1 contains comparisons of the mentioned scan cells with the proposed gating scan cell in terms of total average power during shift and normal/capture mode. In FLS scan cell, an inverter gate has been considered as the first level gate that is the most optimal condition for FLS. The percentage of improvements for proposed gating scan cell over other scan cells is displayed under each related scan cell column.

As observed from Table 1, the proposed gating scan cell exhibits 28.17% improvement in terms of average total power over the conventional scan cell. It means the power consumption in the proposed gating scan cell is even less than the original scan cell without any gating policy. This is expected because the proposed gating scan cell eliminates switching activity on the stimulus path of scan cell during shift mode. Also using shorter shift path that consists of less number of transistors compared to conventional scan cell intensifies power reduction impact of proposed scan cell. The proposed gating scan cell can save up to 44.79% average total power over existing gating scan cells such as NOR gating scan cell that has been used widely in most partial gating methods. It is noteworthy that, except proposed gating scan cell and modified scan cell, all of the compared scan cells experience increase of the total power consumption up to 30.12% compared to conventional scan cell. The proposed scan cell can save total power by 16.49% over modified scan cell since the gating and state preserving logic has been implemented with less number of switching activities.

In Table 2, the amount of power consumption for proposed gating scan cell and other existing gating scan cells during four-shift cycle has been shown. Each column contains the shift power consumption for related scan cell and the percentage of improvement over conventional scan cell. As it is observable from Table 2, the proposed gating scan cell outperforms existing gating scan cells in terms of shift power reduction inside the scan cell structure by 32.95% (on average) over conventional scan cell. Other gating schemes such as FLS, partial MUX gating, and NOR gating show increase in power consumption since they force the scan cell's driving path to a constant logic during shifting that can cause extra transient at this line (refer to Figure 7). Partial MUX gating consumes less shift power in the first two shift cycles compared to the other shift cycles. The reason is that in these shift cycles, the scan cell's driving path has the same value as the gating value when the mode changes to shift mode; thus, no redundant transition occurs.

Based on Table 2, unlike FLS scan cell, partial MUX gating scan cell, and NOR gating scan cell, the proposed gating scan cell can reduce power consumption in scan cell structure during shift mode. It is noteworthy that modified scan cell is able to reduce power only on the scan cell stimulus path by holding the logic during shift mode. However, besides power reduction on stimulus path via holding value on this line, the proposed gating scan cell can also reduce the switching activity inside the scan cell architecture. Hence, we achieve more power reduction compared to modified scan cell.

As mentioned before, one of the main concerns about gating designs is elevated peak power beyond the chip power

Table 3: Comparison of peak power consumption during normal/capture mode.

		Prop. scan cell	% incr.	FLS scan cell	% incr.	Partial MUX gating scan cell	% incr.	NOR gating scan cell	% incr.	Modified scan cell	% incr.
Peak power (W)	Capture cycle #1	$5.3813E-05$	−0.07	$5.6058E-05$	**4.09**	$5.4240E-05$	0.72	$5.6006E-05$	3.99	$5.3778E-05$	−0.13
	Capture cycle #2	$5.3953E-05$	−0.07	$5.5041E-05$	1.94	$5.3995E-05$	0.003	$7.1611E-05$	32.63	$5.3959E-05$	−0.07
	Capture cycle #3	$5.3969E-05$	0.003	$5.4132E-05$	0.30	$5.3970E-05$	0.005	$7.1591E-05$	32.65	$5.3954E-05$	−0.02
	Capture cycle #4	$5.4454E-05$	**0.94**	$5.4746E-05$	1.49	$5.4242E-05$	0.55	$7.1578E-05$	**32.69**	$5.4100E-05$	**0.29**
	Capture cycle #5	$5.4589E-05$	0.93	$5.42010E-05$	0.21	$5.7592E-05$	**6.48**	$7.1567E-05$	32.32	$5.4089E-05$	0.007

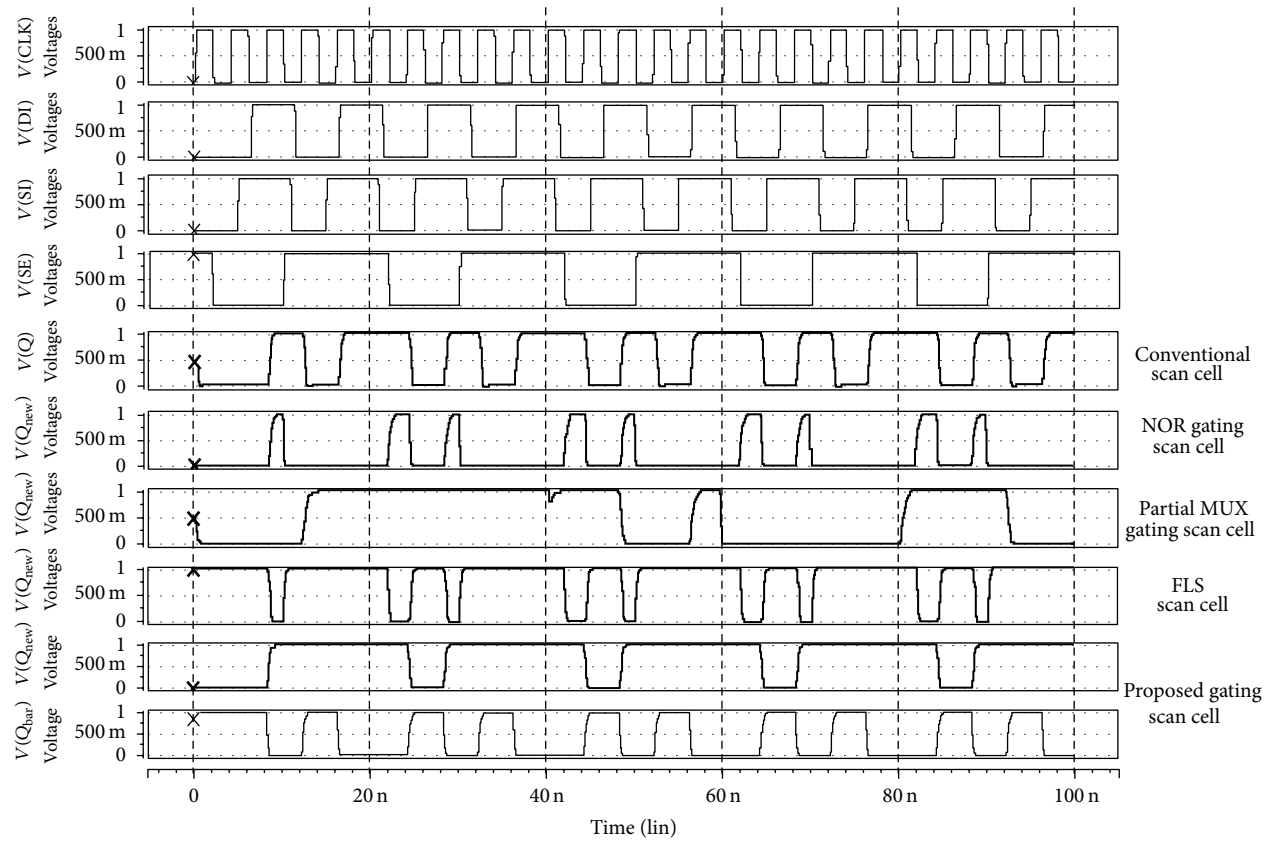

Figure 7: Driving path timing waveforms for existing gating architectures and the proposed gating scan cell.

budget caused by gating logic toggling between gating (shift) mode and transparent (normal/capture) mode. In order to show that the proposed gating scan cell has low impact on peak power increase, we have compared the percentage of peak power increase over conventional scan cell in the proposed gating scan cell and existing gating methods through five normal/capture cycles (each including one clock period).

The proposed gating scan cell and modified scan cell are able to reduce the highest peak power compared with existing gating scan cells. According to Table 3, the proposed scan cell elevates peak power up to 0.94% (less than 1%) while the highest peak power increase in other gating scan cells is up to 32.69% (NOR gating scan cell). Unlike other compared gating scan cells, in case of NOR gating scan cell, peak power increase remains high during four successive capture cycles; thus, there is a strong possibility to elevate the temperature beyond the chip thermal budget. Figure 7 illustrates the impact of existing gating methods such as FLS, partial MUX gating along with proposed gating scan cell, on the stimulus path transients to combinational logic. As it is observable from the waveforms, in contrast with other gating methods and conventional scan cell, the state preserving and

Table 4: Comparison of propagation delay overhead.

	Proposed scan cell		FLS scan cell		Partial MUX gating scan cell		NOR gating scan cell		Modified scan cell	
	Ave. propa. delay (S)	% imp.	Ave. propa. delay (S)	% imp.	Ave. propa. delay (S)	% imp.	Ave. propa. Delay (S)	% imp.	Ave. propa. delay (S)	% imp.
SI to shift output (shift delay)	$1.437E-09$	9.33	$1.587E-09$	−0.12	$1.587E-09$	−0.12	$1.586E-09$	−0.06	$1.448E-09$	8.64
DI to shift output (capture delay)	$9.458E-10$	12.82	$1.089E-09$	−0.36	$1.157E-09$	−6.63	$1.086E-09$	−0.09	$9.545E-10$	12.02
DI to Q_{new} (launch delay)	$1.107E-09$	−2.02	$1.247E-09$	−14.13	$1.271E-09$	−17.14	$1.249E-09$	−15.11	$1.135E-09$	−4.60
CLK to shift output	$1.373E-10$	51.75	$2.866E-10$	−0.70	$2.865E-10$	−0.66	$2.864E-10$	0.0	$1.477E-10$	48.1
CLK to Q_{new} (launch) output	$3.073E-10$	−7.97	$4.470E-10$	−57.06	$4.713E-10$	−65.60	$4.490E-10$	−17.84	$3.354E-10$	−17.84

gating logic is able to completely suppress all transients to the combinational logic. Q_{new} is the Q output of the gating scan cell that drives the combinational part and Q_{bar} represents the new shift output in proposed gating scan cell. As it is shown, the waveform of Q_{new} in the proposed scheme shows almost 50% reduction in transients for the same input patterns compared to FLS, partial MUX gating, NOR gating, and conventional scan cell, leading to less switching activity inside the combinational logic.

From the results it can be concluded that the proposed gating scan cell is able to improve power consumption compared to existing gating methods. This is not only because of power reduction inside the scan cell, but also according to Figure 7 due to power reduction in combinational logic by holding the logic on the scan cell's stimulus path during shifting. The proposed scan architecture also has contributed to accelerating shift because the inverted scan cell has less number of transistors and gating logic and state preserving logic do not involve the scan shift propagation path. Also, due to shorter shift output the captured data will be available faster on the shift output. Therefore, improvements in shift and normal/capture propagation delay over FLS, partial MUX gating scheme, and NOR gating have been observed. A comparative impact of the existing scan gating schemes including the proposed architecture on the scan cell delay parameters has been summarized in Table 4. For all compared scan cells the amount of average propagation delay is followed by the percentage of improvement over conventional scan cell.

According to Table 4, propagation delay improvements in shift and capture have been achieved over FLS scan cell, partial MUX gating scan cell, NOR gating scan cell, and modified scan cell. The clock to shift output delay has been improved in the proposed gating scan cell by 51.75% over conventional scan cell. Moreover, the proposed scan cell improves data shift and capture propagation delays by 9.33% and 12.82%, respectively, compared to conventional scan cell while the delay penalty on data launch and clock to launch output is 2.02% and 7.97%, respectively. However, it still shows significant reduction in launch delay penalties compared to the scan cells in other gating schemes. Thus, we can expect that the proposed gating scan chain will be able to keep performance degradation caused by gating under acceptable threshold.

Since the layout rules for feature size of 45 nm gate length are not available, the measure that has been used for area overhead calculations is the total transistor active area ($W * L$ for a transistor). In order to evaluate the proposed gating scan cell in terms of area overhead, we have compared it with FLS and NOR gating that have the least area penalty in turn among existing gating techniques. The routing overhead has not been considered in area overhead. However, the routing overhead associated with the proposed gating structure should not be high since no additional control signal is required. In the proposed gating architecture, similar to NOR gating, area overhead increases as the number of scan cells in the design increases. The area overhead in FLS does not depend on the number of scan cells directly but the numbers of first level gates are driven by scan cells. This is because gating transistor and pull up transistor in FLS have been introduced on each gate in the first level of combinational gates. Therefore, we consider ISCAS'89 benchmark circuits to study the impact of proposed gating architecture and existing gating techniques on area overhead. Referring to [22], for random input patterns, approximately half of the first level gates are switching at the same time and the gating transistor for idle gates is not actually used. Therefore, the channel width for the shared gating transistor in FLS has been considered half of the sizes of unshared gating transistors and is given by

$$W_{gating} = 0.5 * FO * (10 * W_{min}), \quad (4)$$

where FO is the number of first level gates. In the proposed gating scan cell the pull-up and pull-down transistors in state preserving logic have been shared among all scan cells. Like FLS, we have assumed that for random input patterns nearly half of the scan cells do not switch and the pull-up and pull-down transistors are practiced for almost half of the scan cells

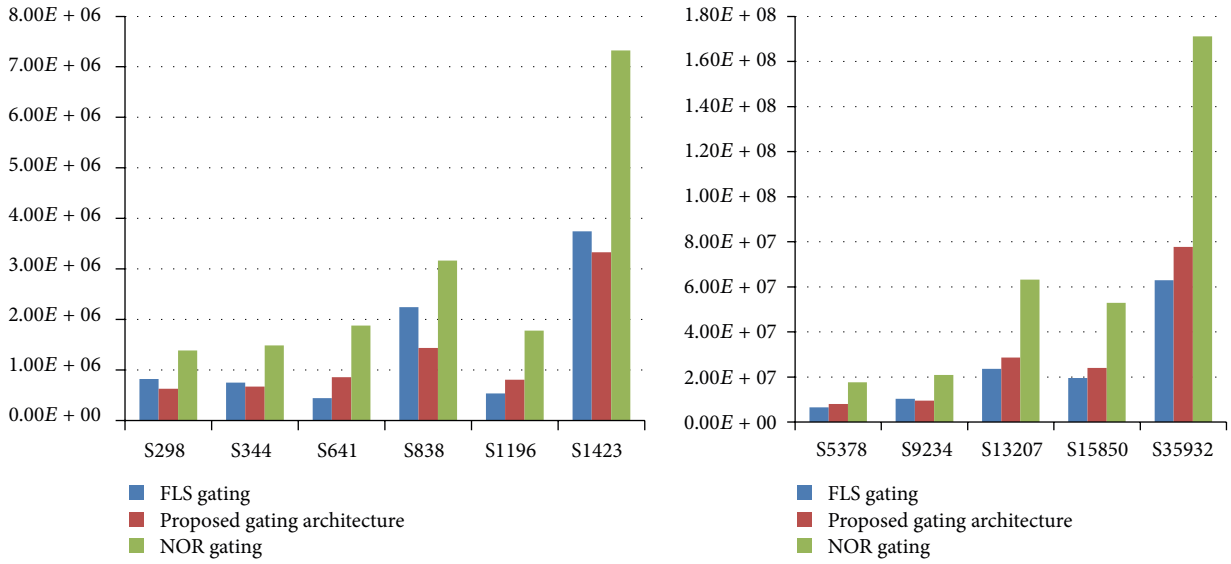

Figure 8: Area overhead comparisons.

at the same time. Thereby, the channel width for shared pull-up and pull-down transistors is chosen to be as follows:

$$W_{\text{pull up}} = 0.5 * FF * \left(5 * W_{\text{min(Pmos)}}\right),$$
$$W_{\text{pull down}} = 0.5 * FF * \left(5 * W_{\text{min(Nmos)}}\right), \quad (5)$$

where FF is the number of scan cells. The comparative impact of the proposed gating architecture and existing gating techniques on area increase in nm^2 scale for different benchmark circuits has been shown in Figure 8.

According to Figure 8, the proposed gating architecture exhibits 21.42% improvement on average in terms of area overhead compared to NOR gating for all benchmark circuits. As mentioned earlier, area overhead in FLS is highly affected by the number of unique fanouts (nonoverlapped fanout cones) of scan cells in which gating transistor and pull-up transistor are inserted. Therefore, as this ratio increases above two in benchmark circuits, the proposed gating architecture saves more area up to 11.29% (s838) compared to FLS. However, the proposed gating architecture loses its efficiency in area improvement over FLS in benchmark circuits with the ratio of the unique fanouts to number of scan cells less than two. The highest area penalty for the proposed gating architecture over FLS is 12.24% in s641 which has equal number of unique fanouts and scan cells (ratio = 1). However, in large industrial designs the number of fanouts of scan cell is usually more than one. Thus, the proposed gating architecture area overhead over FLS is not usually high. The area overhead degradation compared to FLS for all benchmark circuits is on average 1.18% for an average 1.8 unique fanouts per scan cell.

Power and delay improvements for scan cell can be extended to the whole scan chain in our future works of experiments. In order to verify that the proposed architecture keeps its efficiency in terms of power and performance for the scan chains with large number of scan cells, postlayout simulations will be conducted on the benchmark circuits. Further simulations will be established on the various benchmark circuits by applying adaptive test patterns to clarify the exact amount of dynamic power improvement in the combinational logic and results will be presented in near future.

5. Conclusion

Scan gating approach offers simple yet effective solution to reduce shift power significantly independent of test set and is less intrusive to the design. However, gating logics have been exploited as the existing gating methods add significant delay to signal propagation paths. Moreover, they suffer from large overhead in terms of area and switching activity inside the gating logics in normal/capture mode that has high negative impact on peak power. Likewise, shift power reduction in most existing gating approaches has mostly been concentrated on combinational logic while scan part has received less attention. We proposed a novel gating scan architecture as an integrated solution for shift power reduction in both scan cells and combinational logic under area constraints. The proposed gating scan cells in this structure are modified scan cells augmented by gating and state preserving logics to gate and hold the scan cells stimulus path with low impact on peak power. Critical shift timing has been improved by using a less complex shift path in new gating scan cell. Compared to the lowest cost gating techniques the proposed gating scan cell has less DFT overhead with respect to average power, shift, and capture delay. Similar to other gating methods such as modified scan cell, the proposed gating architecture can be used for delay fault testing. The proposed gating scan cell can be applied effectively to both full gating and partial gating methods. The fault coverage is not degraded and it does not face routing problems since no additional control signal has been employed. The proposed scheme can efficiently be utilized in

BIST architecture. It can also be applied together with other scan-based power optimization methods such as scan chain partitioning and reordering techniques. Low power ATPG-based methods can be applied to the proposed structure efficiently. Therefore, these make the proposed approach a potential candidate for scan-based DFT architectures.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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