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A Novel SiC Asymmetric Cell Trench MOSFET With Split Gate and Integrated JBS Diode

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ABSTRACT A novel high performance SiC asymmetric cell trench MOSFET with split gate (SG) and integrated junction barrier schottky (JBS) diode (SGS-ATMOS) is proposed for the first time. The shielding effect provided by the SG structure not only reduces the gate-drain capacitance (C_{gd}) but also alleviates the electric field crowding in the dielectric layer at trench corner. The integrated trench JBS diode bypasses the PiN body diode while obtaining good double protection from the SG and p-type shielding region. Therefore, not only the MOSFET but also diode performance is significantly improved for the proposed structure. Numerical analysis results show that compared with the conventional asymmetric cell trench MOSFET (Con-ATMOS), the high frequency figure of merit (HFFOM[1], $R_{on} \cdot C_{gd}$) is reduced by 92.5% and the Baliga figure of merit (BFOM, $BV^2/R_{on,sp}$) is increased by 57.2%, respectively. In addition, the forward conduction voltage drop (V_F), reverse recovery charge (Q_{rr}) and peak reverse recovery current (I_{rrm}) of the diode are reduced from 3.10V, 1.95μC/cm^2 and 68.0A for the Con-ATMOS to 1.56V, 0.97μC/cm^2 and 35.9A for the proposed SGS-ATMOS, respectively. Compared with the Con-ATMOS, the turn-on loss (E_{on}) and turn-off loss (E_{off}) of the proposed device are reduced by 33.3% and 33.0%, respectively. The E_{on} and E_{off} of the proposed device are also 33.6% and 30.0% off compared with the Con-ATMOS with external JBS diode, respectively. The temperature characteristics of the SGS-ATMOS are also discussed and it is found that the proposed device exhibits good performance at high temperature.

INDEX TERMS 4H-SiC, trench MOSFET, asymmetric cell, split gate, junction barrier Schottky (JBS), figure of merit (FOM), turn-on loss, turn-off loss.

I. INTRODUCTION

Silicon carbide (SiC) based power semiconductor devices are very suitable for high voltage, high power and high temperature applications due to its excellent material performance, such as wide bandgap, large critical electric field strength and high thermal conductivity [1]–[6]. Compared with silicon insulated gate bipolar transistor (Si IGBT), SiC metal-oxide-semiconductor field effect transistor (MOSFET) has faster switching speed and lower switching loss, which significantly improve electric power conversion efficiency and reduce size of passive components [7]–[10]. Although SiC planar gate MOSFET demonstrates good reliability performance [11], [12], trench MOSFET (TMOS) structure is still preferred since it has better device performance, which derived from large channel density and weakened junction field effect transistor (JFET) effect. However, for the conventional SiC TMOS, high electric field in the SiC drift region and large relative permittivity (ε) ratio of SiC to SiO_2 lead to very high electric field in the trench gate oxide layer at the blocking state. The gate oxide layer will breakdown or degrade before the drain bias reaches avalanche breakdown voltage (BV_{av}). 3MV/cm is commonly adopted as the maximum electric field in the gate oxide layer ($E_{ox,max}$) for good long-time reliability. To reduce the electric field in the gate oxide layer, a heavily doped p-type shielding (p-SH) region under the trench bottom is

introduced [13], [14]. However, the p-SH region brings about additional JFET region, which increases the specific on-state resistance ($R_{on,sp}$). So, a relative-heavily doped n-type current spreading layer (CSL) is inserted between the p-base and n drift region [15], [16], or it wraps the p-SH region [17]. It helps to spread current from the MOS channel into the drift region and weaken the JFET effect caused by the p-SH region. References [18] and [19] introduce a SiC double trench MOSFET (DTMOS) with a p-SH region only in the sidewall and bottom of a source trench. The DTMOS achieves a low $R_{on,sp}$ as well as alleviates the electric field crowding in the gate trench oxide layer. However, it has large gate-drain capacitance (C_{gd}) contributed by the bottom of the gate trench [20]. The DTMOS also shows a gate oxide rapture due to its instable avalanche robustness under unclamped inductive switching (UIS) stress [21]. In recent years, SiC asymmetric cell TMOS structures, such as the conventional asymmetric cell trench MOSFET (Con-ATMOS) [22], [23] and asymmetric cell tilt implanted trench MOSFET (ACTI-TMOS) [24], etc. have been proposed. The source-connected asymmetric p-SH region not only alleviates the electric field crowding at the trench bottom and corners in the gate oxide layer but also reduces the C_{gd} at the same time. Therefore, improved device performance and gate oxide reliability were achieved. However, for the SiC asymmetric cell TMOS structures, the gate trench bottom and side wall faced to the n drift region still introduce additional C_{gd} and the electric field crowding at the trench bottom and corners in the gate oxide layer still limit the improvement of device performance and gate oxide reliability.

For the SiC MOSFET, the use of PiN body diode is usually avoided due to the large turn-on voltage and bipolar degradation [9], [25]. External anti-parallel SiC junction barrier schottky (JBS) diode is commonly used but it will increase volume, capacitance and cost of the SiC device. Additional connection wire between the SiC JBS diode and MOSFET also increases stray inductance and reduces reliability of the device. Therefore, integration of a JBS diode in the SiC MOSFET is a promising solution. Using a separate active region to integrate the JBS diode in the SiC MOSFET is a relatively easy way [26], [27]. However, it adds a relatively large chip area. To integrate the JBS diode in the MOSFET cell, a lot of efforts have been made in [28]–[33]. SiC TMOSs with an integrated JBS diode between two trench gates were demonstrated in References [30] and [31], respectively. Based on the conventional SiC TMOS with p-SH region, [32]–[34] report a SiC TMOS with an integrated JBS diode at the side wall of an additional source trench. In these SiC TMOS structures, however, the integrated JBS diode occupies additional chip area and impacts performance of the SiC MOSFET.

In this paper, a novel SiC asymmetric cell TMOS with a split gate (SG) and integrated JBS diode (SGS-ATMOS) is proposed for the first time. Compared with the Con-ATMOS, the proposed structure demonstrates excellent static and dynamic performance with suppressed electric field crowding

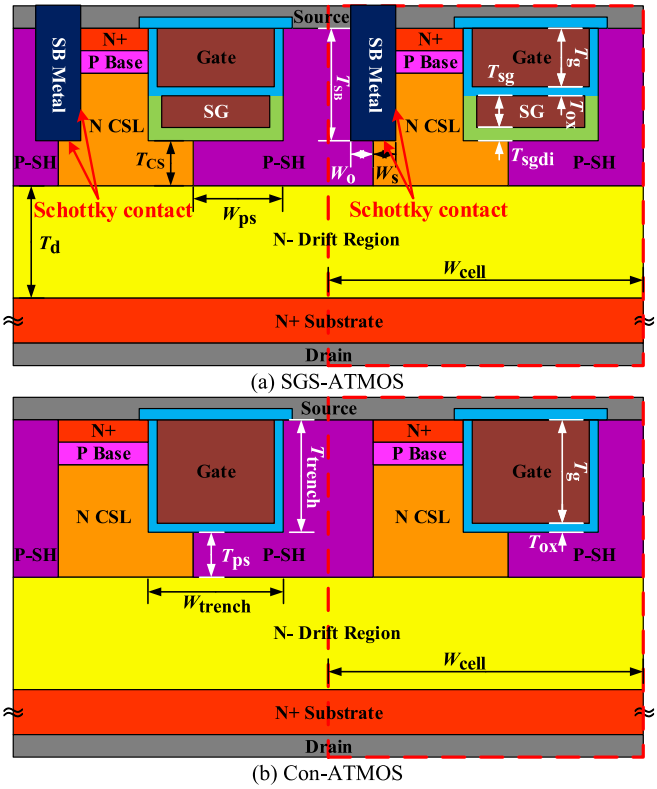

FIGURE 1. Schematic cross sectional view of the SiC devices: (a) proposed SGS-ATMOS and (b) Con-ATMOS.

at the trench corners. Meanwhile, the integrated trench JBS diode with double protection demonstrates excellent performance without occupation of additional chip area.

II. DEVICE STRUCTURE AND MECHANISM

Fig. 1 (a) and (b) show the schematic cross-sectional view of the proposed SiC SGS-ATMOS and Con-ATMOS, respectively. Both structures are asymmetric cell TMOS with a source-connected asymmetric p-SH region surrounding the sidewall and part of the trench bottom. The negative charges provided by the depletion region of the p-SH region alleviate the high electric field at trench bottom and corners in the trench gate dielectric layer. A relative-heavily doped n CSL under the p-base region and part of the trench are adopted in both structures to alleviate the JFET effect. Compared with the Con-ATMOS, the proposed SGS-ATMOS features a source-connected SG under the trench gate as well as a schottky barrier (SB) metal inserted between the p-SH region and n CSL. The source-connected SG decouples the interaction between the drain and gate. Therefore, the C_{gd} as well as gate-drain charges (Q_{gd}) are dramatically reduced, which improves the switching speed and reduces the switching loss. The SB metal forms schottky contact with the n CSL. An integrated trench JBS diode is introduced with good double protection from the p-SH region and trench SG structure. The double protection mechanism of the integrated trench JBS diode reduces the high-temperature leak current

TABLE 1. Main parameters used in the simulation.

Parameter	SGS-ATMOS	Con-ATMOS
Cell width, W_{cell}	2.5μm	2.5μm
Trench width, W_{trench}	1μm	1μm
Trench depth, T_{trench}	1.15μm	1.15μm
Gate depth, T_g	0.6μm	1.1μm
Gate oxide thickness, T_{ox}	50nm	50nm
P-SH region thickness under trench, T_{ps}	0.4μm	0.4μm
P-SH region width under trench, W_{ps}	0.7μm	0.7μm
N- drift region thickness, T_d	12μm	12μm
N- drift region concentration, N_d	8.2×10^{15}cm^{-3}	8.2×10^{15}cm^{-3}
P-base width, W_{pb}	0.8μm	1μm
N CSL concentration, N_{CS}	2×10^{16}cm^{-3}	2×10^{16}cm^{-3}
N CSL thickness under trench, T_{CS}	0.4μm	0.4μm
Split gate thickness, T_{sg}	0.4μm	/
Split gate dielectric thickness, T_{sgdi}	100nm	/
SB metal depth, T_{SB}	1.15μm	/
Ohmic contact width of SB metal, W_o	0.2μm	/
Schottky contact width of SB metal, W_s	0.2μm	/
Work function of the SB metal, W_{fs}	5.1eV	/

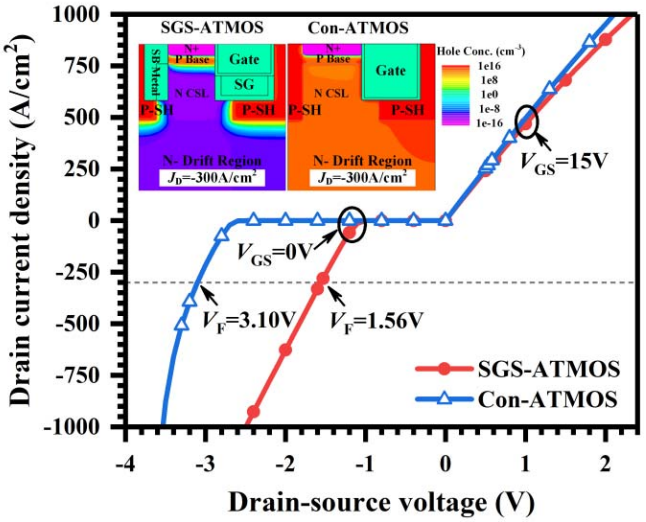

FIGURE 2. Forward and reverse conduction I-V characteristics for the SGS-ATMOS and Con-ATMOS, respectively. The inserted figures show the hole concentration distribution in the device surface in the diode conduction mode at $J_D = -300A/cm^2$.

(J_{lk}) at the blocking state, which is similar to that in our previous work [30]. Since the integrated trench JBS diode are formed mainly at the sidewall of the SB metal, it does not occupy additional chip area and will not increase the cell width of the SiC MOSFET.

Silvaco TCAD is used to simulate the characteristics of the SiC ATMOSs [35]. To simplify the simulation, the cell marked within the red dash line for the two structures are simulated. Similar to our previous work in [3], [6], [21], [30] and [36], Fermi-Dirac statistics is used in the simulation and models, such as band gap narrowing (BGN), incomplete ionization, FLDMOB, CONWELL, SURFMOB, CONSRH, Auger and analytic models are considered. 4H-SiC material is used and the main device parameters used in the simulation are listed in the Table 1. The work function of the SB metal used to form schottky contact is 5.1eV. If not specified in the following discussion, the device active region used is 1cm^2. To have a meaningful comparison, the device parameters not listed in the Table 1 are the same for the two structures.

III. RESULTS AND DISCUSSION

Fig. 2 shows the forward and reverse conduction I-V characteristics for the two devices. The forward and reverse I-V curves are obtained with gate-source voltage (V_{GS}) of 15V and 0V, respectively. SiO_2 is used as the gate and SG dielectric for the proposed SGS-ATMOS and Con-ATMOS. It can be seen that although the source-connected SG structure has a certain impact on the JFET resistance for the proposed device, the two devices still have comparable forward I-V characteristics. It also can be seen that contributed by the lower turn-on voltage of the integrated JBS diode, the forward conduction voltage drop (V_F) for the diode of the proposed SGS-ATMOS is only 1.56V, which is about half of 3.10V for the diode of the Con-ATMOS at drain current density (J_D) of -300A/cm^2. The inserted figures in the Fig. 2 show the surface hole concentration distribution in the diode conduction mode at $J_D = -300$A/cm^2 for the proposed SGS-ATMOS and Con-ATMOS, respectively. It is found that compared with the Con-ATMOS, the hole concentration at the drift region for the proposed SGS-ATMOS is extreme low. It indicates that the integrated JBS diode successfully bypasses the conduction of the PiN body diode. As a result, the proposed device not only has a low V_F in the diode conduction mode but also suppress the bipolar degradation effect appears in the PiN body diode for the Con-ATMOS.

Fig. 3(a) shows the blocking I-V characteristics for the two devices with same P-SH region width under trench (W_{ps}) of 0.7μm. It can be seen that the proposed SGS-ATMOS has a little bit higher BV_{av} than that of the Con-ATMOS. The BV_{av} is 1309V and 1232V for the proposed SGS-ATMOS and Con-ATMOS, respectively. Fig. 3(b) and Fig. 3(c) show the electric field distribution at BV_{av} for the proposed SGS-ATMOS and Con-ATMOS, respectively. It can be seen that although the two devices have comparable BV_{av}, the $E_{ox,max}$ for the Con-ATMOS is much higher than that of the proposed SGS-ATMOS. The $E_{ox,max}$ at BV_{av} is 2.32MV/cm and 3.26MV/cm for the proposed SGS-ATMOS and Con-ATMOS, respectively. Considering good long-time reliability, the higher $E_{ox,max}$ at BV_{av} for the Con-ATMOS shall induces gate oxide breakdown or degradation. Fig. 3(d) shows electric field distribution for the Con-ATMOS with $E_{ox,max}$=3MV/cm, where the V_{ds} is only 1018V. It can be concluded that since the SG with thicker T_{sgdi} for the proposed SGS-ATMOS relieves the electric

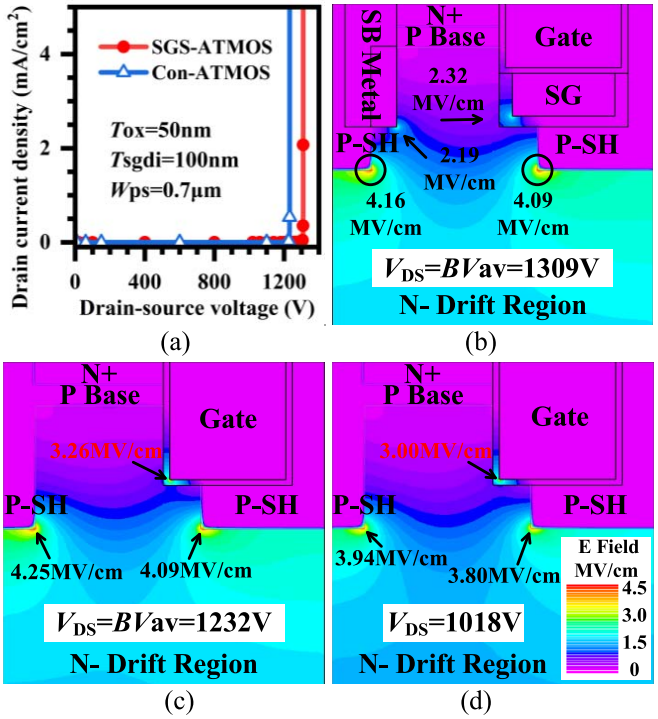

FIGURE 3. **(a) Blocking I-V characteristics for the two devices, (b) electric field distribution for the SGS-ATMOS at BV_{av}, (c) electric field distribution for the Con-ATMOS at BV_{av} and (d) electric field distribution for the Con-ATMOS with $E_{ox,max}$ = 3MV/cm, where the V_{DS} is only 1018V.**

field crowding in the dielectric layer at the trench corner, the limiting factor of breakdown is shifted from the gate oxide breakdown for the Con-ATMOS to the avalanche breakdown for the proposed SGS-ATMOS. As a result, the breakdown voltage (BV) is increased from 1018V of the Con-ATMOS to 1309V of the proposed SGS-ATMOS. Considering Baliga's figure of merit (BFOM, $BV^2/R_{on,sp}$), although the proposed SGS-ATMOS has a little bit higher $R_{on,sp}$, the BFOM is still increased from 5.23×10^8 W/cm^2 of the Con-ATMOS to 8.22×10^8 W/cm^2 of the proposed SGS- ATMOS. Compared with the Con-ATMOS, the BFOM for the proposed device is increased by 57.2% owing to the improved BV. The above results demonstrate that the proposed SGS-ATMOS has an improved static performance.

The device capacitance as a function of the drain-source voltage (V_{DS}) is shown in the Fig. 4. It can be seen that the C_{gd} and gate-source capacitance (C_{gs}) of the proposed SGS-ATMOS are smaller than those of the Con-ATMOS in the whole V_{DS} range. The C_{gd} and C_{gs} at the V_{DS} of 600V for the SGS-ATMOS are 4.31pF/cm^2 and 54.1nF/cm^2, respectively. At the same condition, the C_{gd} and C_{gs} are 60.8pF/cm^2 and 67.4nF/cm^2 for the Con-ATMOS, respectively. Compared with the Con-ATMOS, the C_{gd} and C_{gs} are reduced by 92.9% and 19.7% for the proposed SGS-ATMOS, respectively. Further investigation results show that the dramatically reduced C_{gd} and C_{gs} are derived from the reduced gate depth as well as decoupled interaction

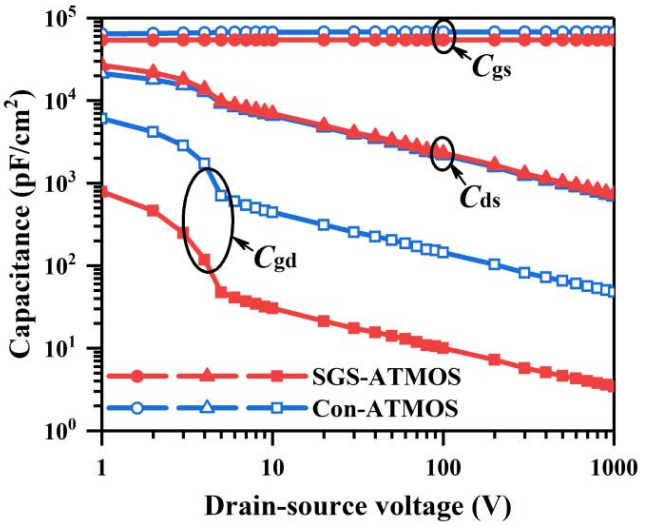

FIGURE 4. **Device capacitance as a function of the drain-source voltage.**

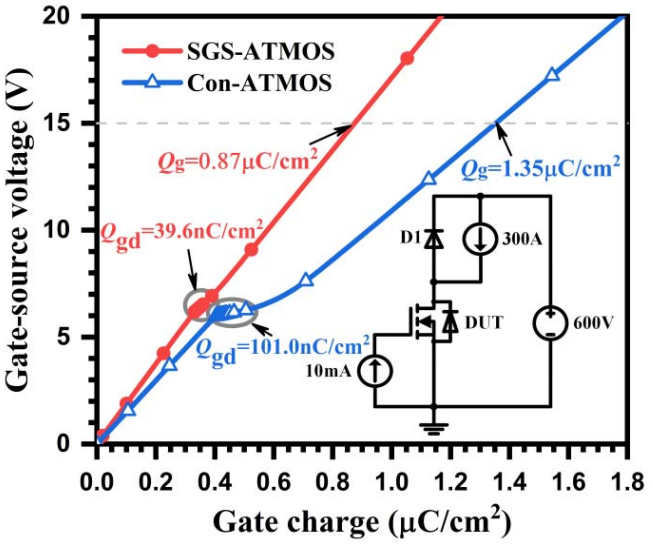

FIGURE 5. **Gate charges versus gate-source voltage for the two devices.**

between the gate and drain. It is contributed by the appearance of the source-connected SG structure. With the much smaller C_{gd}, the proposed SGS-ATMOS demonstrates superior high frequency figure of merit (HFFOM[1], $R_{on}\cdot C_{gd}$). The $R_{on}\cdot C_{gd}$ is reduced from 120.0mΩ·pF for the Con-ATMOS to 9.0mΩ·pF for the SGS-ATMOS. Compared with the Con-ATMOS, the HFFOM[1] ($R_{on}\cdot C_{gd}$) for the proposed SGS-ATMOS is reduced by 92.5%. For the drain-source capacitance (C_{ds}), the SGS-ATMOS has almost same C_{ds} as that of the Con-ATMOS. The obvious reduction of the C_{ds} and C_{gd} at V_{DS} of 2V-5V for the two devices is derived from the depletion of JFET region between the two p-SH regions. The gate charges (Q_g) versus the V_{GS} is also shown in Fig. 5. The inserted figure shows test circuit used in the simulation. It can be seen that the Q_g and Q_{gd} of the proposed SiC SGS-ATMOS are significantly reduced.

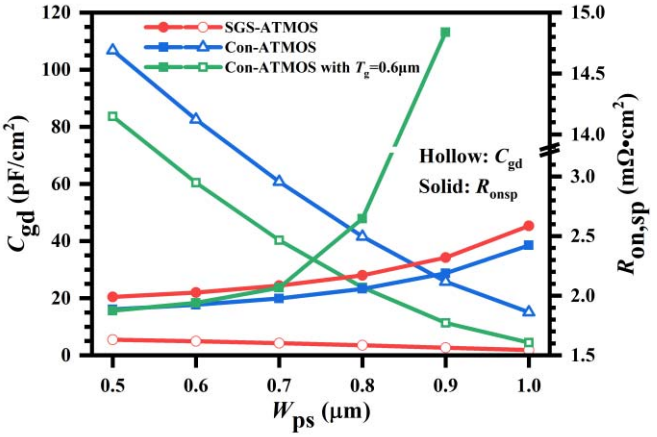

FIGURE 6. Influence of the W_{ps} on the C_{gd} and $R_{on,sp}$.

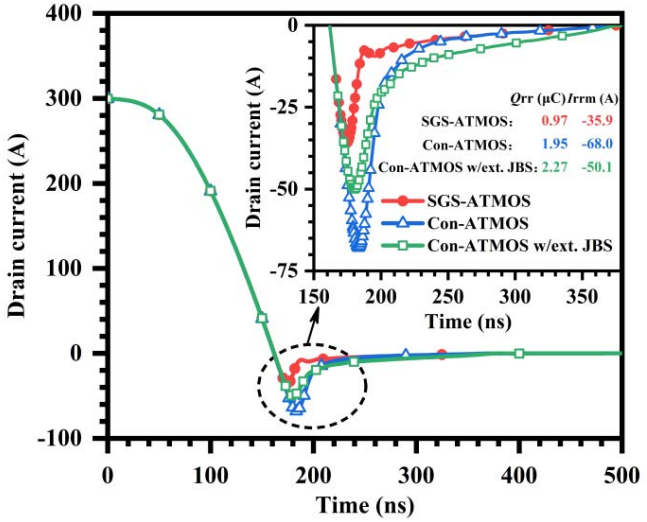

FIGURE 7. Reverse recovery waveforms for the diode of the SGS-ATMOS, Con-ATMOS and Con-ATMOS with external JBS diode.

Compared with 101.0nC/cm^2 for the Con-ATMOS, the Q_{gd} for the SGS-ATMOS is only 39.6nC/cm^2. Meanwhile, the total Q_g from $V_{GS} = 0$V to 15V is only 0.87μC/cm^2 for the SGS-ATMOS. While at the same condition, the total Q_g is 1.35μC/cm^2 for the Con-ATMOS. When it comes to another HFFOM (HFFOM^2, $R_{on} \cdot Q_{gd}$), the $R_{on} \cdot Q_{gd}$ is reduced from 200.0mΩ·nC for the Con-ATMOS to 82.5mΩ·nC for the SGS-ATMOS. Compared with the Con-ATMOS, the HFFOM^2 ($R_{on} \cdot Q_{gd}$) for the proposed SGS-ATMOS is reduced by 58.8%.

Fig. 6 shows the influence of the W_{ps} on the C_{gd} and $R_{on,sp}$ for the proposed SGS-ATMOS and Con-ATMOS, respectively. In order to have a meaningful comparison, the Con-ATMOS with a gate depth (T_g) of 0.6μm is also added in the figure. It can be seen that with the W_{ps} increases from 0.5μm to 1μm, the C_{gd} decreases significantly for the two Con-ATMOSs owing to the enhanced shielding effect provided by the source-connected P-SH region. Compared to the Con-ATMOS, the Con-ATMOS with the $T_g = 0.6$μm has lower C_{gd}, which derived from the smaller T_g. While for the proposed SGS-ATMOS, the C_{gd} decreases slightly with the W_{ps} increases from 0.5μm to 1μm since good shielding effect already provided by the SG structure in the whole range. With the W_{ps}=1μm, the C_{gd} at the V_{DS} of 600V is 1.88pF/cm^2, 15.1pF/cm^2 and 4.50pF /cm^2 for the proposed SGS-ATMOS, Con-ATMOS and Con-ATMOS with the $T_g = 0.6$μm, respectively. Compared to the two Con- ATMOSs, the proposed device shows much lower C_{gd} in the whole range. It also can be found that with the W_{ps} increases from 0.5μm to 1μm, the $R_{on,sp}$ increases for these three devices. For the Con-ATMOS with the $T_g = 0.6$μm, the $R_{on,sp}$ increases sharply after the W_{ps} larger than 0.7μm owing to the increased JFET effect. For the proposed SGS-ATMOS and Con-ATMOS, the increase of the $R_{on,sp}$ shows similar trend. With the $W_{ps} = 1$μm, the HFFOM^1 is reduced from 36.6mΩ·pF for the Con-ATMOS to 4.9mΩ·pF for the proposed SGS-ATMOS. With the much smaller C_{gd} and comparable $R_{on,sp}$, the proposed SGS-ATMOS demonstrates superior high frequency figure of merit.

Fig. 7 shows reverse recovery waveforms for the diode of the SGS-ATMOS and Con-ATMOS, respectively. In order to have a meaningful comparison, the reverse recovery waveform for the Con-ATMOS with external anti-parallel JBS diode is also shown in the figure. The active area for the external JBS diode is also 1cm^2. In the simulation, the forward conducting current (I_F) is 300A and the di_F/dt is kept same for all the diodes. It can be seen that the integrated JBS diode for the proposed SGS-ATMOS exhibits the best reverse recovery performance among these three devices. Without injection of the minority carrier, the diode reverse recovery charge (Q_{rr}) and peak reverse recovery current (I_{rrm}) are only 0.97μC/cm^2 and −35.9A for the proposed SGS-AMOS, which is 50.2% and 47.2% off compared with 1.95μC/cm^2 and −68.0A for the Con-ATMOS, respectively. For the Con-ATMOS with external JBS diode, the Q_{rr} and I_{rrm} are 2.27μC/cm^2 and -50.1A, respectively. It can be found that compared with the proposed SGS-ATMOS, although the external JBS diode can suppress the conduction of the PiN body diode, the larger capacitance induced by the additional JBS diode increases the Q_{rr} and I_{rrm}.

The gate and drain switching waveforms for the SGS-ATMOS, Con-ATMOS and Con-ATMOS with external JBS diode are shown in the Fig. 8 (a) and (b), respectively. The test circuits used in the simulation are shown in the Fig. 8(c). In each circuit, DUT1 and DUT2 are the same device and the active area for all the devices including external JBS diodes (D1 and D2) are 1cm^2. The gate voltage source (Vg) is turned on from 0V to 15V at t = 0μs and turned off from 15V to 0V at t = 10μs. It can be seen from the Fig. 8 (a) that the miller platform of the SGS-ATMOS is much shorter than that of the Con-ATMOS, which is aligned with the results indicated in the Fig. 5. It also can be seen

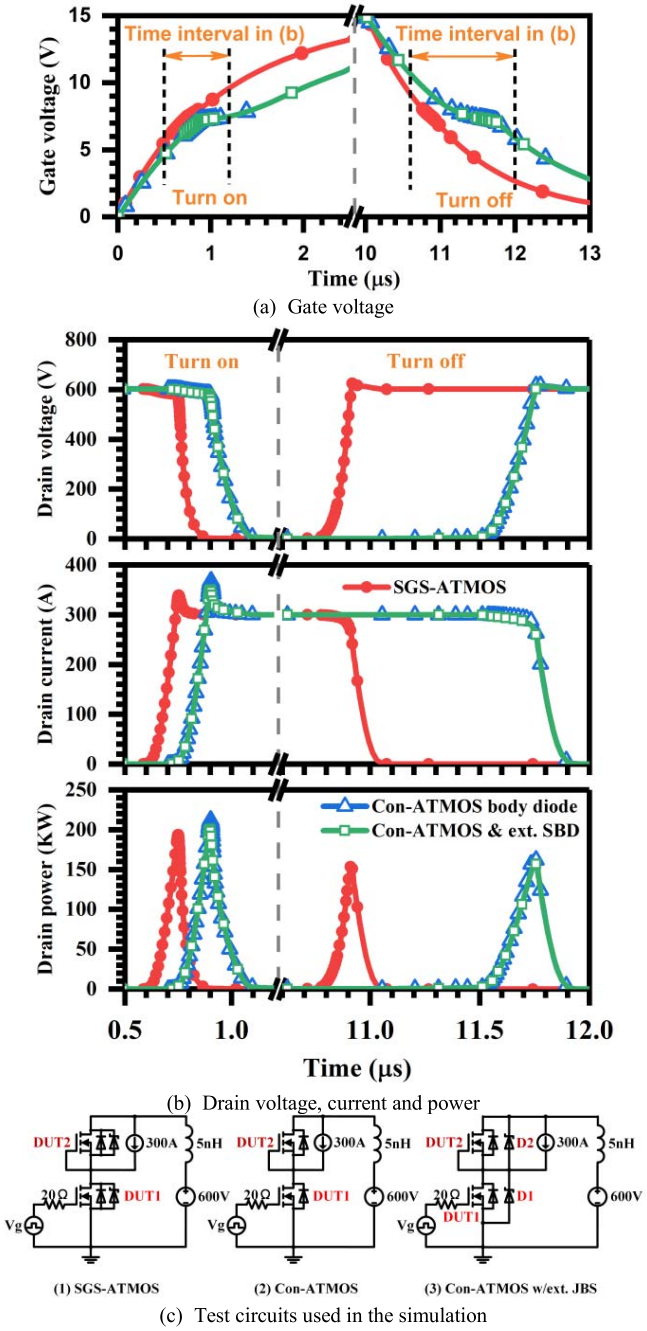

FIGURE 8. **Switching waveforms and test circuits used in the simulation: (a) gate voltage, (b) drain voltage, current and power and (c) test circuits.**

from Fig. 8 (a) and (b) that the switching speed of the SGS-ATMOS is much faster than those of the Con-ATMOS and Con-ATMOS with external JBS diode, which results in a much smaller switching loss. The turn-on loss (E_{on}) and turn-off loss (E_{off}) of the SGS-ATMOS are 16.4mJ/cm^2 and 17.7mJ/cm^2, respectively. The E_{on} and E_{off} are reduced by 33.3% and 33.0% when compared with 24.6mJ/cm^2 and 26.4mJ/cm^2 for the Con-ATMOS, respectively. Meanwhile, the E_{on} and E_{off} of the SGS-ATMOS are also 33.6% and 30.0% off compared with 24.7mJ/cm^2 and 25.3mJ/cm^2 for

TABLE 2. **Comparison of performance for the two devices.**

Parameter	SGS-ATMOS	Con-ATMOS
Specific on-state resistance, $R_{on,sp}$ (mΩ•cm^2)	2.08	1.98
Diode forward conduction voltage drop, V_F (V)	1.56	3.10
Breakdown voltage, BV (V)	1309	1018
Maximum electric field in oxide, $E_{ox,max}$ (MV/cm)	2.32	3.00
BFOM, $BV^2/R_{on,sp}$ (W/cm^2)	8.22×10^8	5.23×10^8
Gate-drain capacitance, $C_{gd,sp}$ (pF/cm^2)	4.31	60.8
Gate-source capacitance, $C_{gs,sp}$ (nF/cm^2)	54.1	67.4
HFFOM[1], R_{on}•C_{gd} (mΩ•pF)	9.0	120.0
Gate-drain charges, Q_{gd} (nC/cm^2)	39.6	101.0
Total gate charges, Q_g (μC/cm^2)	0.87	1.35
HFFOM[2], R_{on}•Q_{gd} (mΩ•nC)	82.5	200.0

*$R_{on,sp}$ is obtained at V_{GS}=15V and J_D=300A/cm^2 and V_F is obtained at V_{GS}=0V and J_D=-300A/cm^2.

TABLE 3. **Comparison of performance for the three devices.**

Parameter	SGS-ATMOS	Con-ATMOS	Con-ATMOS w/ext. JBS
Peak reverse recovery current, I_{rrm} (A)	-35.9	-68.0	-50.1
Reverse recovery charge, Q_{rr} (μC/cm^2)	0.97	1.95	2.27
Turn on loss, E_{on} (mJ/cm^2)	16.4	24.6	24.7
Turn off loss, E_{off} (mJ/cm^2)	17.7	26.4	25.3

the Con-ATMOS with external JBS diode, respectively. In addition, other than the smaller E_{on} and E_{off}, the turn-on and turn-off delay time are also much shorter for the proposed SiC SGS-ATMOS. Furthermore, the smaller Q_g for the proposed SGS-ATMOS also makes it easier to be driven, which reduces the requirement for the gate driver.

Tables 2 and 3 summarize the simulation results for the SGS-ATMOS and Con-ATMOS. The reverse recovery and switching performance for the Con-ATMOS with external anti-parallel JBS diode are also listed in the Table 3. The results indicate that the proposed SGS-ATMOS has superior performance when compared with the Con-ATMOS with and without external anti-parallel JBS diode.

The impact of the temperature (T) on the static I-V characteristics of the SGS-ATMOS are shown in Fig. 9. It can be seen that with increase of the temperature, the forward and reverse conduction I-V characteristics are degraded due to reduction of the mobility at higher temperature. The $R_{on,sp}$ increases from 2.08mΩ·cm^2 at T = 300K to 3.38mΩ·cm^2 and 5.21mΩ·cm^2 at T = 400K and T = 500K, respectively. The V_F of the integrated JBS diode increases from 1.56V at T = 300K to 1.81V and 2.20V at T = 400K and T = 500K, respectively. Although the positive temperature coefficient of $R_{on,sp}$ and V_F increases the conduction loss at high temperature, it can avoid forming local current filament in applications due to the negative feedback mechanism of heat and electricity, which makes the SGS-ATMOS reliable and suitable for parallel usage [37]. The J_{lk} in the blocking state increases on orders of magnitude when the

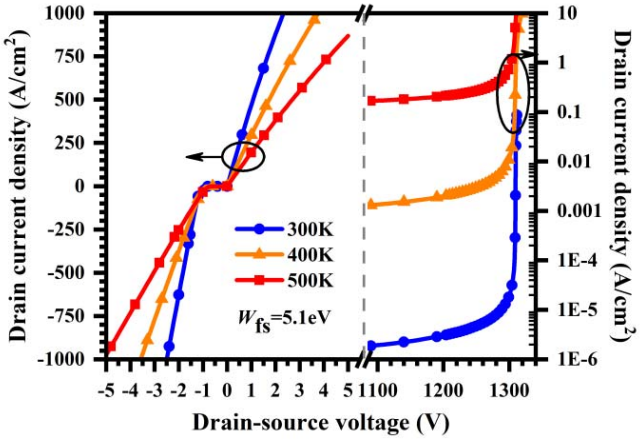

FIGURE 9. Impact of temperature on the static I-V characteristics of the SGS-ATMOS.

temperature increases from 300K to 500K. However, the increase of the J_{lk} is still acceptable since good double protection is formed for the integrated trench JBS diode. Further investigation results show that the $E_{ox,max}$ of the device is below 3MV/cm at different temperature and indicates the breakdown of the device is still avalanche breakdown.

To investigate the impact of the SG on the SGS-ATMOS, the relative permittivity (ε_{sgdi}) and thickness (T_{sgdi}) of the SG dielectric are varied to see how the device performance changes. In the discussion, the trench depth, gate depth as well as gate oxide thickness keep no change. The dependence of the device performance, such as capacitance (C_{gs}, C_{ds} and C_{gd}), $R_{on,sp}$ and HFFOM[1] ($R_{on} \cdot C_{gd}$) on the ε_{sgdi} with the $T_{sgdi} = 100$nm is shown in Fig. 10(a). It can be seen that with the ε_{sgdi} increases, the C_{gd} and R_{on} C_{gd} decrease significantly while the C_{gs}, C_{ds} and $R_{on,sp}$ increase slightly. The C_{gd} and HFFOM[1] ($R_{on} \cdot C_{gd}$) are reduced from 4.31pF/cm^2 and 9.00mΩ·pF to 1.81pF/cm^2 and 3.85 mΩ·pF when the ε_{sgdi} increases from 3.9 to 24, respectively. The decrease of the C_{gd} and HFFOM[1] ($R_{on} \cdot C_{gd}$) are induced by the enhanced shielding effect provided by the SG. Fig. 10(b) shows the impact of the T_{sgdi} on the device performance, such as capacitance (C_{gs}, C_{ds} and C_{gd}), $R_{on,sp}$ and HFFOM[1] ($R_{on} \cdot C_{gd}$) with the $\varepsilon_{sgdi} = 3.9$. It can be seen that the C_{gs}, C_{ds} and $R_{on,sp}$ decrease while the C_{gd} and $R_{on} \cdot C_{gd}$ increase as the T_{sgdi} increasing. The changing trends are all opposite to that shown in Fig. 10(a). The C_{gd} increases from 4.31pF/cm^2 to 9.92pF/cm^2 when the T_{sgdi} increases from 100nm to 300nm. The increase of the C_{gd} is induced by the weakened shielding effect provided by the SG with the thicker T_{sgdi}. However, the C_{gs} decreases 14.7% when T_{sgdi} increases from 100nm to 300nm. The reduction of the C_{gs} comes from the reduced overlap area between the gate and SG. The slightly reduced $R_{on,sp}$ comes from the enhanced impact of the gate on the JFET region when the T_{sgdi} increases from 100nm to 300nm, which increases the accumulation of the electron near the trench in the forward conduction state at the V_{GS} of 15V. It is found that adoption of the high-k

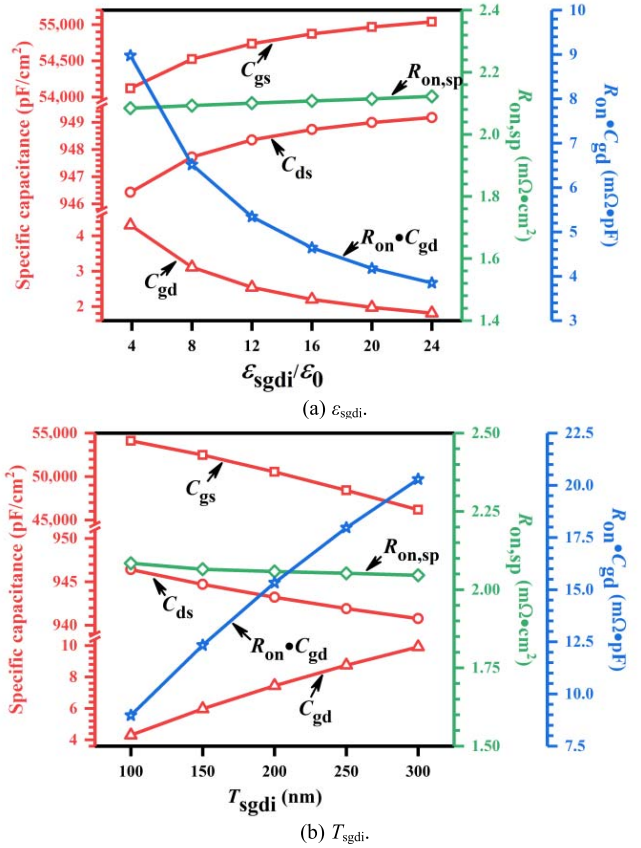

FIGURE 10. Impact of the ε_{sgdi} and T_{sgdi} on the device performance (a) ε_{sgdi} and (b) T_{sgdi}.

material or making the SG dielectric thinner is benefit for the reduction of the C_{gd} as well as HFFOM[1] ($R_{on} \cdot C_{gd}$), which is benefit to the improvement of the dynamic performance.

A brief fabrication process flow for the SiC SGS-ATMOS is proposed in Fig. 11. A 4H-SiC epitaxial material with n− epitaxial layer on n+ substrate is used as a starting material. Similar to the Con-ATMOS, the CSL, P base, N+ source and P-SH layer are formed via epitaxial growth and ion implantation, respectively. Compared with the Con-ATMOS, additional process steps are used to form the SG and schottky contact. The SG forming process for the SiC SGS-ATMOS is similar to that used for the Si SG-TMOS in our previous work [38], [39]. The SG is connected to source at the both ends of the trench strip via un-etched SG poly and metal via. Considering the lower temperature required to form schottky contact between the SB metal and n CSL, the SB metal is deposited and annealed after the formation of the backside and front side ohmic metals. The schottky contact process is similar to that used in [32]–[34] for 4H-SiC TMOS with an integrated JBS diode at the side wall of an additional source trench. Therefore, the additional process steps for the SG and schottky contact are fully compatible with the process flow of the SiC Con-ATMOS.

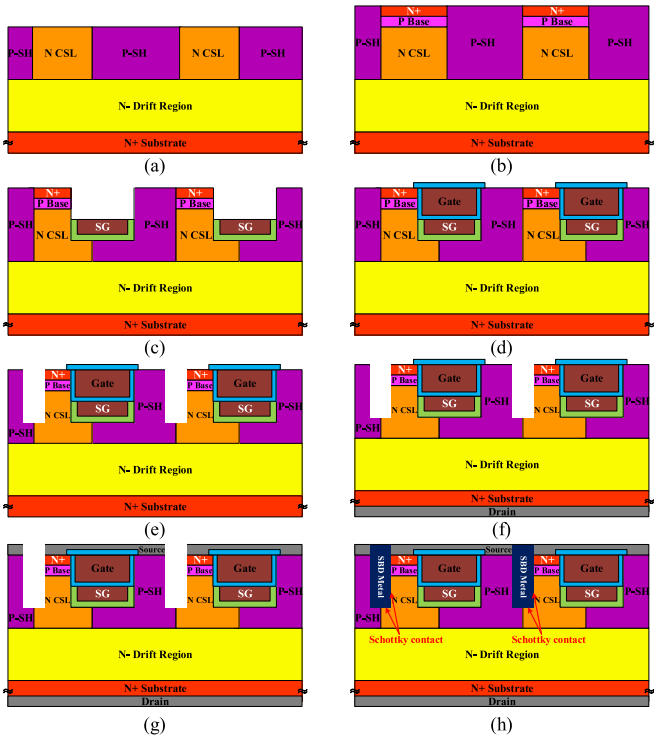

FIGURE 11. Proposed brief fabrication process flow for the 4H-SiC SGS-ATMOS. (a) epitaxial growth of the CSL and then formation of the first part of the P-SH layer via ion implantation, (b) epitaxial growth of the P base and N+ source layer successively and then formation of the second part of the P-SH layer via ion implantation, (c) etching the gate trench and then forming the SG (The SG is connected to source at the both ends of the trench strip via un-etched SG poly and metal via. The connection is not demonstrated in the figure), (d) forming the gate and isolation dielectric layer, (e) etching the SB metal trench, (f) forming the back side ohmic metal layer, (g) forming the front side ohmic metal layer and (h) forming the SB metal layer and then the top metal layer.

IV. CONCLUSION

A novel SiC SGS-ATMOS with SG and integrated trench JBS diode is proposed and analyzed in this paper. Compared with the SiC Con-ATMOS, the proposed SGS-ATMOS demonstrates excellent static and dynamic performance in both MOSFET and diode modes. The simulation results show that the BFOM for the proposed SGS-ATMOS and Con-ATMOS with same parameters are 8.22×10^8 W/cm^2 and 5.23×10^8 W/cm^2, respectively. Compared with the Con-ATMOS, the BFOM for the proposed device is improved by 57.2%. Meanwhile, compared with the Con-ATMOS, the C_{gd}, C_{gs}, Q_{gd} and Q_g are significantly reduced since the source-connected SG reduces the gate depth as well as decouples the interaction between the drain and gate. Compared with the Con-ATMOS, the HFFOM^1 ($R_{on}\cdot C_{gd}$) and HFFOM^2 ($R_{on}\cdot Q_{gd}$) for the proposed SGS- ATMOS are reduced by 92.5% and 58.8%, respectively. Contributed by the integrated trench JBS diode, the V_F, Q_{rr} and I_{rrm} of the diode are reduced from 3.10V, 1.95μC/cm^2 and −68.0A for the Con-ATMOS to 1.56V, 0.97μC/cm^2 and −35.9A for the proposed SGS-ATMOS at the J_D of −300A/cm^2, respectively. The E_{on} and E_{off} of the SGS-ATMOS are 16.4mJ/cm^2 and 17.7mJ/cm^2, which are 33.3% and 33.0% off compared with 24.6mJ/cm^2 and 26.4mJ/cm^2 for the Con-ATMOS, respectively. Meanwhile, the E_{on} and E_{off} of the SGS-ATMOS are also 33.6% and 30.0% off compared with 24.7mJ/cm^2 and 25.3mJ/cm^2 for the Con-ATMOS with external JBS diode, respectively. The temperature characteristics for the SGS-ATMOS are discussed and it is found that the proposed device exhibits good performance in high temperature and suitable for parallel usage. Finally, the dependence of the device performance on the SG dielectric parameters are also discussed for the SGS-ATMOS, which presents a further improvement direction for the proposed device.

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