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A novel single event upset hardened CMOS SRAM cell

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Abstract: This paper presents an improved design of a radiation-hardened static random access memory (SRAM). The simulation results based on the 0.18 μm standard digital CMOS technology show that its static current drops dramatically compared with the WHIT cell, and the write speed is equivalent to that of other cells. The memory cell is extremely tolerant to logic upset as it does not flip even for a transient pulse with 100 times the critical charge of the ROCK cell. According to these features, this novel cell suits high reliability applications, such as aerospace and military.

Keywords: single event-upset, radiation-hardened SRAM

Classification: Integrated circuits

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1 Introduction

To ensure the reliability of computational systems in space, electronic circuitry must be resilient when exposed to the flux of ionized particles. Semiconductor memories occupy large area in modern integrated circuits. A high

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energy charged particle may change the content of a memory cell when energetic particles (ions) strike the storage cell's sensitive node [1, 2]. Preventing such a single event upset (SEU) will be a great challenge to the designers of reliable space based systems. Moreover, the aggressive scaling of CMOS technology also suffers reliability of operation with respect to external circumstances. Due to the lower supply voltage and the smaller node capacitance, the amount of charge stored on storage nodes in SRAM cell is smaller, increasing the susceptibility of SEUs to particles. So designing hardened SRAM cells to SEU is a feasible way to progress towards technology scaling.

Many researchers have designed different radiation hardened SRAM cells against SEU [3, 4, 5]. Rockett proposed a SEU hardened CMOS SRAM cell by virtue of the latch design [3]. In the ROCK SRAM cell, transistors P1, P3, P4, and P6 (as shown in Fig. 1 (a)) provide the necessary control logic to the state-redundant devices. The WHIT hardened cell (Fig. 1 (b)) was presented later [4]. This RAM cell consists of two storage structures. The top half is constructed from p-channel devices while the bottom half consists solely of n-channel devices. The WHIT cell used two stable structures coupled to have obviously higher LETth than other two cells. One major drawback in the design is that due to the degraded voltage, none-negligible static power is consumed by the cell. Liu and Whitaker improved the cell by inserting complementary devices N6/N7(P6/P7) between the power supply $V_{DD}(V_{SS})$ and n-type(p-type) memory structure which is called the LIU cell (Fig. 1 (c)) [5]. Recently, a quad-node ten transistor (10T) SRAM cell has been proposed by Jahinuzzaman [6]. This cell offers differential read operation for easier design of the sense amplifier and reliable sense operation under the worst case conditions.

This paper presents an improved radiation hardened memory cell design that it combines the advantages of the ROCK cell and the WHIT cell to withstand higher intensities of single event upset without compromising on the performance.

2 Proposed SEU hardened SRAM cell design

The proposed SEU hardened SRAM cell is shown in Fig. 1 (d). The circuit consists of three storage structures and two of them each use a single type of transistors like the WHIT cell. The section using p-type can safely store 1's and the n-type section can safely store 0's. Transistors P1, P3, P4, P6 and N1, N3, N4, N6 constitute two stable structures to guarantee higher stability towards single event upset. Meanwhile, the circuit continues to have small static current and rail-to-rail outputs like the ROCK cell. The harden design concept uses the inactive and active (that is, OFF and ON) levels of the CK and CKb to load and off-load the state-redundant transistors (P2 and P6, N2 and N6). The state-redundant transistors prevent the high node discharging during single-event disturbances, thereby ensuring the cell doesn't change state.

Nodes Q and Qb, QP and QPb, QN and QNb store the data and the

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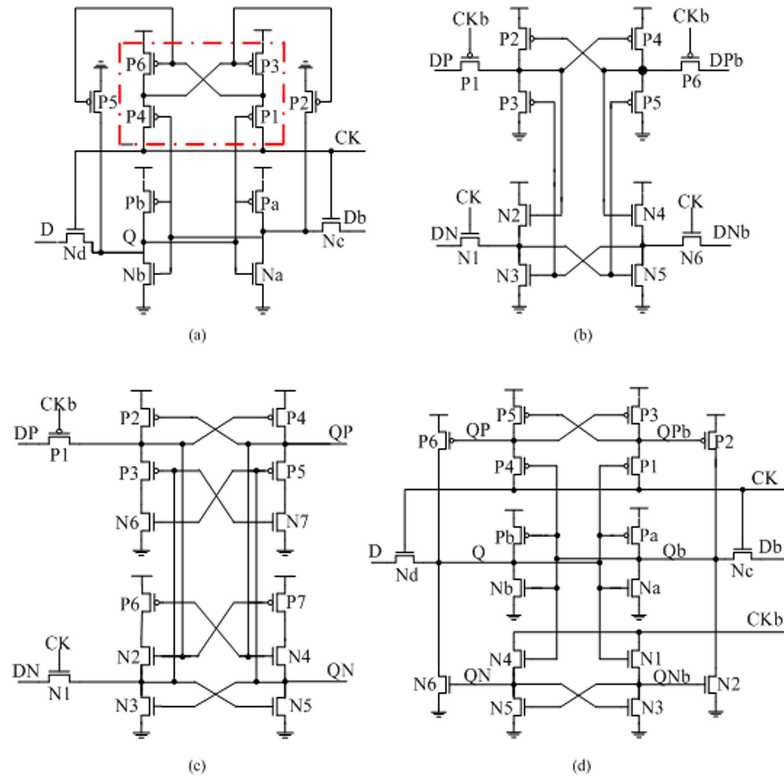

Fig. 1. (a) ROCK cell, (b) WHIT cell, (c) LIU cell, (d) Proposed radiation- hardened memory cell

logic states are complementary. To perform a write operation with a high data bit, the data D is transferred to the data node Q when the CK is pulsed logic high. Nodes QP, QPb, QN, QNb off-load the memory cell during the operation, thus avoid write speed degradation. After the write operation is performed, nodes QPb, Q, QNb are high, while nodes QP, Qb, QN are low. The SEU-sensitive nodes of the cell are the strongly reverse-biased p+ diffusion at nodes QP, Qb and the strongly reverse-biased n+ at nodes Q, QNb. The memory cell flips the data when collected charge exceeds the critical charge (Q_{crit}) that has been stored in these nodes, where the critical charge Q_{crit} is the minimum charge required to flip the data. We study the behavior of these four nodes during a single event upset and show how the effects are mitigated in the proposed improved design.

Case1-vulnerability of node QP: Node QP is critically vulnerable if the drain of the transistor P5 is struck. The excess charge will cause node QP to go high, momentarily turning P3 and P6 OFF. No change of the stored data state at nodes Qb, Q is involved. Node QP is eventually recharged low through P4(ON).

Case2- vulnerability of node Qb: Node Qb is vulnerable if the drain of the transistor Pa is struck, causing node Qb to potentially go high. The removal of charge from node Qb causes transistor N4 ON. In addition, the saturation current of N5 is greater than the saturation current of transistor N4 (Transistors N4 is sized to be weak compared with N5). This enable node QN keeps low. Meanwhile, the isolating node QNb keeps N2 turned ON,

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directing the excess charge to ground and pulls node Qb low to recovery.

Case3- vulnerability of node Q: Node Q is critically vulnerable if the drain of the transistor Nb is struck. The excess charge will cause node Q to go low and turning P1 ON. Since P3 has been designed to have a greater saturation current than transistor P1 (Transistors P1 is sized to be weak compared with P3), the voltage distribution in the P1-P3 conduction path keeps node QPb high. P6(ON) eventually pulls Q to the original high state.

Case4-vulnerability of node QNb: Node QNb is vulnerable if the drain of the transistor N3 is struck, causing node QNb to potentially go low, momentarily turning N2 and N5 OFF. No change of the stored data state at nodes Q, Qb is involved. Node QNb is eventually recharged high through N1(ON).

3 Simulation results and evaluation

The performance of the proposed cell is simulated in 0.18 μm standard digital CMOS technology by Cadence. As the device size shrinking, the SEU results of the scaled device are different. In order to shed light on the effect on scaled device, we choose smaller read-write transistors as gate width W=0.22 μm and gate length L=0.18 μm. First we checked that reading and writing was proper and then we simulated the SEUs. Since the write-time is longer than the read-time, only the write-time is analyzed here. Initially, Q is in a high state and Qb is in a low state. When t=10 ns, a low state is written to Q and a high state is written to Qb and when t=12 ns, the single-event hit is simulated. The current pulse that results from a particle strike is traditionally described as a double exponential function [1] as follows:

$$I(t) = \frac{Q}{\tau_\alpha - \tau_\beta} \cdot (e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) \quad (1)$$

Where Q is the amount of charge deposited as a result of the ion strike, while τ_α is the collection time constant for the junction and τ_β is the ion track establishment constant. Here τ_α is set as 45 ps and τ_β is set as 145 ps [7].

SEU at the drain of an NMOS is modeled as an outgoing exponential current pulse and incoming current pulse in case of PMOS. The voltage waveforms at various internal nodes when SEU strikes transistor Nb are shown in Fig. 2 (a). In order to have an effective comparison with previous designs, here we choose Q=0.7 pC. There is a 2.6 Volts bump (1.8 to around −0.8 Volts) at Q where SEU strikes, but that causes only 0.7 V spike at QPb and no perceptible change at Qb and QNb. Next, we give the simulation results for SEU strike at Pa in Fig. 2 (b). There is 2.7 Volts bump at the point where SEU strikes (Qb) and less than 0.6 Volts at Q. Simulation results show that after less than 1 nanosecond, the node voltage recover to initial state and stored data don't lost.

Fig. 2 (c) shows the response of the proposed cell when it is subjected to a SEU hit to the high data node which, in this case, is node Q. The amount of charge that can be collected at Q sweep from 71.4 pC to 71.7 pC and the interval is 0.1 pC, because this interval will not introduce large errors compared to the order of magnitude. Due to 71.6 pC, charge cannot flip

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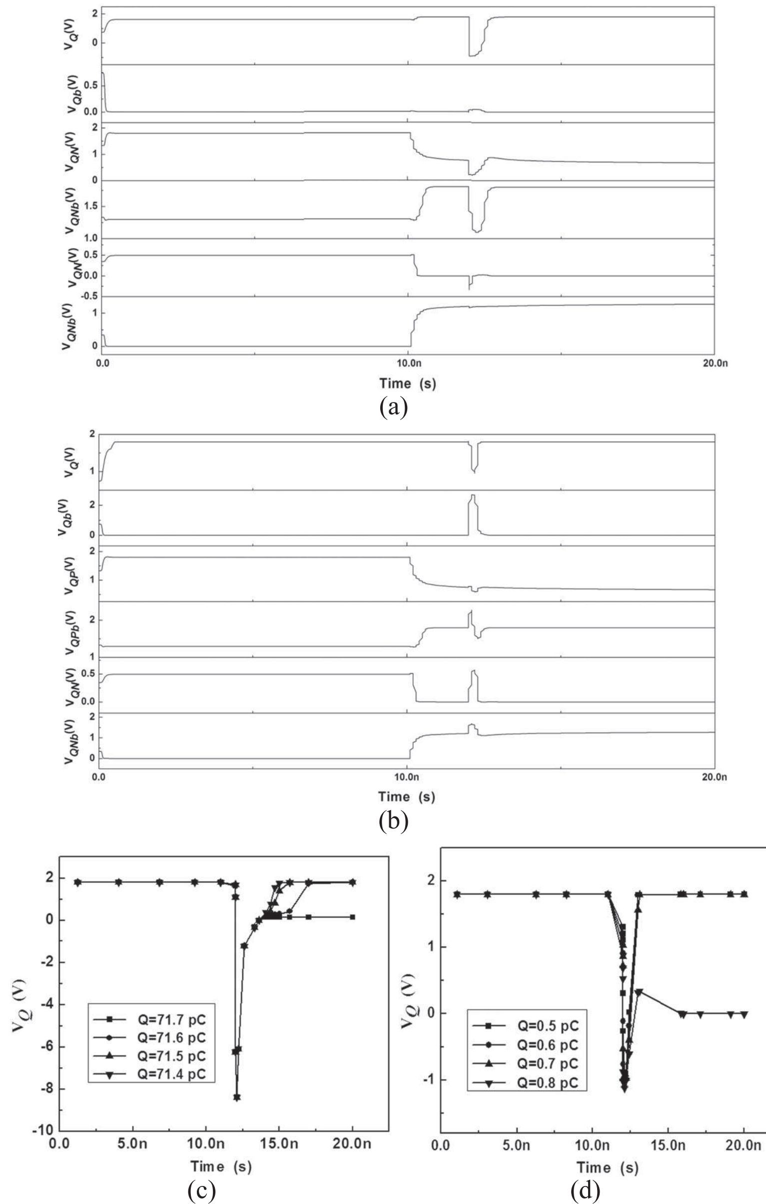

Fig. 2. Write cycle response time when subjected to single radiation strike at t=12 ns, (a) Voltage response when the drain of the transistor Nb is struck, (b) Voltage response when the drain of the transistor Pa is struck, (c) V_Q in the proposed cell versus different collected charge, (d) V_Q in the ROCK cell versus different llected charge

the cell, but 71.7 pC charge flips the cell, so the critical charge Qcrit of this memory cell is 71.7 pC. Similar simulations of the ROCK cell were performed and are shown in Fig. 2 (d). From this figure, the ROCK cell's Qcrit is 0.8 pC, drops dramatically compared with the proposed cell.

The performance of the proposed memory cell is compared with the ROCK cell, the WHIT cell and the LIU cell and JAH's cell proposed in [6]. The comparative parameters include Qcrit, write time, recovery time and

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Table I. Comparison of six types of SEU immune SRAM cells

Features	General 6T cell	ROCK cell [3]	WHIT cell [4]	LIU cell[5]	JAH cell [6]	Proposed cell
Qcrit (pC)	0.008	0.8	2	2	0.028	71.7
Write time (ns)	0.3	0.8	0.35	0.35	0.32	0.6
Recovery time (ns)	-	0.96	1.61	1.47	-	0.51
Static Power(nW)	5.4	21.2	14500	6.8	9.3	37.4
Dynamic Power(μW)	47.5	222.17	92.4	102.6	68.24	254.06
Area(μm^2)	3.35	6.13	5.96	7.27	4.68	9.92

static current. The write time is the time interval defined from the midpoint of the rising edge of an activated write clock pulse to the midpoint of the rising edge of the feed-forward response of the latch node. The recovery time is measured from peak voltage to 0.9volts level with 0.7 pC depositing on a vulnerable node. Table I shows the results of the circuit simulation. The write speed is equivalent to that of the other cells and the static power of the proposed cell drops dramatically compared with the WHIT cell. The dynamic power dissipation of the proposed cell is the highest due to the large capacitance of nodes Q and Qb and two wordline (CK/CKb) are connected to the source diffusion of P1, P4, N1 and N4. The area consumption is about 3 times of the general 6T cell. Nevertheless, the most remarkable progress is that Qcrit is absolutely higher than the other five cells, especially 100 times of the ROCK cell. Such high energy fluxes of ionizing particles may cause hard damages of the cell. On the other hand, the simulation result can show that the cell has a prominent characteristic of resisting the soft errors caused by single event upsets. Thus, the proposed cell can be used for some special application circumstance in which reliability is very important.

4 Conclusion

In this paper, an improved design of a SRAM cell is proposed. It combines the advantages of the ROCK cell and the WHIT cell to withstand higher intensities of single event upset. Circuit simulation results show that the cell is highly robust from the effects of radiation causing single-event upset. The memory cell is extremely tolerant to logic upset as it does not flip even for a transient pulse with 100 times the Qcrit of the ROCK cell. The read/write-time of the cell is less than 1 ns, making it suitable for reliable high-performance applications.

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