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A Novel Single Phase Synchronous Reference Frame Phase-Locked Loop with a Constant Zero Orthogonal Component

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Abstract

A novel single phase Phase-Locked Loop (PLL) is proposed in this paper to accurately and rapidly estimate the instantaneous phase angle of a grid. A conjugate rotating vector pair is proposed and defined to synthesize the single phase signal in the stationary reference frame. With this concept, the proposed PLL innovatively sets one phase input of the PARK transformation to a constant zero. By means of a proper cancellation, a zero steady state phase angle estimation error can be achieved, even under magnitude and frequency variations. The proposed PLL structure is presented together with guidelines for parameters adjustment. The performance of the proposed PLL is verified by comprehensive experiments. Satisfactory phase angle estimation can be achieved within one input signal cycle, and the estimation error can be totally eliminated in four input cycles for the most severe conditions.

Key words: Conjugate rotating vector pair, Phase-locked loop, Single phase phase-locked loop, Synchronization

I. INTRODUCTION

Due to the popularity and wide acceptance of distributed generation systems, the last decade has become an explosive period for grid-connected power electronics converter research [1]. A variety of converter topologies have been proposed and well-studied. Later, different control methods were proposed [2], [3]. In addition, a variety of applications for three phase grid-connected power electronics converters and single phase grid-connected power electronics converters have become standard configuration in many applications, such as photovoltaics, UPSs, energy storage technologies, aerospace applications and FACTS [4]-[9]. In such systems, the control performance is greatly dependent on accurate grid information [5], [7], [9]. Both phase and magnitude have been used to generate references for the converters output, for example, the current command. Phase information has also been utilized to transform particular state variables into the synchronous reference frame [10], [11]. Islanding detection can be achieved by monitoring the grid frequency [12], [13]. Therefore, the grid synchronization method is a key method for the control of grid-connected power converters.

A lot of work has already been done on this topic. Zero-crossing point detection suffers from low dynamic transients and sensitivity to jitters at around the zero-crossing point. The Discrete Fourier Transformation (DFT) requires more computational resources, and it also features a one-cycle detection delay [14]. Among all the exiting synchronization methods, the Phase-Locked Loop is the most widely accepted method.

Different types of single phase PLLs have been proposed in the literature. They are usually constructed in terms of structure by the Phase Detector (PD), Loop Filter (LF) and Voltage Controlled Oscillator (VCO). Most creative work on PLL research focused on new PDs. The original PLL used a mixer as the PD [15]. However, multiplication generates an undesired ripple simultaneously at twice the input frequency under the phase locked state. This ripple contaminates the phase angle estimation, and further influences the output of the grid-connected converter. Therefore, either a Low Pass Filter (LPF) or a reduced bandwidth LF has to be implemented to guarantee the phase angle estimation accuracy [8], [16]. A Modified Mixer PD is proposed to reduce such a ripple, but accurate phase angle estimation can only be achieved within a limited input magnitude range around unity value [17].

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In three phase systems, synchronous rotating transformation is widely used in control and phase angle estimations [18]-[20]. These PLLs are referred to as Synchronous Reference Frame PLL (SRF-PLL). This transformation is also adopted in single phase grid-connected converter control and PLLs. Many single phase SRF-PLLs have been proposed with a synchronous rotating transformation PD, referred to as the PARK PD [18]. These PLLs generate a clean phase angle estimation during the phase-locked state. However, the sole source of information sensed at the input makes the PARK PD unable to be implemented directly in single phase PLLs. Almost all the proposed methods focused on the generation of the required signal, which is orthogonal to the input. This process is also called Quadrature Signal Generation (QSG). Transport delay [21], differentiation [11] and certain kinds of filters [22]-[25] can be used for QSG. However, the transport delay QSG introduced an inevitable undesired delay. The differentiation QSG amplifies the noise of the input. Filtering the input can also generate an orthogonal signal without delay, and additional attenuation of the undesired harmonics can be also achieved. However, such QSG methods are not frequency-adaptive. In order to be frequency-adaptive, an additional frequency loop is required.

A single phase SRF-PLL which does not equip QSG has also been proposed. This type of SRF-PLL sets the orthogonal signal as zero constantly [14], [26]. Although it is declared in [14] that it sets a constant zero orthogonal signal, the cascaded delay signal cancellation operators in the stationary reference frame generates two signals in orthogonal for the PARK PD.

It can be concluded from all of the single phase PLLs in the literature that, the single phase PLL with a mixer PD is inherently frequency-adaptive. However, accurate phase angle estimation is hard to obtain. Accurate phase angle estimation can be achieved by single phase SRF-PLLs, but frequency-adaptive phase angle estimation requires an additional frequency-locked loop. The removal of QSG from a single phase SRF-PLL is novel but not fully achieved in the literature. In this paper, a novel single phase PLL is proposed to achieve both accurate phase angle estimation and inherent frequency-adaption without QSG.

This paper is organized as follows. In section II, the conjugate rotating vector pair is defined and described to synthesize a single phase signal. In section III, a novel single phase SRF-PLL is proposed and presented. The design issues in the proposed PLL are discussed in detail with both mathematical analysis and numeric simulation. In section IV, a comprehensive experiment verified the static and dynamic performances of the proposed PLL. The paper is concluded in Section V.

II. Synthesis of a Single Phase Signal

Fig. 1 shows a commonly used power converter along with the related control systems for single-phase grid-connected applications. The PLL is used to estimate the line voltage phase angle, or the voltage angle at the point of common connection. It has to be mentioned that the PLL estimates the line current phase angle in series connected converters, such as the distributed series compensator. Therefore, the PLL estimates either the voltage or current phase angle, depending on the application. In this paper, the variables are represented by u for example.

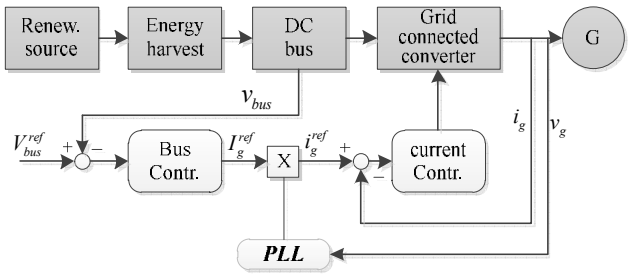


Fig. 1. Common single phase distributed generation system.

In the well-known stationary reference frame, a pulsing vector can be generated by setting the value of the α-axis as the single phase signal, and by setting the value of the β-axis as zero constantly. In this case, the single phase signal is expressed in (1). The end of the pulsing vector is on the α-axis, and it moves back and forth within the range of $\alpha \in [-A, A]$. The vector can be represented mathematically in (3).

$$u_i(t) = A \cdot \cos(\theta(t)) \tag{1}$$

Where:

$$\theta(t) = \int_0^t \omega(t)\mathrm{d}t + \theta(0) \tag{2}$$

$$\begin{cases} \alpha = A \cdot \cos(\theta(t)) \\ \beta = 0 \end{cases} \tag{3}$$

It is straight forward that such a pulsing vector can be synthesized by two rotating vectors, which are called rotating vector pairs. They are referred to as the positive rotating vector $\vec{U}^+$ and the negative rotating vector $\vec{U}^-$. If these two vectors are represented as (4) and (5), the relations within (3), (4) and (5) can be easily obtained as follows: $A^+ = A^- = 0.5 \cdot A$, $\theta^+(t) = \theta(t)$, and $\theta^-(t) = -\theta(t)$. This means that the magnitude of the rotating vector pair is the same as half of the input signal magnitude, and the phase angle with respect to the α-axis is opposite. This rotating vector pair is defined as cconjugate rrotating vector pair. A vector synthesis diagram is shown in Fig. 2. The synthesized input vector is also plotted.

$$\vec{U}^+ : \begin{cases} \alpha^+ = A^+ \cdot \cos(\theta^+(t)) \\ \beta^+ = A^+ \cdot \sin(\theta^+(t)) \end{cases} \tag{4}$$

$$\vec{U}^- : \begin{cases} \alpha^- = A^- \cdot \cos(\theta^-(t)) \\ \beta^- = A^- \cdot \sin(\theta^-(t)) \end{cases} \tag{5}$$

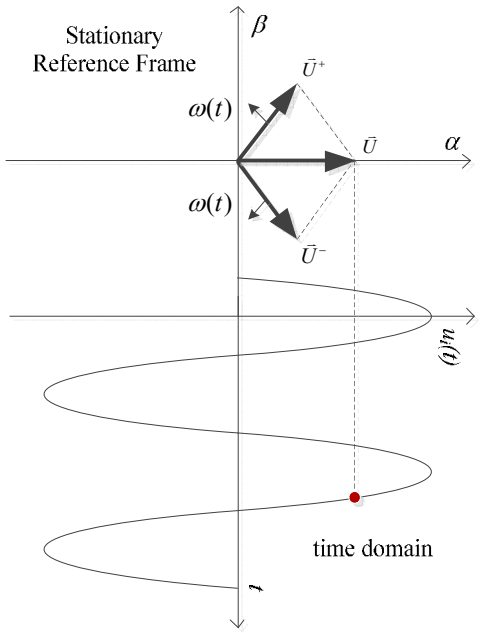


Fig. 2. Vector synthesis with Conjugate Rotating Vector Pair and time domain representation.

It should be noted that the positive rotating vector carries the instantaneous phase angle information of the single phase signal. The phase angle estimation of the single phase signal can be achieved by suitably obtaining the angle between the positive rotating vector and the α-axis.

In addition, as shown in (2), the frequency is not limited at a unique constant. All of the frequency components in $u_i(t)$ can be synthesized by a series of rotating vector pairs. It should be mentioned that the DC component in $u_i(t)$ cannot be synthesized by the sum of a rotating vector pair. It can be synthesized by the static vector pair shown in (7) and (8), while the DC component in $u_i(t)$ is represented in (6). In this way, any single phase signal can be synthesized by a series of conjugate rotating vector pairs.

$$u_{i0}(t) = A_0 \cos(\theta_0(0)) \tag{6}$$

$$\begin{cases} \alpha_0^+ = 0.5 \cdot A_0 \cdot \cos(\theta_0(0)) \\ \beta_0^+ = 0.5 \cdot A_0 \cdot \sin(\theta_0(0)) \end{cases} \tag{7}$$

$$\begin{cases} \alpha_0^- = 0.5 \cdot A_0 \cdot \cos(-\theta_0(0)) \\ \beta_0^- = 0.5 \cdot A_0 \cdot \sin(-\theta_0(0)) \end{cases} \tag{8}$$

III. The Proposed PLL

A. Description

In order to simplify the following analysis, the input single phase signal is redefined in (9). Harmonics are not considered for the sake of simplicity. By using the PARK transformation rotating at the estimated phase angle $\theta_e(t)$, the d-axis and q-axis output can be found in (10), after setting u_i as α, and maintaining the β at zero. In this case, the PARK transformation rotating at $\theta_e(t)$ is defined as (11).

$$u_i = 2 \cdot A \cdot \cos(\theta_1(t)) \tag{9}$$

$$\begin{bmatrix} d \\ q \end{bmatrix} = A \cdot \begin{bmatrix} \cos(\theta_1(t) - \theta_e(t)) \\ \sin(\theta_1(t) - \theta_e(t)) \end{bmatrix} + A \cdot \begin{bmatrix} \cos(-\theta_1(t) - \theta_e(t)) \\ \sin(-\theta_1(t) - \theta_e(t)) \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} d \\ q \end{bmatrix} = T_{PARK}(\theta_e(t)) \cdot \begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} \cos\theta_e(t) & \sin\theta_e(t) \\ -\sin\theta_e(t) & \cos\theta_e(t) \end{bmatrix} \cdot \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \tag{11}$$

It is noted from (10) that the first term of the q-axis output carries the phase angle error between the input signal and the phase angle estimation. It is supposed that the error is well controlled by a certain feedback mechanism and that the error goes to zero. This means that $\theta_e(t) \approx \theta_1(t)$. Under this phase-locked state, the d-axis and q-axis outputs are shown in (12).

$$\begin{bmatrix} d \\ q \end{bmatrix} = A \cdot \begin{bmatrix} \cos(\varepsilon) \\ \sin(\varepsilon) \end{bmatrix} + A \cdot \begin{bmatrix} \cos(-2 \cdot \theta_e(t) - \varepsilon) \\ \sin(-2 \cdot \theta_e(t) - \varepsilon) \end{bmatrix} \tag{12}$$

Where, ε is a small value, i.e. nearly zero, and it is expressed in (13).

$$\varepsilon = \theta_1(t) - \theta_e(t) \tag{13}$$

It can be stated from (12) that under phase lock, the d-axis output consists of a DC component and a second order AC component. The DC component is nearly half of the input magnitude, and the magnitude of the second order AC component is also half of the input. Corresponding to the cconjugate rotating vector pair, it is true that the projection of one vector became a DC quantity in the SRF synchronous to it, and the other is kept rotating in that SRF at twice the angular frequency. The module of the vectors is unchanged and they are still equal to each other in that SRF. By making use of this characteristic, the AC components in (12) can be expressed as (14). In other words, the AC components can be obtained by a proper transformation of the DC components in (12). The 2x2 matrix in (15) is just the PARK transformation matrix with a rotating phase angle of $2 \cdot \theta_e(t)$.

$$\begin{aligned} A \cdot \begin{bmatrix} \cos(-2 \cdot \theta_e(t) - \varepsilon) \\ \sin(-2 \cdot \theta_e(t) - \varepsilon) \end{bmatrix} &= A \cdot \begin{bmatrix} \cos(2 \cdot \theta_e(t) + \varepsilon) \\ -\sin(2 \cdot \theta_e(t) + \varepsilon) \end{bmatrix} \\ &= A \cdot \begin{bmatrix} \cos(2 \cdot \theta_e(t)) & \sin(2 \cdot \theta_e(t)) \\ -\sin(2 \cdot \theta_e(t)) & \cos(2 \cdot \theta_e(t)) \end{bmatrix} \cdot \begin{bmatrix} \cos(\varepsilon) \\ -\sin(\varepsilon) \end{bmatrix} \end{aligned} \tag{14}$$

In this way, (10) can be rewritten as (15). (15) indicates that the second order AC component in (10) can be cancelled by a certain feedback of the PARK transformation of the DC component in (10) at twice the estimated phase angle.

$$\begin{aligned} \begin{bmatrix} d \\ q \end{bmatrix} &= A \cdot \begin{bmatrix} \cos(\theta_1(t) - \theta_e(t)) \\ \sin(\theta_1(t) - \theta_e(t)) \end{bmatrix} \\ &+ A \cdot T_{PARK}(2 \cdot \theta_e(t)) \cdot \begin{bmatrix} \cos(\theta_1(t) - \theta_e(t)) \\ -\sin(\theta_1(t) - \theta_e(t)) \end{bmatrix} \end{aligned} \tag{15}$$

The derived PLL is presented in Fig. 3. The outputs of the proposed PLL are the phase angle estimation, the frequency estimation and the magnitude estimation. The frequency

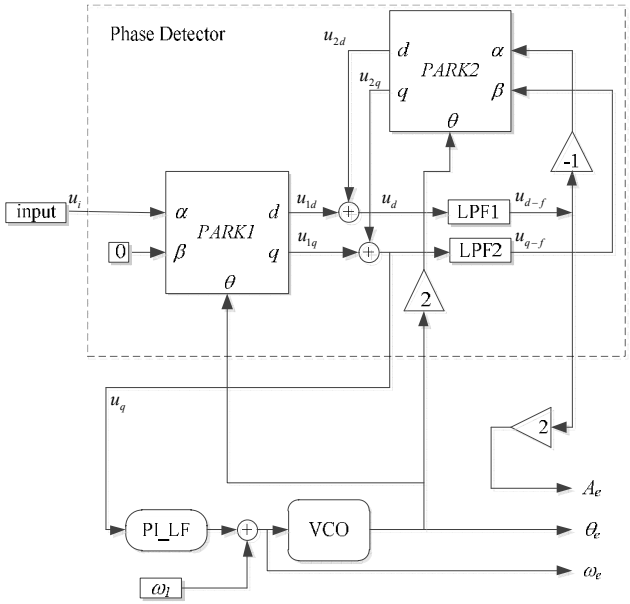


Fig. 3. Structure of the proposed PLL.

estimation is a useful state variable which can be a measure of the PLL dynamics.

The PD can be seen inside the dashed box in Fig. 3. It contains 2 PRAK transformation blocks (i.e. PARK1 and PARK2), 2 identical low pass filters, 2 adders and 2 gains. The single phase input is set as the α-input of PARK1, and the β-input of PARK1 is kept at a constant zero. The estimated phase angle is fed back to PARK1 to accomplish the rotating transformation. The outputs of PARK1 are then added to the outputs of PARK2. The sums (i.e. u_d and u_q) are filtered by LPF1 and LPF2 to obtain their DC components, as shown in (10). The filtered u_d and u_q are then served as the input of PARK2, which is rotating at $2\cdot\theta_e(t)$. These procedures accomplished the extraction of the DC components in (10) by means of a kind of feedback instead of a simple filtering.

The rest of the parts of the proposed PLL are same as those of a conventional PLL. The output of PD u_q is fed to the PI-type LP to obtain an accurate phase angle estimation. In addition, the filtered u_d, which carries the magnitude information of the input, is used to estimate the magnitude of the input with a gain of 2.

There are only two blocks to be designed in the proposed PLL. The design issues will be discussed in the following parts. It has to be mentioned that there are two LPFs in the proposed PLL. However, they are not responsible to the attenuation of the characteristic ripple created by the negative rotating vector. Consequently, simple first-order LPFs are well suited to this purpose.

B. Phase Detector Evaluation

It is well known that most PLLs differ from the PD, and the proposed PLL is not different. Hence, the dynamic and static behavior of the PD is very important for the PLL performance. The PD of the proposed PLL is indicated by the dashed box in Fig. 3. It is obvious that the PD behavior depends largely on the LPFs. Since a first-order LPF can serve this purpose satisfactorily, it can be said that the cut-off frequency is dominant in the PD performance.

In order to simplify the analysis, PARK1 is constantly rotating at ω_1 rad/s. In addition, the cut-off frequency ω_c is selected so that is it proportional to ω_1 with the coefficient k. The transfer function of the LPF is expressed in (16), using the variables of LPF1 for example.

$$\frac{U_{d-f}(s)}{U_d(s)}=\frac{\omega_c}{s+\omega_c} \tag{16}$$

Where:

$$\omega_c = k\cdot\omega_1 \tag{17}$$

Because two PARK transformations are included in the PD, it is hard to derive the transfer function in the s-domain. Therefore, the LPF is expressed in the time domain as (18).

$$\frac{du_{d-f}(t)}{dt}=\omega_c\cdot[u_d(t)-u_{d-f}(t)] \tag{18}$$

Based on (18), the relations of LPF1 and LPF2 can be derived and written in matrix (19).

$$\begin{bmatrix}\frac{\mathrm{d}u_{d-f}}{\mathrm{d}t}\\ \frac{\mathrm{d}u_{q-f}}{\mathrm{d}t}\end{bmatrix}=\omega_c\cdot\begin{bmatrix}u_d-u_{d-f}\\ u_q-u_{q-f}\end{bmatrix} \tag{19}$$

The computation of the two sums in Fig. 3 is written in (20), and PARK2's output is expressed in (21).

$$\begin{bmatrix}u_d\\ u_q\end{bmatrix}=\begin{bmatrix}u_{1d}+u_{2d}\\ u_{1q}+u_{2q}\end{bmatrix} \tag{20}$$

$$\begin{aligned}\begin{bmatrix}u_{2d}\\ u_{2q}\end{bmatrix}&=\begin{bmatrix}\cos2\theta & \sin2\theta\\ -\sin2\theta & \cos2\theta\end{bmatrix}\cdot\begin{bmatrix}-u_{d-f}\\ u_{q-f}\end{bmatrix}\\&=\begin{bmatrix}-u_{d-f}\cdot\cos2\theta+u_{q-f}\cdot\sin2\theta\\ u_{d-f}\cdot\sin2\theta+u_{q-f}\cdot\cos2\theta\end{bmatrix}\end{aligned} \tag{21}$$

In addition, u_{1d} and u_{1q} are the PARK transformation outputs of the single phase input. For the sake of simplicity, its phase angle is assumed to be θ, and the PARK1 outputs are expressed in (22).

$$\begin{aligned}\begin{bmatrix}u_{1d}\\ u_{1q}\end{bmatrix}&=\begin{bmatrix}\cos\theta & \sin\theta\\ -\sin\theta & \cos\theta\end{bmatrix}\cdot\begin{bmatrix}2\cdot A\cdot\cos\theta\\ 0\end{bmatrix}\\&=A\cdot\begin{bmatrix}1+\cos2\theta\\ -\sin2\theta\end{bmatrix}\end{aligned} \tag{22}$$

From (19)-(22), the following differential equations model can be written:

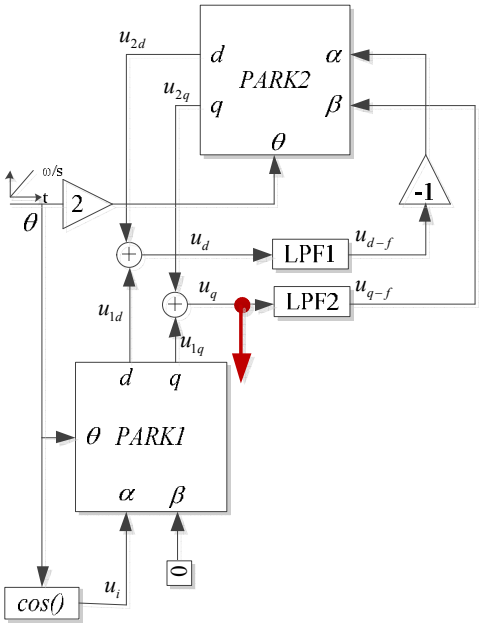
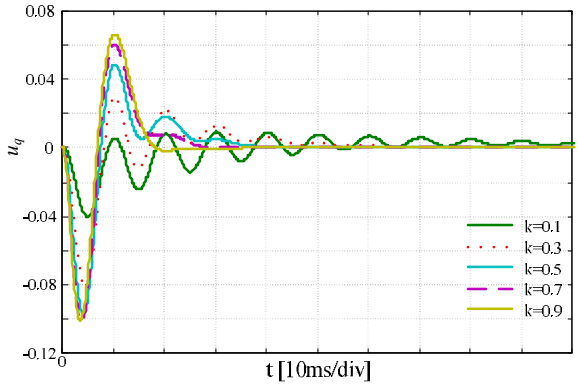


Fig. 4. Performance evaluation method for Phase Detector.

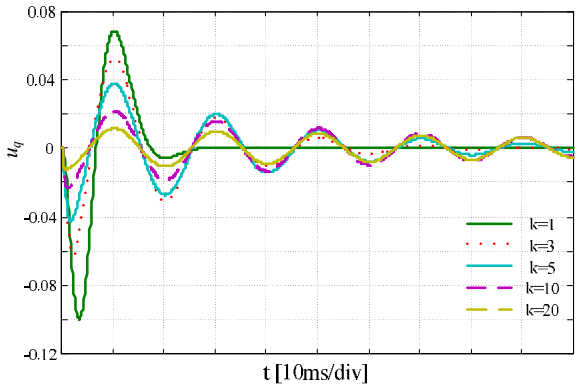
$$\begin{bmatrix} \frac{du_{d-f}}{dt} \\ \frac{du_{q-f}}{dt} \end{bmatrix} = -\varpi_c \cdot \begin{bmatrix} 1+\cos 2\theta & \sin 2\theta \\ -\sin 2\theta & 1-\cos 2\theta \end{bmatrix} \cdot \begin{bmatrix} u_{d-f} \\ u_{q-f} \end{bmatrix} + \varpi_c \cdot \begin{bmatrix} 1+\cos 2\theta & \sin 2\theta \\ -\sin 2\theta & 1-\cos 2\theta \end{bmatrix} \begin{bmatrix} A \\ 0 \end{bmatrix} \quad (23)$$

The differential equation model in (23) states that the PD is a linear time variant system. Since the analytical solution is highly complex and hard to obtained, a computer-aided method is proposed to evaluate the performance of the PD. This method is efficient and fast in guiding the selection of ω_c and is expressed in Fig. 4. The cosine function in the bottom left generates the cosine unity input to the PD, and the phase angle error to each PARK block is zero. As a result, when a step input occurs in the PD, the PD output u_{d-f} converges to 0.5 in the steady state since the input is a unity input, while the PD output u_{q-f} goes back to zero. This method is implemented in MATLAB/SIMULINK, u_q with different values of the coefficient *k* shown in Fig. 5(a) and Fig. 5(b), respectively.

It can be observed from Fig.5 that an LPF with a low ω_c attenuates the ripple well. However, it can also be seen that the convergence takes a longer time. When *k* is lower than 0.3, it takes more than 2 input signal cycles. A high *k*, which is over 1, brings u_q into the extended steady state in almost half an input signal cycle. However, the ripple is under-damped, which causes periodic errors. By selecting a value for *k* that is between 0.5~1, a satisfactory result can be obtained in u_q. Considering the total settling time, *k* is selected to be 0.707. In the following tests of the paper, *k* is equal to 0.707 in both the simulation and the experiment.



(a)



(b)

Fig. 5. u_q for different *k* with unity input (a: *k*<1; b: *k*>1).

C. Loop Filter Design

The LF is commonly designed with the PLL's linear small signal model, as shown in Fig. 6. Most studies select a PI controller as the LF in order to track the ramped phase angle without errors. The VCO is model as an integrator. Usually, only the static gain of the PD G_{PD} is considered in the LF design procedure.

Based on the small-signal model, the closed loop transfer function of the PLL can be easily derived in (24). Certain relations can be derived by rewriting (24) in the general form of a second order system.

$$\frac{\theta_e(s)}{\theta_i(s)} = \frac{G_{PD} \cdot k_p \cdot s + G_{PD} \cdot k_i}{s^2 + G_{PD} \cdot k_p \cdot s + G_{PD} \cdot k_i} \quad (24)$$

$$\frac{\theta_e(s)}{\theta_i(s)} = \frac{2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2} \quad (25)$$

$$\begin{cases} k_p = \dfrac{2 \cdot \zeta \cdot \omega_n}{G_{PD}} \\ k_i = \dfrac{\omega_n^2}{G_{PD}} \end{cases} \quad (26)$$

The PI-type LF can be designed with the desired system performance expectations with (26), i.e. ω_n and ζ. The damping factor ζ is commonly selected as 0.707 for sufficient tracking speed and suppression of the overshoot.

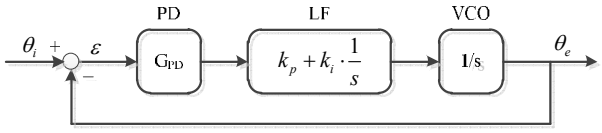


Fig. 6. Small-signal model of PLL.

Because G_{PD} is usually constant, the LF parameters are dominated by ω_n. For certain values of ω_n, the relation between k_p and k_i is expressed in (27). The special case of the proposed PLL is expressed in (28) when $\zeta = 0.707$ and the input is 1.5 times the per-unit value. In most PLLs, G_{PD} is equal to the input magnitude. However, based on the analysis in Section II, it should be pointed out that G_{PD} is equal to half of the single phase input signal. Attention should be paid to this when calculating the LF parameters.

$$k_i = \frac{G_{PD}}{4 \cdot \zeta^2} \cdot k_p^2 \tag{27}$$

$$k_i = \frac{3}{8} \cdot k_p^2 \tag{28}$$

In this way, ω_n becomes the only parameter of concern while ζ is already selected as 0.707. The natural frequency ω_n is decided by the desired bandwidth ω_b. Let the module of (25) equal $\frac{\sqrt{2}}{2}$, and when $s = j \cdot \omega_b$, the coefficient between ω_n and ω_b can be obtained, i.e. $\omega_b \approx 2.1 \cdot \omega_n$.

The dynamic performances of the PLL under common conditions are evaluated with different values of ω_n, and the results are shown in Fig. 7. In this case, *m* is the ration between the natural frequency ω_n and the input fundamental frequency ω_1.

It can be observed that with a high *m*, which means a high bandwidth, the overshoot of the frequency estimation is considerably high. Large variations in the frequency estimation also mean a large mismatch in the phase angle estimation during transients. Especially in Fig. 7(c), the transient overshoot is undesirable with a high *m* value. What is even worse, the frequency estimation fails to converge back to the new frequency of the input, when *m*=0.7. This is not acceptable in PLL applications.

The ±1 Hz band around the actual frequency is also plotted in dot-dash lines in all of the simulation results. A low bandwidth LF brings a small frequency estimation overshoot but at the expense of a longer settling time.

The phase angel comparison in Fig. 8, with *m*=0.2, states that: 1) after a sudden 90 degree phase angle jump, the estimated phase angle mismatch is well limited after 1 input signal cycle, and the mismatch is totally eliminated after 3 input signal cycles. 2) The input sag brings a minor influence

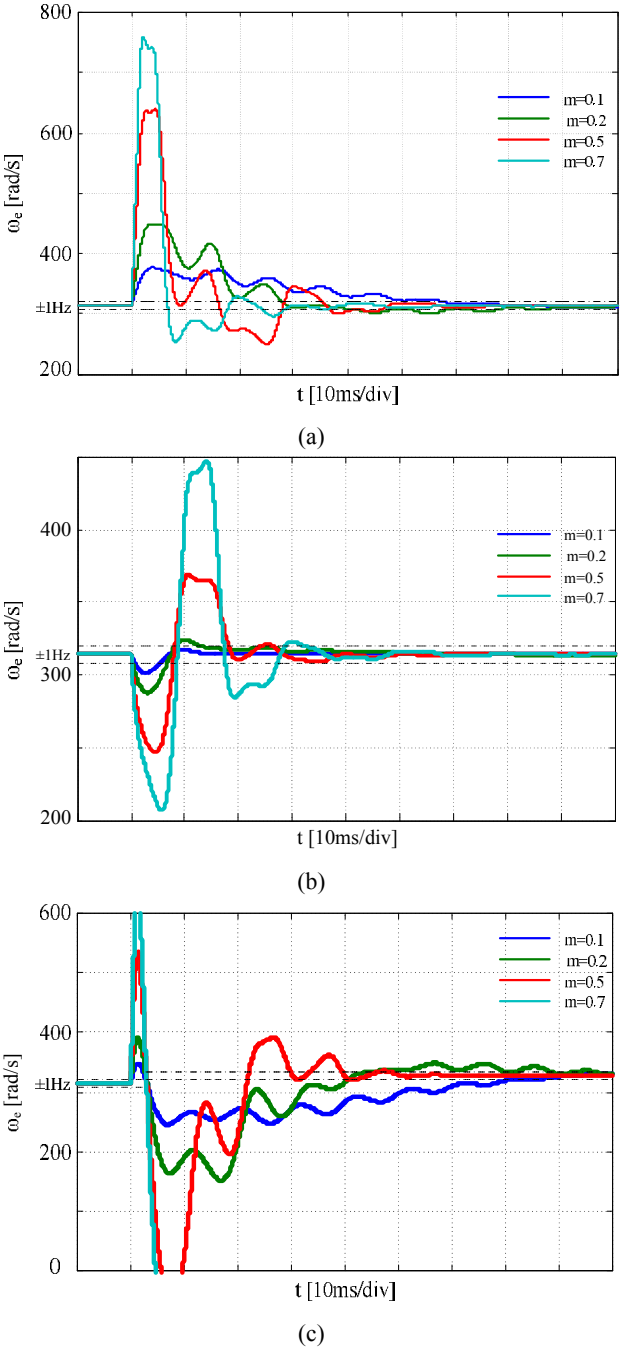


Fig. 7. Frequency estimation with different ω_n under (a) 90 degree phase angle jump, (b) 50% sag and (c) 2 Hz frequency step.

to the estimated phase angle. 3) The frequency step is the most critical condition for the proposed PLL. The proposed PLL limits the phase angle mismatch in a small range after one input cycle. The phase angle estimation coincides with the actual phase angle totally after 4 input cycles.

It is well accepted that the anti-harmonics performance of a PLL can be enhanced by reducing the bandwidth. Because the PLL is a low pass filter, which can be known from (25), it

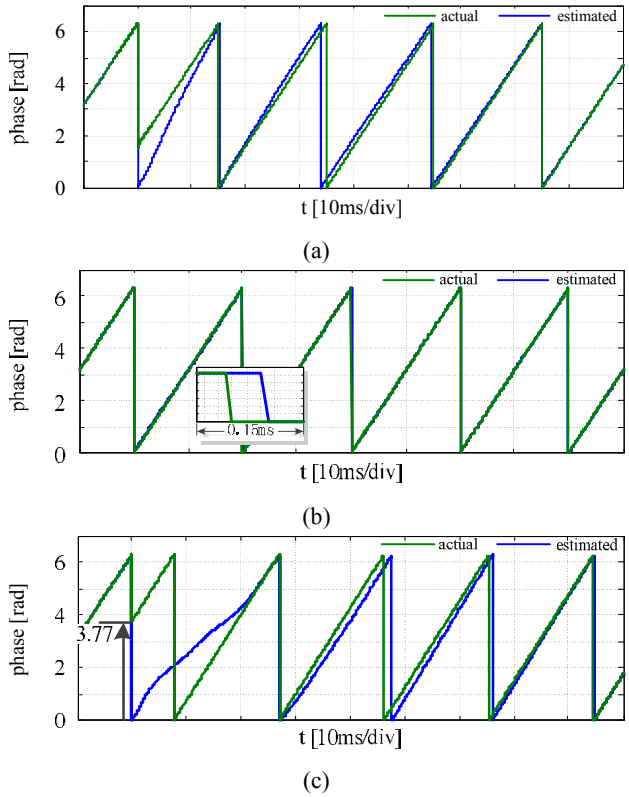


Fig. 8. Phase angle comparison with m=0.2 under (a) 90 degree phase angle jump, (b) 50% sag and (c) 2 Hz frequency step.

provides attenuation at a slope of 20dB/Dec at a frequency higher than ω_b. However, the bandwidth is related to the lock range of the PLL. Too small a ω_b will cause a lock failure under certain conditions. It order to deal with this failure, the value of ω_1 in Fig. 3 should be set to the frequency of concern. The abandoned set of ω_1 should be avoided.

IV. Experiments and Comparisons

The proposed PLL is verified and evaluated by comprehensive tests. The test platform is sketched in Fig. 9. During the test, a function/arbitrary waveform generator (Agilent 33220A) is used to generated a set of particular single phase inputs. The PLL algorithm is implemented in a DSP development board based on a TMS320F28069, whose clock frequency is 90MHz. The estimated phase angle and frequency are visualized by an onboard digital-analog converter.

A. Sampling Frequency Selection

It is important to select a suitable sampling frequency when implementing algorithms in a digital signal processor. However, when any algorithm is implemented in a digital control IC, there are 2 time constants which need considerations, i.e. the sampling period T_s and the computation delay T_d. A diagram of a PLL digital implementation considering these 2 time constants is shown in Fig. 10.

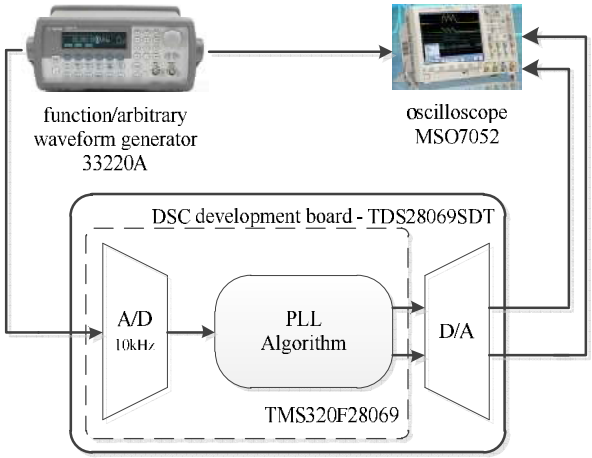


Fig. 9. Experiment setup for PLL evaluation.

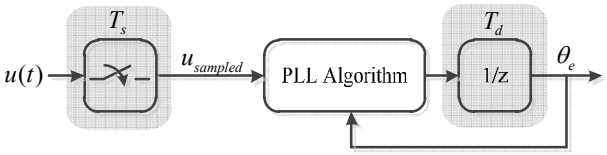


Fig. 10. PLL implementation diagram considering discrete time constants.

T_s is introduced by the AD conversion, which translates the continuous input into a sampled data signal with a constant update rate. T_d is a time interval where the algorithm completes the computation and makes the output update. After the PLL algorithm is implemented in a TMS320F28069, it can be measured that the maximum execution time of the proposed PLL algorithm for each phase angle estimation update is 16.756μs, i.e. 59 kHz. In other words, a T_s which is smaller than 17μs is unnecessary. Because T_d is about 17μs in the PLL program, the extra sampled data will be dropped by the controller IC since it will not read new samples before the computation is complete.

A lower sampling frequency results in a delay and an excessive overshoot as shown in Fig. 11. It can be seen that the overshoot and the settling time become small when the sampling frequency is increased. However, there are very small distinctions between the results when using 5 kHz sampling frequency and 50 kHz sampling frequency. Therefore, an extremely high sampling frequency is also unnecessary. It brings less of a performance contribution but a higher thermal stress to the controller IC. The selection of a sampling frequency should follow the target of the application. If only the steady state results of fundamental frequency are of concern, an extreme low sampling frequency such as 500Hz (10 samples in each input cycle) can be selected. For grid connected converters, such as distributed generation and laptop adapters, the sampling frequency should be set as high as the switching frequency. If the digital Pulse Width Modulation (PWM) is configured in double update mode, it is better to set the sampling frequency at twice the switching frequency. The

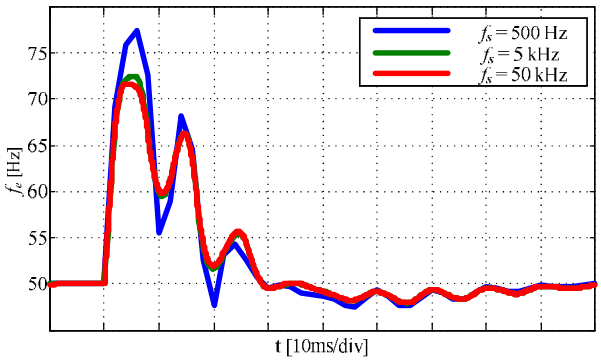


Fig. 11. Frequency estimation under 90 degree phase jump with different sampling frequency.

premise of such a selection is that all of the control algorithm computations can be completed within one selected sampling period, i.e. $T_d \le T_s$.

B. Static and Dynamic Performance Evaluation

The evaluation follows the procedure below. During the tests, the sampling frequency is set at 10 kHz.

1) The input signal is zero;

2) The input is switched to a sinusoidal source;

3) 300ms later (hereafter called step-time) certain variations are performed in the input signal;

4) The results of 200ms (10 input cycles) are recorded and shown in the following parts.

In the experiments, the proposed PLL is carried out with the following parameters to cope with all of the serious tests. The LPF1 and the LPF2 have the same cut-off frequency as 0.707 times of the input fundamental frequency, i.e. 35.35Hz. In addition, a PI-type LF is selected with k_p=124.4 and k_i=5803. This means that the system natural frequency is 10Hz, the damping factor is 0.707, and the PLL bandwidth is 21Hz.

The experiment results are shown in Fig. 12 to Fig. 14, corresponding to a 90 degree phase angle jump, a 50% input sag and a 2 Hz frequency jump, respectively. The largest overshoot in the frequency estimation during transition happens in the phase angle jump test. The phase angle estimation slope bends in the first 20 ms. After another 20 ms, it restores a high linearity. This phenomenon is shown in Fig. 12. The input sag has a minimal influence on the proposed PLL. Although a 50% sag is an unusual case, the phase angle estimation maintains a high linearity during transition. This is due to the fact that the observed fluctuation in the frequency estimation is quite small. In the above 2 tests, the phase estimation is well limited within one input cycle.

In the 2 Hz frequency step test, the excitation contains both a 2 Hz frequency increase and a 3.77 rad (216.7 degree) phase jump. The phase jump is introduced by the generation of the input's instantaneous phase angle $\theta_i(t)$. Since the value of t in (29) is not zero when the 2 Hz step is added, a certain phase jump is also added.

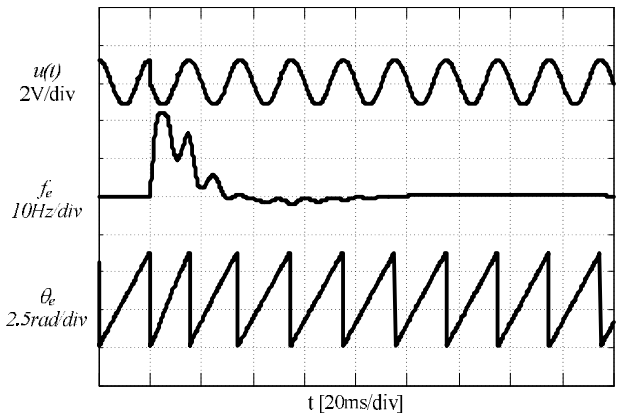


Fig. 12. Phase angle jump experiment results.

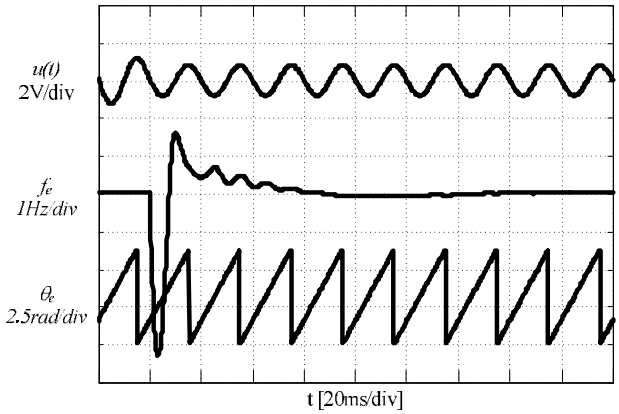


Fig. 13. Input sag experiment results.

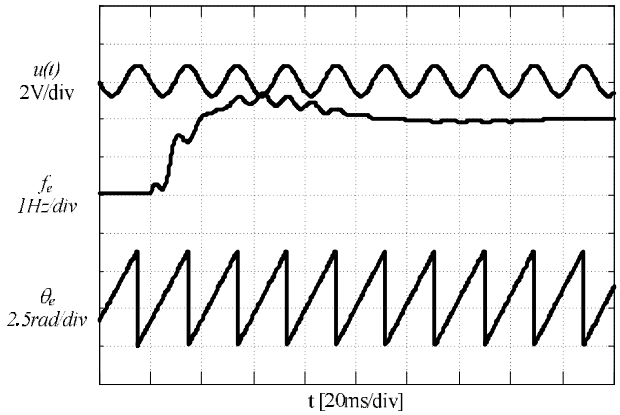


Fig. 14. Frequency jump experiment results.

$$\theta_i(t) = 2\pi \cdot (f_1 + \Delta f) \cdot t \tag{29}$$

It can be observed from Fig. 14 that the transition is smooth, and that the overshoot in the frequency estimation is much smaller than in the case of the phase angle jump test. However, the proposed PLL takes 4 input cycles to fully eliminate the estimation error.

In order to experimentally evaluate the behavior of the proposed PLL when the input is distorted, the PLL is implemented in a cascaded H-bridge multilevel static VAR generator prototype. the grid voltage is distorted by 20% of the 5th order harmonics which is provided by a programmable

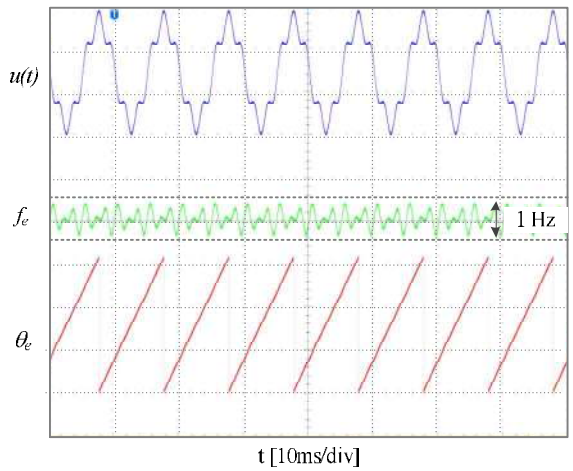


Fig. 15. Experiment results with 20% 5th harmonics distortion.

voltage source. The results are shown in Fig. 15. The ripples in the frequency estimation are well limited to below 0.5 Hz. This guarantees the phase angle estimation with a high linearity. As mention in the LF design, decreasing the PLL bandwidth helps attenuate such ripples at the cost of settling time.

C. Comparisons with Existing PLLs

As introduced in section I, a lot of PLLs have been proposed in the literature. As a result, it is necessary to make comparisons among the proposed PLL and the existing PLLs. The SOGI-PLL [13], [22], [23] and the delayed signal PLL [14], [21] are selected for the comparison because of their widespread use in single phase converters. The loop filters in all of the PLLs are identical, i.e. k_p=124.4 and k_i=5803. For the SOGI-PLL, the SOGI coefficient is 1. Additionally, because the original structures of the SOGI-PLL and the delayed signal PLL are not frequency adaptive, a certain frequency feedback is added in order to compare their performance under frequency variations. In addition, the sampling frequency is 20 kHz in order to obtain enough data for the delayed signal PLL. The results are shown in Fig. 16 and Fig. 17.

As can be seen from Fig. 16, i.e. the phase angle error under a 90 degree phase angle jump, the delayed signal PLL features the largest overshoot. However, the transition of the delayed signal PLL is minimal. After less than 2 input cycles, the phase angle error is well limited. Comparatively, the overshoot of the proposed PLL is minimal. After one and half input cycles the phase angle error is well limited. At the same time, the SOGI-PLL features a long transition and a remarkable overshoot. Therefore, the proposed PLL is the most convenient of the PLLS under the phase angle jump test.

A 2 Hz frequency step test is also concluded with these 3 PLLs, and the results are shown in Fig. 17. It is shown that all of the PLLs can operate in the new operation point, and that the phase angle error is much smaller than in the cases of phase angle jump test. The proposed PLL has the minimum overshoot in terms of the phase angle error. Ripples can be

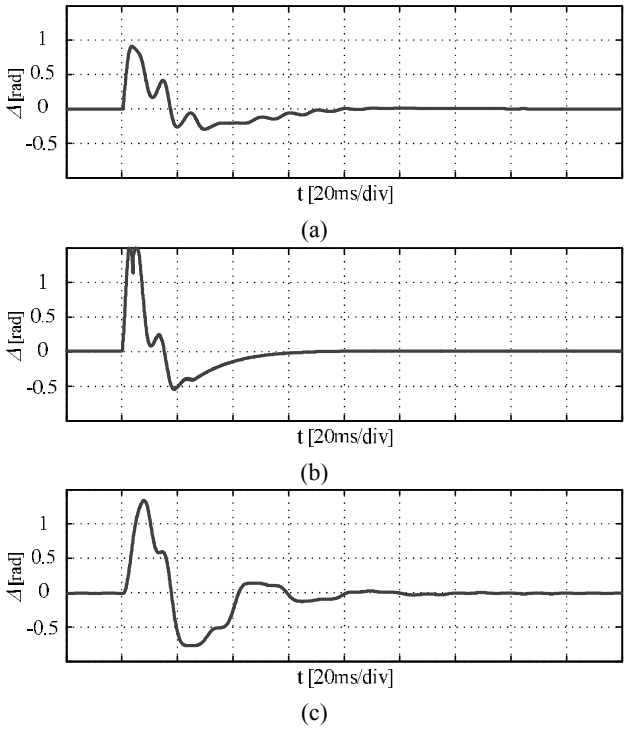


Fig. 16. Comparative results under 90 degree phase angle jump. (a) the proposed PLL, (b) delayed signal PLL and (c) SOGI-PLL.

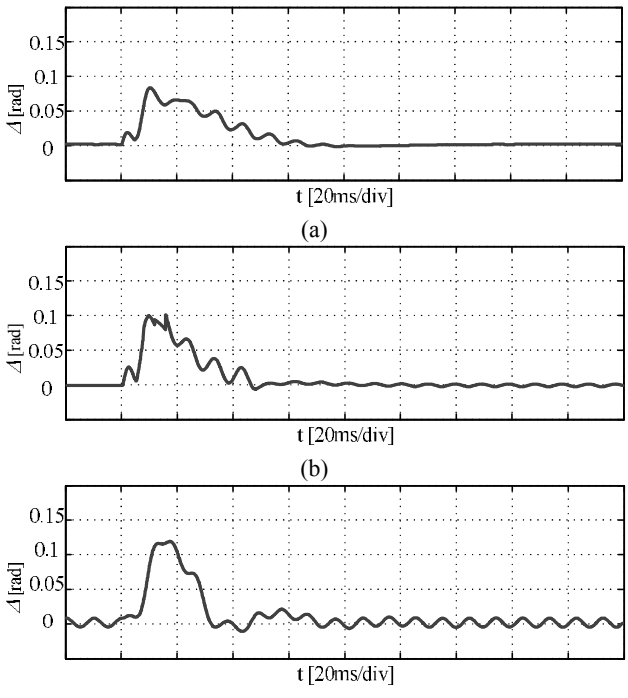


Fig. 17. Comparative results under 2 Hz frequency step. (a) proposed PLL, (b) delayed signal PLL and (c) SOGI-PLL.

observed in the other 2 PLLs. In the delay signal PLL, the number of necessary samples for the delay is not an integer after the frequency jump. This results in the undesired small ripple shown in Fig. 17(b). An even bigger ripple is founded in the SOGI-PLL. It is introduced by the simple forward Euler

discretization of the SOGI block in the comparison. A discussion on the discretization can be found in [22]. Although ripples can be found, they do not bring undesired effects because they are too small. It has to be mentioned that the proposed PLL shows no ripples, even though the simple forward Euler discretization is employed in all of the comparisons.

The comparative results state that the proposed PLL shows more convenient performance when the input has a single frequency. Unlike the SOGI-PLL, which provides attenuation of the harmonics in the QSG block, the proposed PLL can only provide harmonic attenuation by decreasing its bandwidth. However, as shown in Fig. 15, convenient estimation can also be obtained in the steady state by the proposed PLL even under a distorted grid.

V. CONCLUSIONS

The issues related to the single phase PLL are systematically discussed in this paper. By introducing conjugate rotating vector pair, the pulsing single phase input vector in the stationary reference frame is synthesized with both the positive rotating vector and the negative rotating vector. A single phase SRF-PLL is proposed in this paper by utilizing the characteristics of the conjugate rotating vector pair. It is distinguished by a constant zero β input. The design of the PLL parameters is divided into the LPF design in the PD and the loop filter design. A time domain phase detector model of the proposed PLL is derived, and a numerical simulation method is proposed to evaluate the performance of the PD with different LPF cut-off frequencies. The LF design is revised, and a brief guideline is described. Comprehensive tests are executed to verify and evaluate the proposed PLL performance. The bandwidth of the PLL, which is between 0.21 and 1.05 times the input frequency, is acceptable. Experimental results show that the PLL with suitable parameters provides satisfactory phase angle estimation in one input cycle. They also show that the estimation error can be eliminated in four input cycles for the most severe conditions.

ACKNOWLEDGMENT

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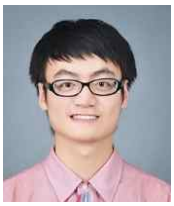

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