Research Article

A novel square wave generator based on the translinear circuit scheme of second generation current controlled current conveyor-CCCII

Umar Mohammad[1] · Mohd Yusuf Yasin[2] · Romana Yousuf[1] · Imtiyaz Anwar[1]

Abstract

A robust square wave generator employing a sole capacitor and two resistors has been presented in this study. Low power as well as popular translinear circuit scheme of Second generation current controlled current conveyor-CCCII has been taken as an active element to implement the proposed square wave generator. CCCII inhibits promising features like availability of three mutually independently and electronically adjustable parameters corresponding transconductance (g_m), intrinsic resistance (r) of the current input terminal and current gain between two terminals) that are very prevalent for control applications accepted currently. The operating frequency of the proposed model has been analyzed with respect to the passive components present there, with no exposure of output signals to the thermal voltage (V_T). Electrical/Device properties (like Noise, Threshold, area etc.) of the proposed circuit have also been discussed in this work. The simulation work was carried out on *Synopsis* Hspice tool (*v-2008.03*) from *Avant*. Satisfying results with anticipation of theoretical and simulated results, including precision (*consistency assessment*) with Pareto analysis (*Ist order Best Test flavored by Decision making analysis*) were observed during the study. The 45 nm *BSIM CMOS* modelling parameters were adopted to prove the theory. The elementary purpose of using such parameters is to maximize the circuit drive and lowering the leakage current. Another purpose of using these modelling parameters is to enhance the realization of the proposed circuit in the form of chip die and further get it fabricated in custom Integrated circuit(IC) form, from a Standard local foundry. Maximum power consumption of the circuit is 600 µW, with ± 1 V rail to rail operating voltages.

Keywords Square wave generators · CCCII based novel MOS devices · Monte Carlo analysis · Voltage and current mode circuits · Low power and low voltage CMOS circuits

1 Introduction

In the recent years, the digitals systems have maintained strong dominance over the traditional analog systems due to their outstanding features and characteristics [1–6]. But still analog devices/circuits can't be overruled or neglected, for the reason of their long term consistency in various engineering fields, by the advantage of their promising features. Advancements in both the fields have framed and shaped the fourth industrial revolution. Likely, square wave generator is the basic building block of many signal processing elements like A/D and D/A converters, applied electronics and instrumentation [7–12]. In literature, a number of square wave generators have been presented, that differ among each other by one or the other feature. Multiple active devices have been utilized

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to present the wave generator (C.L. Hou et al. used OTRA) [31], (Pal, D et al. used CCII) [19], (Silapan et al. used MO-CCCDTA) [34], (Sotner, R et al. used ZC-CG-VDCC) [36]. In the paper, we are implementing the square wave generator using the translinear circuit scheme of CCCII. Dominant low power, low voltage devices with full availability of full bandwidth (λ) are expected to ascend using CCCII schemes [13–20]. A detailed Analytical outlook of the pros and cons of the previous and present literature is also discussed in this paper. Fourier components of the voltage (V) at the output node with signal components like frequency (υ), phase(Φ), normalized phase etc. through the reference of Total harmonic distortion (THD) and *DC* components have also been presented here. Active elements find applications in the field of signal generation, such as controllability of oscillation frequency, control of output amplitudes, duty cycle etc. [18–21].

1.1 Literature review

In literature, we came across different varieties of square-wave generator circuits based on multiple active elements. A detailed comparative summary has been kept in the Table 1 of this study. However, the basic overview of literature present relating the proposed circuit/waveform generators is below.

1. In [29], square wave generator employing two CCII and five passive elements has been reported. Circuit has been verified through simulation and practically using Spice level 1 transistor parameters and AD844AN IC respectively. Maximum range of the tunable frequency has been found 300 kHz. Power consumption of the circuit is 16.83 mW.
2. C.L. Hou et al. in [32] [33] have presented square/triangular wave generator with switch controllable OTRA's. The feasibility of these OTRA's have been verified using commercial AD844AN IC. This study has mainly focused on the practical demonstration of the waveform generators. Silapan et al. [34] have used MO-CCCDTA as an active device to enhance the realization of Schmitt triggers. Bipolar *PNP* and *NPN* Pspice transistor models were used to complete the verification purposes. A total of 27 transistors were used to complete the circuit. Moreover multiple devices like AD844AN and LM13600 N have been used to make the possible implementation of the proposed circuits. Enough simulation and calculations are reported in the study. Power consumption of one of the circuits is 235 µW.
3. In [35], Sotner, R et al. have presented ZC-CG-VDCC as an active element to implement the fully fledged functional generator using both current and voltage signals. Circuit topology of the active element was completed with 52 MOS transistors using 0.18 µM CMOS technology. Practical implementation of the design has also been reported using diamond transistors, buffer models-BUF634/OPA660/860 and two resistors. Backing this work, Sotner, R et al. in [36], [37], [38] presented DT-VCA, DO-FB-VDBA & CG-CDVA as active elements to (triangular/squarewave) waveform generators. Possible implementation in simulation and on practical hands have been done greatly. Frequent use of diamond transistor has been done by the authors. Theoretical fitting in these papers is presented greatly. In [39], [40] Srinivasulu, A et al. proposed waveform generators using CCII practically as well as through simulation. Reportedly Cadence Tools were used to simulate the circuit presented at [39] in CMOS micrometer technology, however, at [40] practical implementation of the proposed theory was illustrated using commercially available AD844AN IC's.
4. In [41], [46] Siripruchyanun, M et al. proposed waveform generators using OTA and MO-VDTA. Pspice has been used to simulate the circuit presented in the above cited literature. [41] has reportedly enough application part exceeding square wave generation. BJT transistors has been used to prove the proposed theory. In [46], number of BJT transistors have been increased up to 36 and has been made essential for square/triangular waveform generation. Total Power consumption of the proposed circuit in the study is reported 14.3 mW. In [42] Hung-Chun Chien proposed waveform generators DVCC. This paper presents a voltage-controlled dual slope operation square/triangular wave generator circuits. Various other applications based on multiple differential voltage current conveyors has been reported by the authors. Some practical simulations and verifications have also been proposed in the study. Overall power consumption of the circuit has been reported 763 mW.
5. In [43], Vijay et al. have proposed squarewave generator using Second-Generation Differential Current Conveyor DCCII. Simulation of the circuit was done using cadence systems implying 180 nm gpdk parameters. In addition, hardware realization has also been reported using AD844AN. In [45, 47, 48] chattervedi et al. have proposed multi output active devices MO-DXCCTA, MO-CIDITA for advanced square/triangular waveform generation. Reportedly in the particular literature, few hardware implementation have been done using the commercially available IC's AD844AN and LM13700. Satisfying cooperation of theoretical and practical outputs have been found. Probably, [48] is the only study that has proposed Schmitt trigger without any passive element. Various other features like high frequency,

Table 1 Comparison of the state of art-*square wave generator technologies*

Reference	Active element	No of active elements	No of passive elements	Grounded capacitor (s)	Grounded resistor (s)	Hardware implemented	Transistor type/IC used	Technology node/ Models	Ib/ Vcc
C.L. Hou et al. [33]	OTRA	1	4	No	No	Yes	AD844AN	Not applicable	N.A/ 15 V
C.L. Hou et al. [32]	OTRA	2	4	No	No	Yes	AD844AN	Not applicable	0.9 mA/5 V
Pal D et al. [29]	CCII	2	5	Yes	Yes	Yes	AD844AN	Spice level 1	5–10 V
Silapan et al. [34]	MO-CCCDTA	2	1	Yes	No	Yes	BJT	µM	1.5 V
Sotner R et al. [35]	ZC-CG-VDCC	1	4	Yes	Yes	Yes	MOSFET	0.18 µM	1 V
Sotner R et al. [36]	DT-VCA	3	2	Yes	No	Yes	VCA610, OPA860/660	–	5 V
Sotner R et al. [37]	DO-FB-VDBA	2	3	Yes	Yes	Yes	MOSFET	0.18 µM	50 µA/1.2 V
Sotner R et al. [38]	CG-CDVA	1	2	Yes	No	No	EL2082	Macro models	5 V
Srinivasulu A et al. [39]	CCII	3	7	Yes	Yes	Yes	MOSFET	0.6 µM	6 V
Srinivasulu A et al. [40]	CCII	3	7	Yes	Yes	Yes	AD844AN	Spice model	7 V
Siripruchyanun M et al. [41] [46]	OTA, MO-VDTA	3 2	3 3	Yes Yes	Yes Yes	Yes No	BJT	Pspice model/ µM	5 V
Chien et al. [42]	DVCC	2	4	Yes	Yes	Yes	AD844AN	Spice Model	–
Vijay et al. [43]	DCCII	1	3	Yes	Yes	Yes	MOSFET	180 nm	2.5 V
Chattervedi et al. [45, 47–50]	DXCCTA/ MO-CIDITA	7	22	Yes	Yes	Yes	AD844AN,LM13700	µM/ 90 nm	–
Ranjan et al. [51]	FTFN	1	2/3/8/10	Yes	Yes	Yes	AD844AN	µM	1.65 V
PROPOSED (Fig. 3)	CCCII	1	2	Yes	Yes	No	MOSFET	45 nm	8µA/1 V

OTRA Operational trans resistance amplifier

MO-CCCDTA Multiple-output current controlled current differencing transconductance amplifier

ZC-CG-VDCC z-copy controlled-gain voltage differencing current conveyor

DT-VCA Dual transistor voltage controlled amplifier

DO-FB-VDBA Dual output fully balanced-voltage differencing buffer amplifier

CG-CDVA controlled gain current and differential voltage amplifier

CCII Second generation current conveyor

OTA Operational transducer amplifier

DVCC Differential voltage current conveyor

DCCII Second generation differential current conveyor

DXCCTA Dual-X current conveyor transconductance amplifier

MO-VDTA Multi output voltage differencing transconductance amplifier

CCCII Second generation current controlled current conveyor

controllable duty cycle have also been found in the above literature.

6. Ranjan et al. in [51] have presented FTFN based Schmitt trigger enlightening the behaviors of square and triangular waveform generation. Pulse width modulation scheme has been used to enhance the realization of the proposed circuitry. Micrometer technology in Pspice tool has been used for the realization of the circuit. Finally hardware implementation has been done using AD844IC. Power Consumption has been figured at 2.4 mW in the study.

While concluding the literature and revealing the post justification, excellence and the commensurate advantages of the proposed design, fewer thing can be settled down finally. Firstly an ultimate low power circuit, implemented using the translinear circuit scheme of second generation current conveyor-CCCII has been presented. Which according to the author's best knowledge isn't available yet in the literature present. Furthermore, proposed Circuit has lesser complexity in terms of design and component requirement. In standings with the comparative operating frequency, CCCII based squarewave generator is expected to work in megahertz range (MHz). Higher slew rate in Gigahertz (GHz) has been found, during the simulation study of the circuit. Finally, a good handoff of theoretical and practical results was seen in the study.

2 Cccii Design, Non Idealities And Considerations

The scheme, we have adopted in the second generation current conveyor is the current mirror based translinear circuit (CCCII +) [13] shown below in Fig. 1. The advantage of using this circuit scheme is that it is fully balanced. The intrinsic resistance in this type can be balanced by tuning the biasing current I_b.

The matrix representation of CCCII is below;

From the above matrix as shown in Fig. 2, we can conclude the following things relating the operation of CCCII ± .

$$I_y = 0 \tag{1}$$

$$V_x = V_y + I_x \cdot R_x \tag{2}$$

$$I_{z+} = +I_x \tag{3}$$

$$I_{z-} = -I_x \tag{4}$$

$$\text{Resistance at } x = R_x = \frac{1}{2gm} = \frac{1}{\sqrt{8\beta_n}} I_b \tag{5}$$

where $\beta_{n=}\mu_n C_{ox} \cdot \frac{W}{L}$

The above equations are well defined from the above matrix in Fig. 2, in which we have, I_y is the node current at Port *Y*. V_x refers to voltage at node *X*. V_y is the voltage at node *Y*. I_z and V_z are the current and Voltages at the node *Z* respectively. Lastly, R_x is the intrinsic resistance of the translinear circuit. R_X present at port X depends inversely on bias current (IB). The parasitic resistance RX of terminal X is proportional to $1/I_B$ for BJT realizations and inversely proportional to the square root of the bias current for CMOS realization [56] [57]. The Limitations of the CCII enhanced by *Fabre* resulted the new the new device termed as Current controlled current conveyor-CCCII. Inclusion of Rx was shown in the particular device, in order to balance the adjustment of the voltage relationship between node X and node Y, thereby imparting tunability to the device.

Some of the promising features of the CCCII are viz. [22–26]

1. Greater Linearity and Current mode Applicability.
2. Availability of full bandwidth.
3. Auto balancing at higher temperatures.
4. Low power & low voltage.

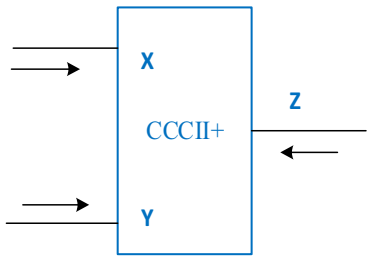

Fig. 1 General representation of CCCII+

$$\begin{bmatrix} V_X \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} R_X & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_z \end{bmatrix}$$

Fig. 2 Matrix representation of CCCII±

3 Proposed and implemented square wave generator

In literature a Variety of circuits quoting reference of square wave generator are available. Few circuits employing CCII [39, 40] as an active device are available. But no such circuit with the translinear circuit scheme of CCCII is available yet. CCCII is expected to enhance the features of the existing literature, because of its dominant features as described above. The literature available has been compiled in the table below.

Figure 3 shows the presented square wave generator circuit. One CCCII+, one capacitor (C), and only two resistors (R_1 and R_2) have been used to implement the circuit. Translinear circuit topology used to drive CCCII+ has been put forth here for the readers.

Captivating CCCII+ as an active principal component and casually joined passive components fashioned a novel square wave generator is shown in Fig. 4, with a single capacitor and two resistances. The Parasitic elements can be tuned to obtain the self-satisfying (*commercially needed for IoT and Coginitive radio*) simulation results.

Considering the ideal input/output terminal characteristics of the CCCII+ documented in Figs. 1, 2, 3 and 4 and Eqs. (1–5). Referring to the notations as shown in Fig. 3 and for ideal CCCII, $i_y = 0 : v_x = v_y + i_x.r_x : i_z^+ = +i_x : i_z^- = -i_x$ and $v_x = v_y$ therefore, i_x flows out of the node *X* as shown in Fig. 3.

A detailed analysis of the Time period can be investigated from the desired corresponding specimen wave form (provided in Fig. 5) of the proposed circuit.

From the Fig. 5, we have two possible saturation levels pointed as L+ and L− for the output voltage V_o. Individual Steady state operations can be made for the charging as well as the discharging mode of the capacitor. Alternate

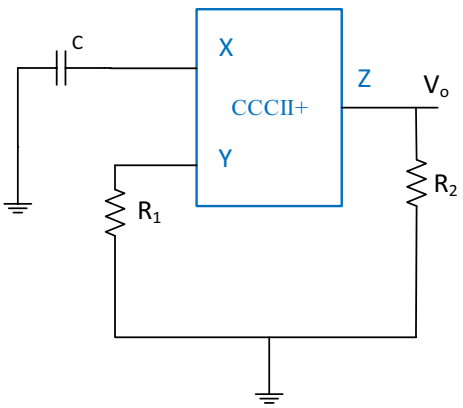

Fig. 3 Proposed circuit of square wave generator

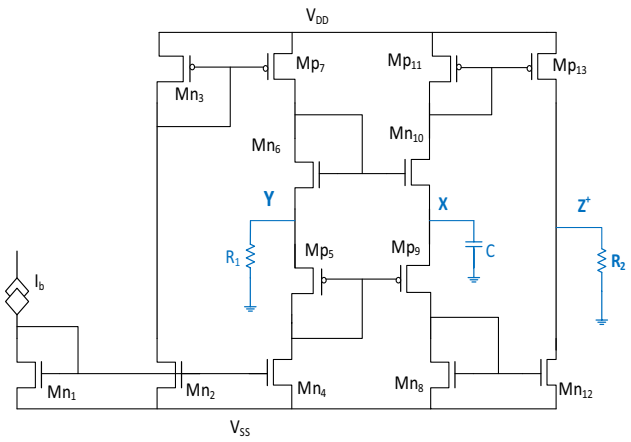

Fig. 4 Proposed circuit implemented using CMOS translinear circuit topology

standard equations presented in the literature [44], [43] can also be followed to sum up the circuit description. Theoretical calculations based on the commensurate observations from Fig. 5 leads us to reveal the probable equations for the time period.

$$V_{out} = V_x \cdot R_2/R_1$$

Now, the Standard charging equation for a Capacitor can be written as;

$$q = CV\left(1 - e^{-t/RC}\right) + q_o \cdot e^{-t/RC} \tag{6}$$

Further, few conclusions can be made for the rising waveform viz: $(V_{c(t)} = \lambda \cdot V_{out}; V_{TL} = -\lambda \cdot V_{DD}; V_{TH} = V_{DD})$

Hence Eq. 6, can be written as;

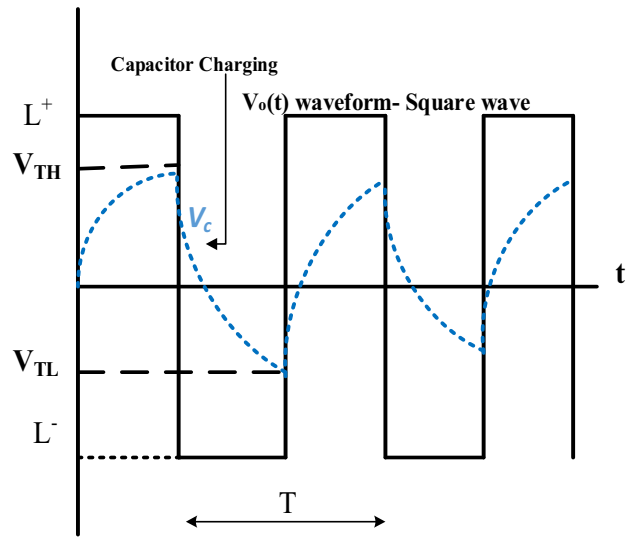

Fig. 5 Specimen waveform of the proposed design

$$q = C \cdot V_{DD}\left(1 - e^{-t/RC}\right) - \lambda \cdot C \cdot V_{DD} \cdot e^{-t/RC} \quad (7)$$

Now, Considering the Fig. 5, when the charging voltage switches from one cycle to another, a change occurs at the extreme points of V_{TH} and V_{TL} and surely the time t = T/2 for the particular squarewave and this particular change can be mathematically drafted in the Eq. 7 viz.

$$-\lambda \cdot C \cdot V_{DD} = C \cdot V_{DD}\left(1 - e^{-T/2RC}\right) - \lambda \cdot C \cdot V_{DD} \cdot e^{-T/2RC} \quad (8)$$

Solving above equation for *Time period* T, we have the following equation;

$$T = 2R_1 C \ln\frac{1+\lambda}{1-\lambda} \quad (9)$$

Equation 8 represents the overall time period function of the circuit design to achieve behavior of square wave generator.

4 Simulation results of the proposed square wave generator

The results obtained from simulation study of the proposed circuit were quite adequate and satisfying in anticipation with the theoretical ones. Various types of analytical results were observed on the Cosmos Scope (C-Scope) tool provided by the Hspice tool from Avant. 45 nm bulk cmos modelling parameters [44] were used to simulate the implemented translinear circuit employing MOS transistors. Figure 6 is the output waveform of the circuit with *overshoot* 0.086% and *undershoot* of 0.0057348 (nearly 3.0277%). Hence depict the exemplary linearity and consistency of the square waveform. A detailed analysis of the proposed circuit provided in the Fig. 4 was done, including the decision making analysis.

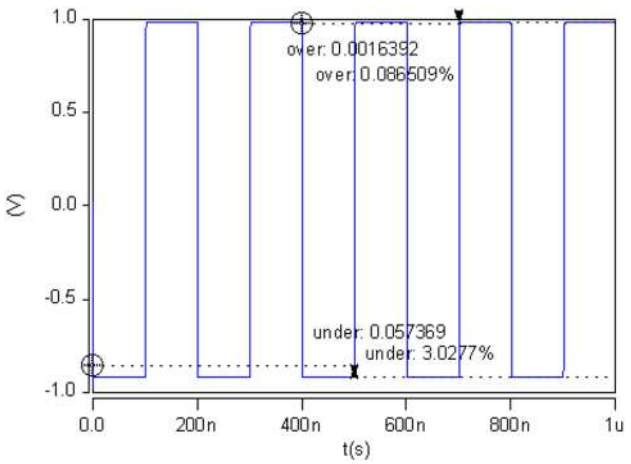

Fig. 6 Output waveform of the proposed square wave generator with the over and undershoot compressions

Figure 7 observed output electrical properties of the proposed circuit in Fig. 4: *Rise time* 666.97 ps and *fall time* 79.32 ps, *Slew rate* 2.1794 g, *Period of one cycle* is 200 ns, *Frequency* of 4.999 MHz, *Duty cycle* 0.49552 s, *Pulse width* 99.105 nm. *Mean* 0.14889, *Median* 0.52534, *Range* 1.9601 and *Standard deviation* 0.84512 (Table 2).

Figures 8 and 9 represent the histograms of the square wave generator in two forms. Former one pointed at Fig. 8 has number of bins = 20, with the advantage of having impact with *cumulative* and *normalising* functions than the latter one shown in Fig. 9. Apart from this, Frequency Fourier transform analysis of the Fig. 4 is done here. FFT was done using the time increment *linear/logarithmic,* waveform view *line/spectral,* sampling frequency – 2.08 GHz and window function using various *scheme*. Few parameters like total harmonic distortion-THD, signal to noise ratio-SNR, Signal to noise and distortion ratio-SINAD were calculated for the proposed circuit. Phase and the Noise Plots of the circuit at the Fig. 4, have been analyzed using hann,

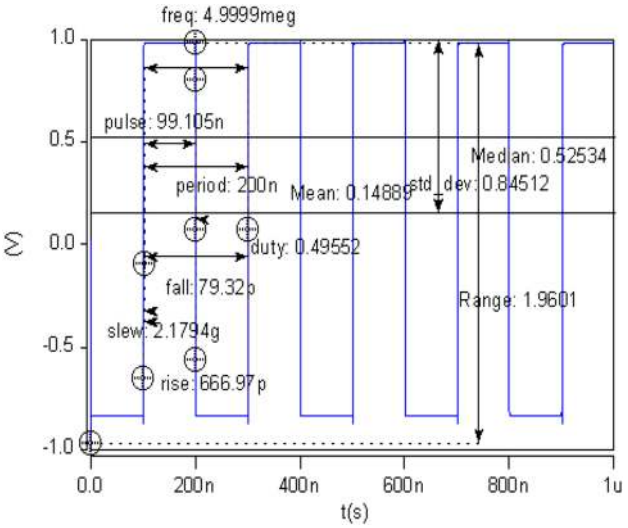

Fig. 7 Detailed analysis plot of the proposed circuit

Table 2 W/L of MOSFET'S used to implement proposed design

Transistor no.	Width (micrometer)	Length (micrometer)
Mn_1, Mn_2, Mp_5, Mp	0.5 u	0.1 u
Mn_8, Mn_{10}, Mp_{13}	0.5 u	0.1 u
Mp_3, Mn_4, Mn_6, Mp_9, Mp_{11}, Mn_{12}	2.5 u	0.5 u

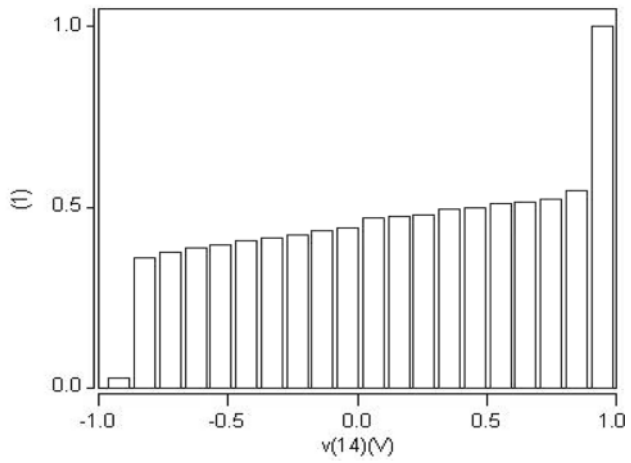

Fig. 8 Effective histogram of the proposed design

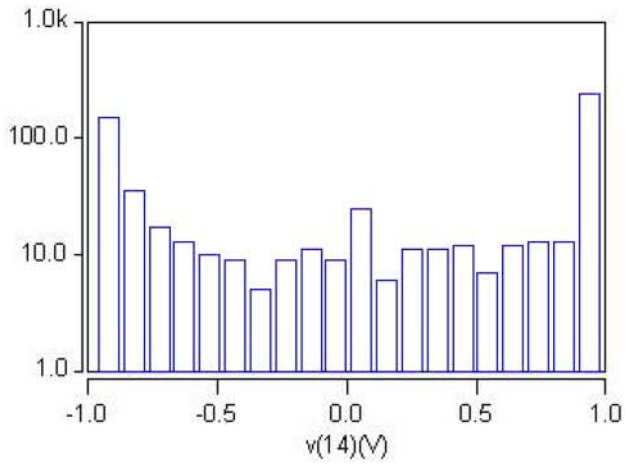

Fig. 9 Actual histogram of the proposed design

hamming, Blackman, flat top, cosine, rectangular and Bartlett window schemes. A quick overview of the results has also been summarized in the Table 3 below. For a total of 10 harmonics Fourier components at output (*V(14)*-O/P *node)* were observed with overall dc component finally figured at 9.39E-02 and overall total harmonic distortion 43.2281%.

In addition to the above analysis, several other circuit response have also used to analyse the behaviour of the proposed circuit. Continuity as well as the linearity of the design in Fig. 4 can be well deprived form these plots.

Detailed Ist order Best Fit Pareto Plot of the Proposed Circuit is signposted in the above plot involving the statistical measurement with comprehensive decision making analysis for the overall extreme performance of the various nodes as well the device/electrical properties for the expanded view (*Translinear circuit Topology*) of the proposed design presented in Fig. 4. In this Plot, X1 stands for the major active element(CCCII +), V(13) is the voltage at the node Y, V(12) represents voltage at node X and V(14) is the output voltage at node Z. TPOWER is the total power of the circuit, i(vss) and i(vdd) are the drain and source currents. x1[v(5), v(3), v(4), v(8), v(7) and v(10)] are the voltages across the mos transistors as per the nomenclature adopted for the proposed circuit topology in the Fig. 5.

5 Pre and post layout designs of the proposed circuit

Layout simulations were carried out using Tanner tool (*L-Edit-v16* and *S-Edit-v16*). A good agreement of satisfying results in both of the layouts and the performed spice simulations was seen. The width (W) and length (L) of the MOS were kept under the bounds of the Tanner Tool. Generic 250 nm device parameters were used for the prelayout simulation with W = 1.5 u and L = 250 n. Further, a simplified post layout simulation has been put before the readers for better understanding, with MOS width of 450 nm and length of 250 nm. Lastly, Simulations were observed out, using *layout extraction method* (Figs. 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22 and 23).

Table 3 Comparative numerical analysis of THD, SNR and SINAD

Parameter	Blackman response	Hamming response	Rectangular response	Flat top response	Cosine response	Bartlett response
THD	26.957	28.581	58.156	25.91	26.301	28.958
SNR	− 26.957	− 28.581	− 58.156	25.91	− 26.301	− 28.958
SINAD	− 26.957	− 28.581	− 58.156	25.91	− 26.301	− 28.958

The detailed comparative summary of the Total harmonic distortion (THD), Signal to Noise ratio (SNR) and Signal to Noise and Distortion ratio (SINAD) is shown in the Table 3 Above

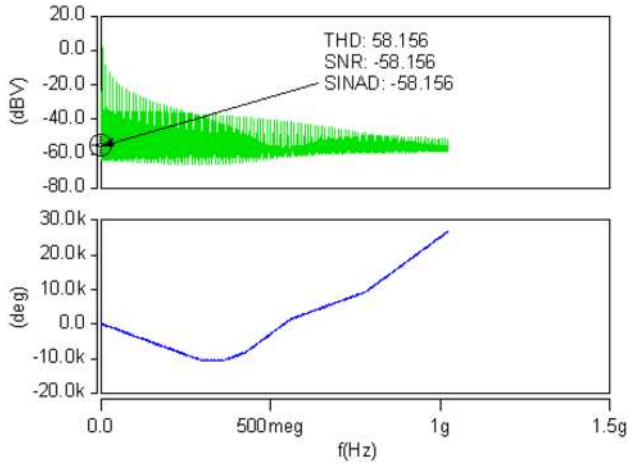

Fig. 10 FFT analysis using rectangular window scheme

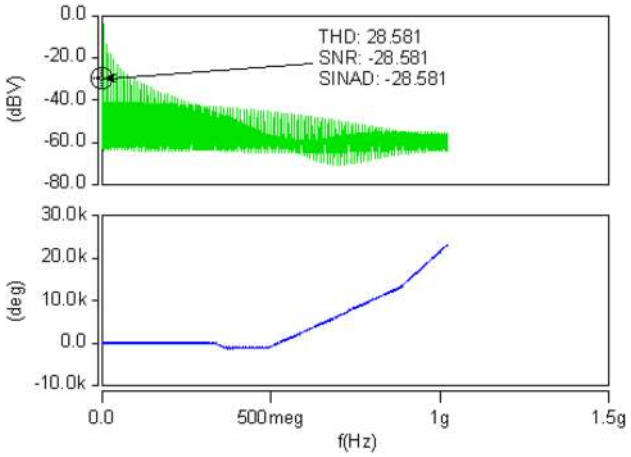

Fig. 13 FFT analysis using Hamming window scheme

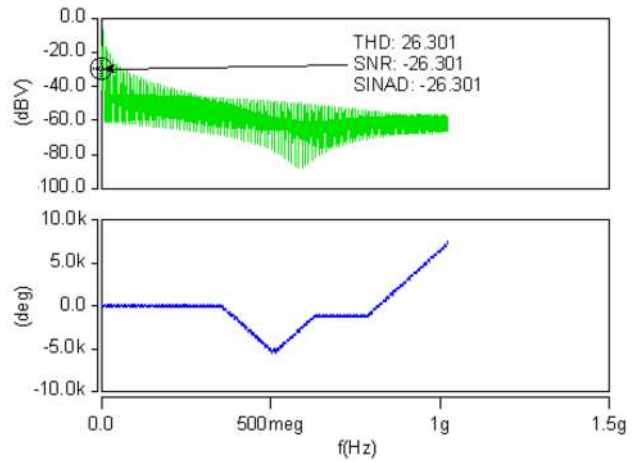

Fig. 11 FFT analysis using Blackman window scheme

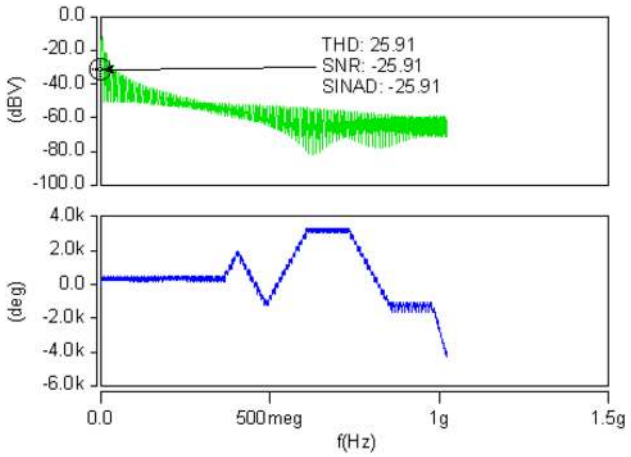

Fig. 14 FFT analysis using flatop window scheme

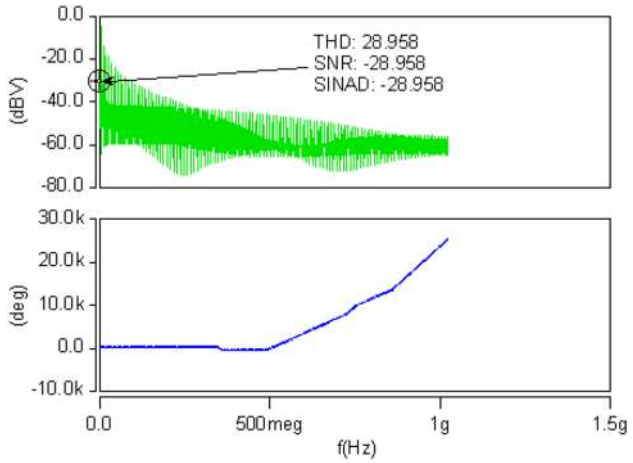

Fig. 12 FFT analysis using Bartlett window scheme

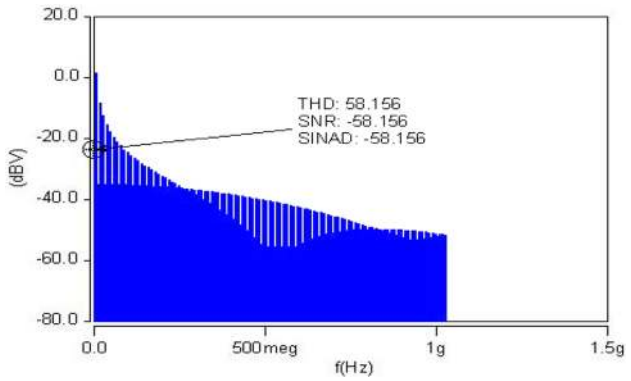

Fig. 15 Logarithmic plot using rectangular window scheme

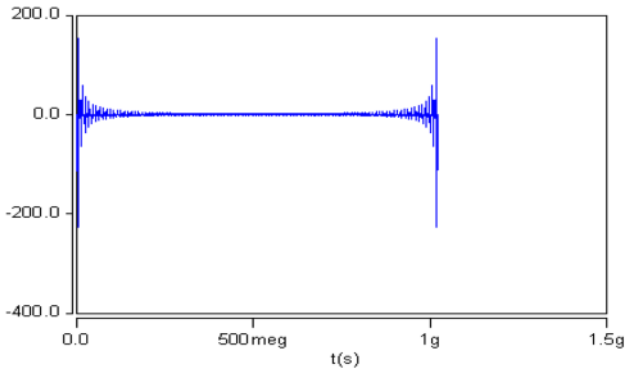

Fig. 16 IFFT plot of the proposed circuit

6 Hardware implemention of the proposed circuit using conventional ad844 ic

Commercially available CCII in the form of AD844 IC was used to realise the proposed square wave generator. Two *AD844 IC's* were used as a single *CCCII IC*, for carrying out the realisation. Figure 24 shows the hardware schematic of the AD844 based square wave generator circuit.

Comparison of simulated and measured results The setup in the figure X as well as the simulated results of the Fig. 4, conclude the working of the circuits for wide range of frequencies up to the megahertz range (~ 4 MHz). However, a large variation of the supply voltage was seen in between the simulated and the measured circuits. AD844 based CCCII requires a supply voltage of not less than 5 V, whereas the simulated circuit runs only on a supply voltage of 1 V. Nevertheless, it is better to mention, that the layouts presented in the study have close comparison with the simulated results (Fig. 25).

7 Evaluation of the pre and presented square wave generator circuits

Circuits available in the literature possess the clarity as well as the conventional Industrial perspective too. In addition, the presented circuits in literature edify satisfying results,

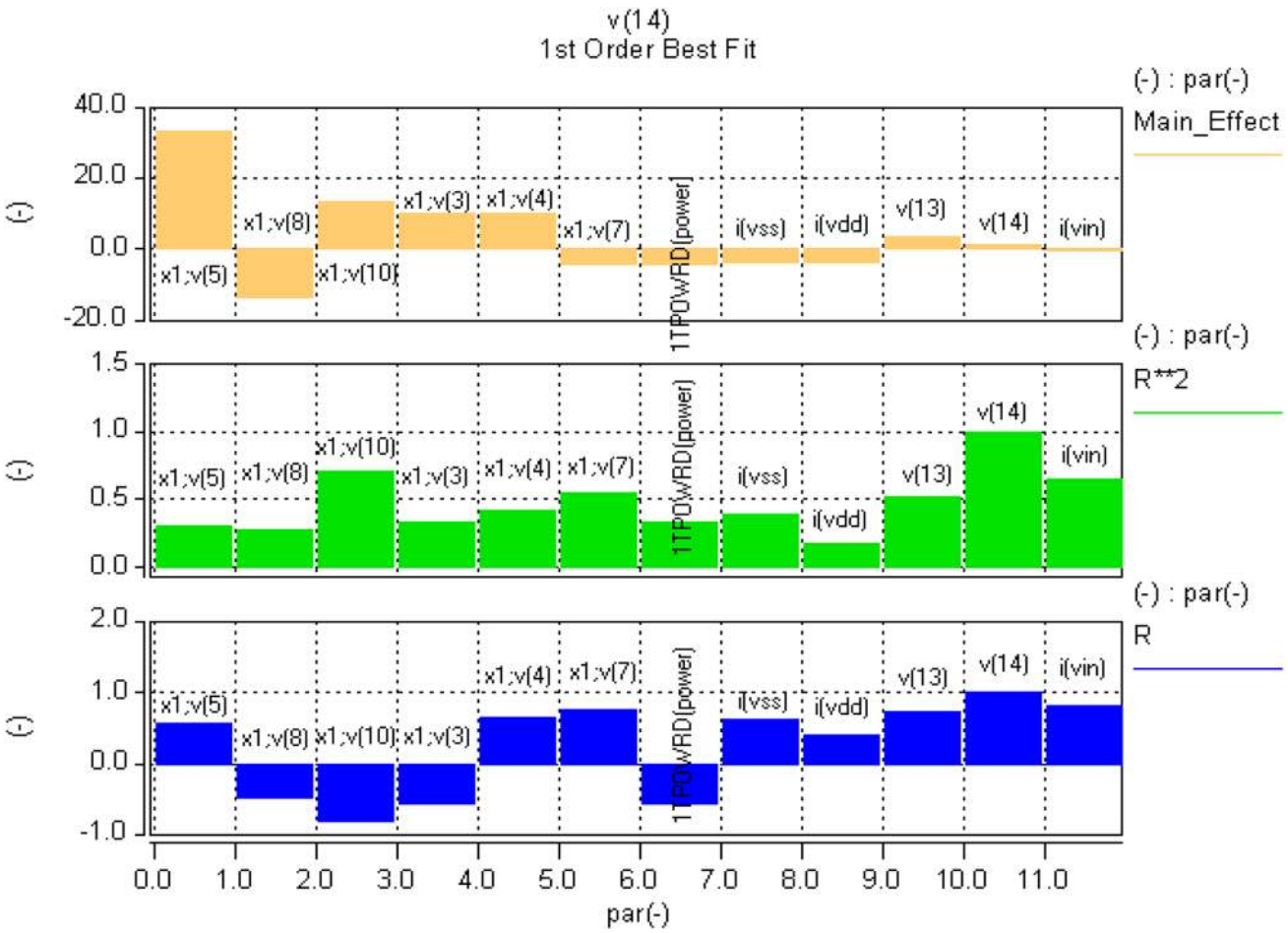

Fig. 17 Pareto plot of proposed circuit

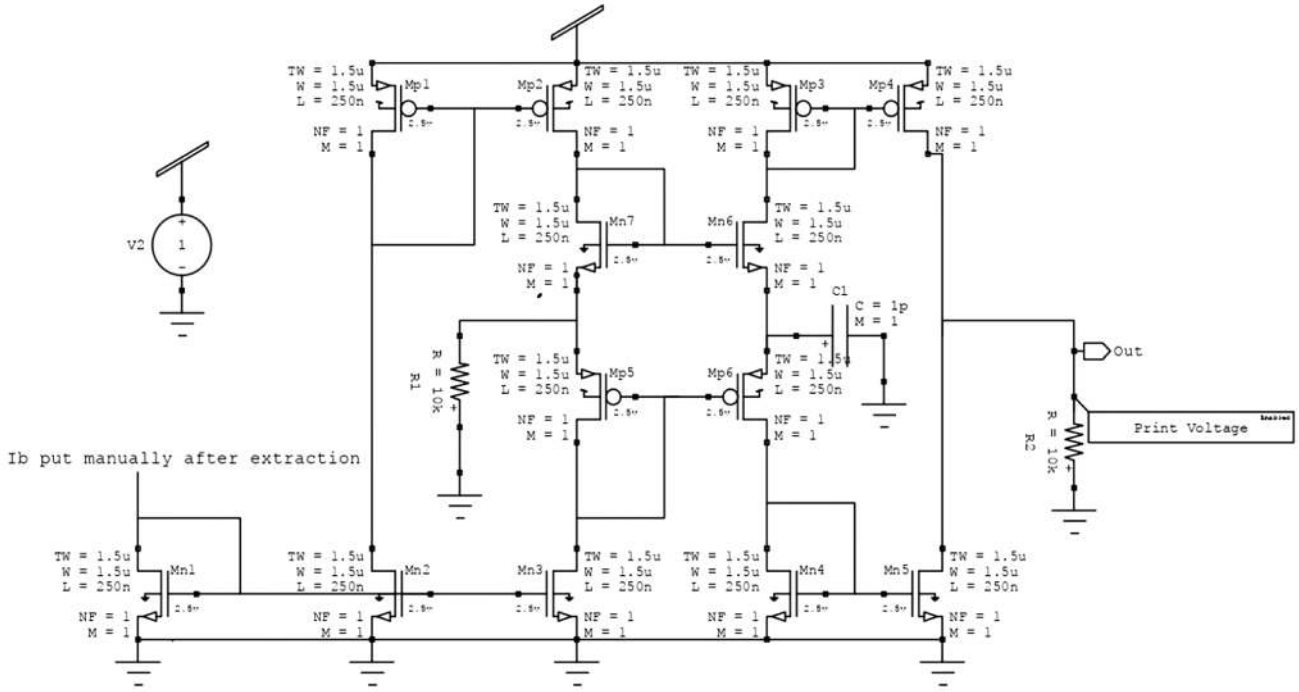

Fig. 18 Prelayout of the proposed circuit in S-Edit-v16 Mentor graphics Tool

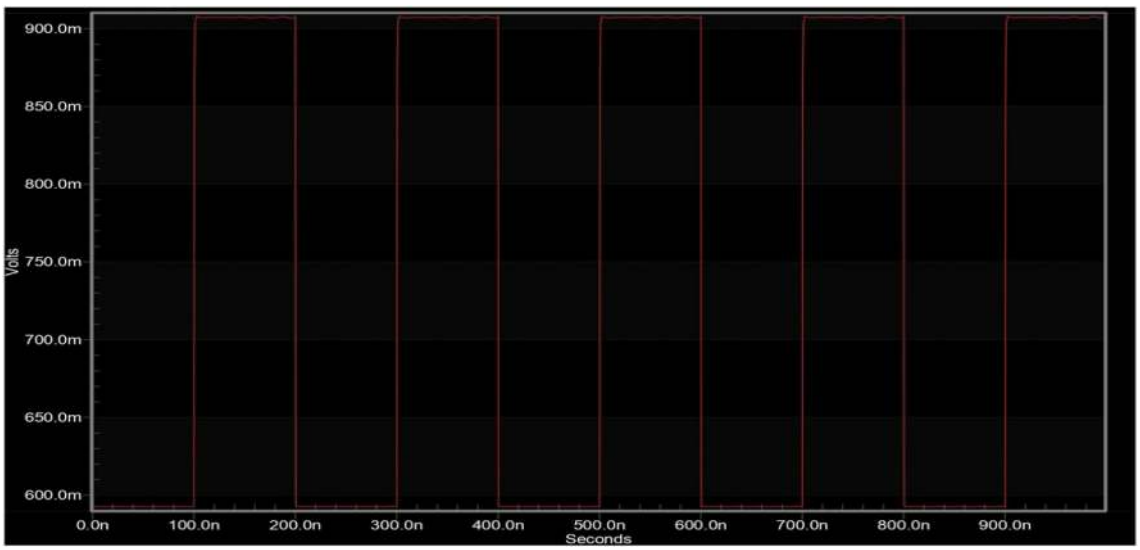

Fig. 19 Simulation O/P of the prelayout of the Fig. 18

however in the modern Industrial era of nanotechnology, an intense focus on chip *Area* and *Power* is kept whilst designing circuits. Circuits presented in the literature [13] [28] [29] have the drawback of having more number of active and passive elements than the presented in Fig. 4. Moreover, circuits presented at [16–22] [26] are lagging the grounding feature of passive elements. The striking feature of our work is the implementation of the square wave generator using the translinear circuit scheme of CCCII + (*with a single CCCII + as active device and all three passive elements grounded*). To the author's prior knowledge, the presented circuit scheme is not available in the literature till now. Circuit designed in Fig. 5, facilitates low power, low voltage terminology, high slew rate, expected to give advanced performance at higher frequencies and first of its kind implemented in the ultra-deep submicron technology. Another thing that

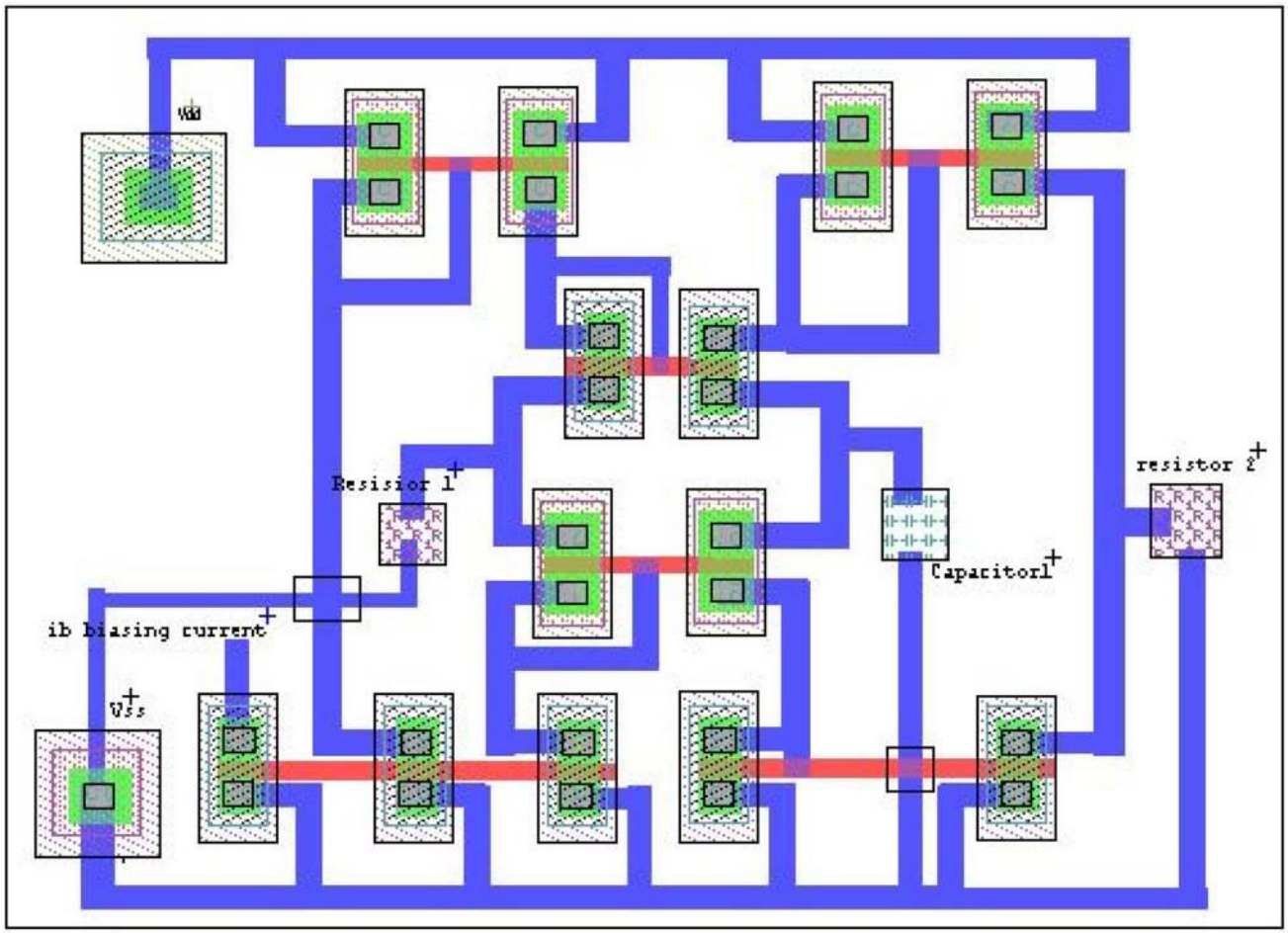

Fig. 20 Post layout of the proposed circuit in L-Edit-v16 Mentor graphics Tool

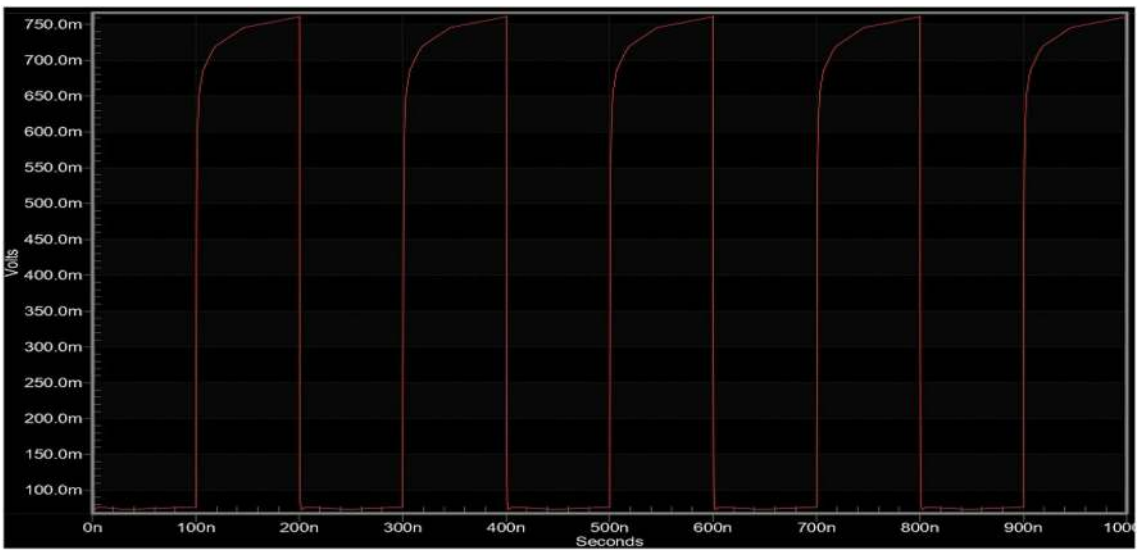

Fig. 21 Simulation O/P of the Post layout of the Figure x

circuit.

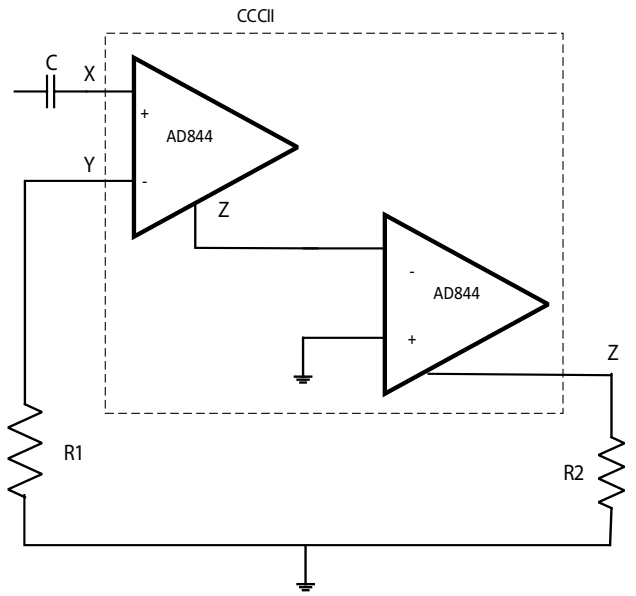

Fig. 22 Hardware setup of the proposed circuit

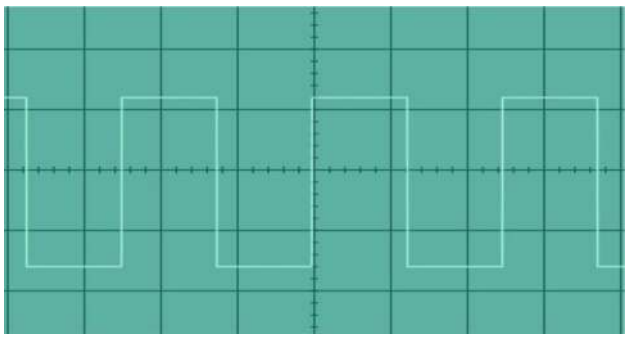

Fig. 23 Waveform (Seconds/Division: 1 ms and Volts/Division: 5 V) on the oscilloscope of Figure X

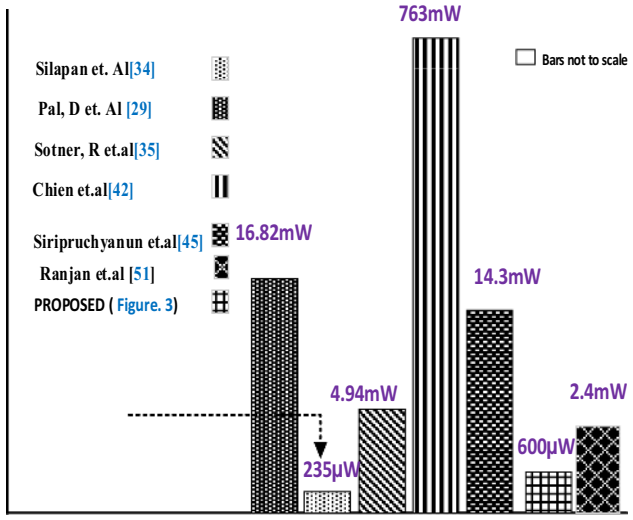

Fig. 24 Figure showing the comparative power consumption of the circuits presented in the literature and the proposed one in the Fig. 3 of this work

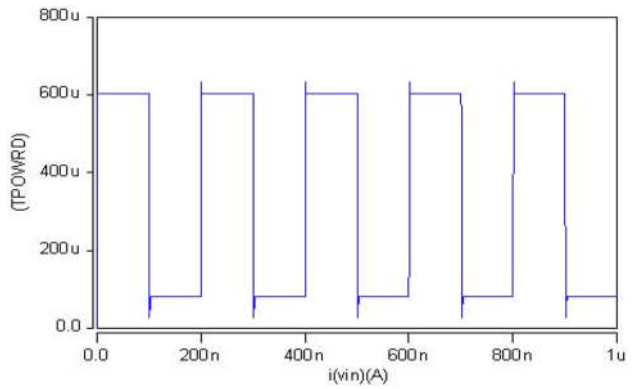

Fig. 25 Total Power Plot of the proposed squarewave circuit

differentiates this circuit scheme from the literature, is the use of Minimum number of *MOS* transistors occupied in the translinear circuit adopted. Total power consumption of the circuit is 600 µW, with ± 1 V rail to rail operating voltages. To the author's prior knowledge, the circuit (*MOS based*) presented guarantees the lowermost total power consumption amongst all the circuits presented in literature till date. However, only at [34], circuit presented using BJT's has extreme low power consumption. The reason behind the fact, that the total power consumption reported at [34] is less than the proposed circuit, is directly due to the implementation of the BJT's at the *transistor level* for Schmitt trigger device and not used as the *switch* or as active *building blocks*. Further, the application of the BJT and its dominance stem from the use in the particular application and utility. Graphical plot of total power consumption of the circuits presented in the literature and the proposed one is shown below in the Fig. 18. To the Authors prior knowledge, the proposed circuit consumes the least power among all other circuits available in the literature. Main and possible reason behind the least power consumption is the implementation of the presented circuit using the 45 nm BSIM predictive modelling technology. Use of deep sub-micron parameters enhances greatly the higher drive as well as the minimization of the leakage current of the circuits.

8 Conclusion and future work

Low voltage and low power square wave generator using CCCII + is presented in this study. The circuit was implemented using a sole capacitor and two resistors. Simulated

and Measured results of the circuit has been also detailed in the manuscript. Apart from the wide simulation analysis, the proposed circuit was also demonstrated practically using commercially available CCII, in the form of AD844 IC. A fair agreement and anticipation of theoretical and practical results was observed. Proposed circuit was passed through high level Pareto analysis with the scope of decision making. Satisfying results were obtained during the whole of the simulation processes. Presented circuit is expected to deliver sophisticated performance than the already existing in the literature. Total power consumption of the circuit is 600 µW, with ± 1 V rail to rail operating voltages. High frequency application part in the wider areas of electronics and communication are expected to be covered by the presented design. In Future, authors are making efforts to present the extended and enhanced simulations of the pre and post layouts using 45 nm technology parameters with the inclusion of DIE of the proposed circuit from the author's university lab. Finally, a compact and a minatursiated device fabricated from a local foundry is also expected to be put before the readers.

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Compliance with ethical standards

Conflict of interest The author(s) declare that they have no competing interests.

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