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A Novel Step-Up Single Source Multilevel Inverter: Topology, Operating Principle and Modulation

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***Abstract*—This paper presents a novel step-up DC to AC converter with only one power supply. These types of converters are suitable for renewable and sustainable energy applications with low input DC sources. The proposed topology has the ability of self-voltage balancing and does not apply end side H-bridge to produce a bipolar staircase waveform. Consequently, switching losses and voltage stress of semiconductor components are reduced to a great extent. A small DC voltage source can be used to achieve a high voltage high quality AC waveform through switching the pre-charged capacitors in series and in parallel. Circuit configuration and its operation principle, capacitors' charging process, thermal model, capacitances and losses calculations are discussed in details. Moreover, the comparison of the proposed circuit with the other single source multilevel converters shows that the proposed topology reduces the number of circuit elements. Finally, a laboratory 9-level prototype is built to verify the theoretical analyses and feasibility of the proposed topology. The experimental results show that the converter efficiency at 1 KW output power is 92.75 %.**

***Index Terms*— DC-AC power conversion, Single source multilevel converter, Switched-capacitor technique, Voltage step-up, Phase disposition pulse width modulation, Efficiency.**

I. Introduction

NOWADAYS, the current energy arena is changing. The generation of electrical energy through unstable/fossil sources impose irreparable damages on the environment. This issue encourages governments to use clean energy sources like solar and wind energy for producing demanded power. Variant families of power converters have been designed to connect these types of new energy systems to the electrical network and/or local loads. Among these converters, multilevel inverters (MLIs) play a critical role in converting DC power to AC power [1-3].

The idea of MLIs was introduced by Baker et al in 1970s to mitigate disadvantages of two-level inverters (i.e. low power quality and the use of high power semiconductors) [4]. Lower switching and conduction power losses, increased efficiency, and extended power range due to the high voltage capability are other benefits of the MLIs compared to the two-level inverters [5-7]. The most common types of multilevel converter topologies are diode clamped or neutral point clamped (NPC) [8], capacitor clamped or flying capacitor (FC) [9], and cascaded H-bridge (CHB). NPC and FC suffer from dc-link voltage unbalancing problem and high number of semiconductor elements, particularly when the number of voltage levels are increased [10]. There have been special attention to the CHB converter due to modularity, symmetric structure, and its simple control. However, the main drawback of the CHB is the need for large number of isolated DC sources [11].

The above mentioned converters do not have the potentiality of voltage boosting. The voltage boosting capability will be essential when the converter is designed for electric vehicles (EVs), uninterruptible power supplies (UPS), and grid connected renewable energy systems such as photovoltaic cells [12]. Low input DC voltage should be boosted to an acceptable range for these systems [13, 14]. In recent years, one of the main orientations in power electronics has been the development of step-up DC to AC switched-capacitor converters without inductors and transformers [15]. They are able to boost their small input DC voltages to high AC voltages through switching the pre-charged capacitors in series. Low weight, small size, high power density, and low harmonic contents are some benefits of these converters [15]. Nevertheless, they should be accompanied with isolation transformers where the isolation between different energy sources is required.

Figs. 1a to 1c show the switched-capacitor circuits presented in [16], [17], and [18], respectively. They are based on a series connection of a DC-DC converter and an end side H-bridge inverter. The DC-DC parts consist of series switched-capacitor units, in a way that provide the capacitors' charging potentiality

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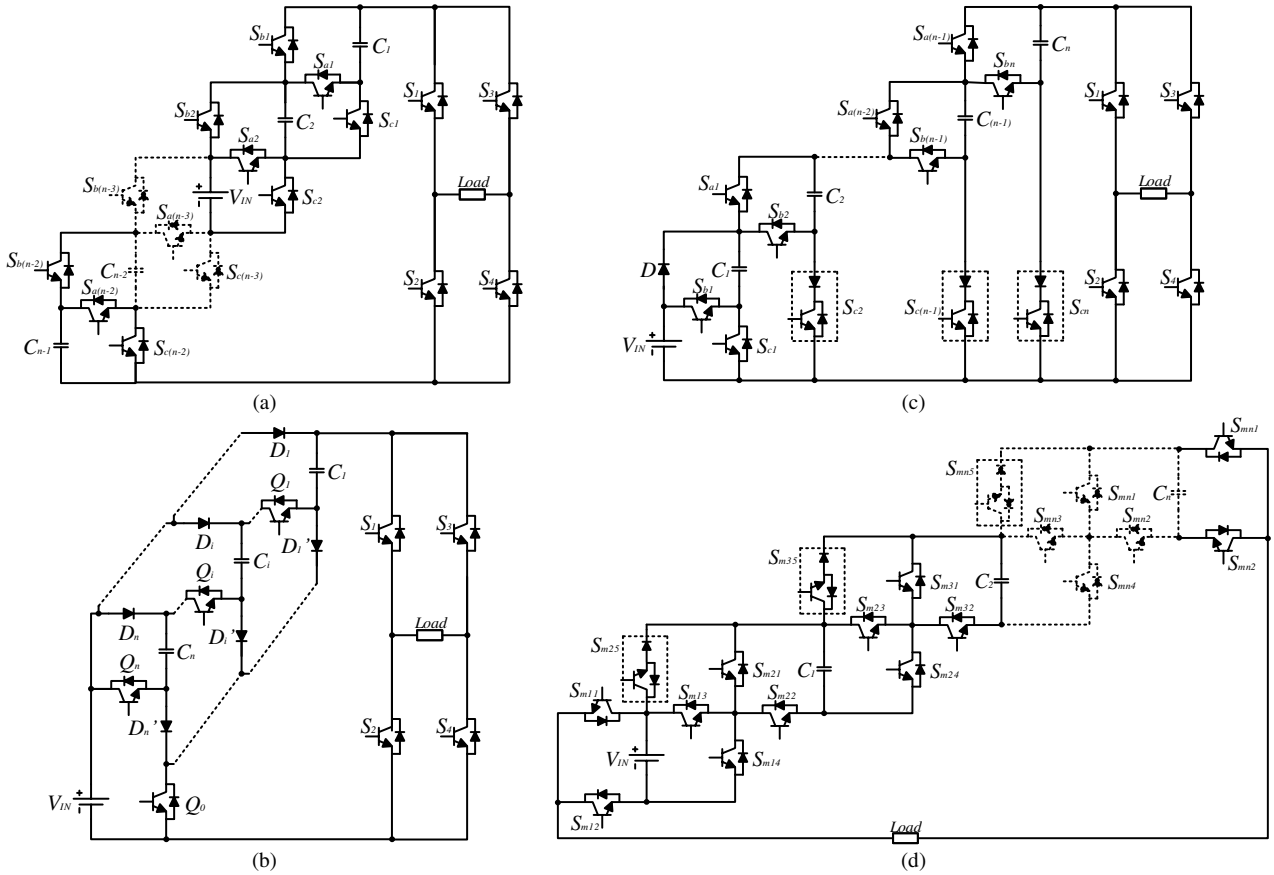


Fig. 1. Presented circuits in the recent years (a) [16], (b) [17], (c) [18], (d) [20]

in self-balancing form. Voltage boosting and applying only one power supply are among the advantages of these circuits compared to classical topologies and other modified CHB converters. However, the number of active switches and capacitors are high in these converters, which lead to increase in system cost, size and complexity. Note that [16-18] converters use end side H-bridges to produce bipolar voltage waveforms. Four H-bridge switches should withstand voltages equal to the maximum output voltage. This weakness might restrict converter applications in medium/high power ranges; because providing high voltage switches is difficult and costly [19]. [20] presented a step-up single source multilevel converter based on switched-capacitor technique in which capacitors' charging is performed in a self-balancing form (see Fig. 1d). The voltage stress of semiconductor elements, and therefore total standing voltage (TSV) is decreased in this converter; however, it uses very high number of active switches and related gate drivers.

This work presents a novel step-up single source multilevel converter based on switched-capacitor technique. Capacitors' charging in the proposed converter is performed in a self-balancing form and it generates a bipolar output voltage with no need to an end side H-bridge. The comparison of the proposed converter with other topologies in the same category shows that the number of semiconductor elements, capacitors, and TSV parameter are decreased in the proposed circuit. Due to these benefits, this circuit is an appropriate alternative for traditional/up to date multilevel converters which are applied for electric vehicle drives, renewable and sustainable energy sources, and other applications. Other sections of the paper are organized as follows: section II describes the performance of the proposed circuit, capacitors' charging process and its modulation strategy. The capacitances and power losses calculations along with the thermal analysis of the proposed 9-level converter are presented in section III. Section IV compares the proposed converter with the other presented circuits in the recent years. Section V provides achieved simulation and experimental results from a 9-level prototype. Finally, conclusions are brought in section VI.

II. Proposed Step-up Multilevel Converter

A. Circuit Configuration

Fig. 2a shows the proposed single source multilevel converter. It consists of two half-bridge (HB) inverters (RHB and LHB for the right and left sides of the converter) and m modified switched-capacitor cells (SCC) which are connected in series in the middle of the topology. The voltages produced by SCCs are transferred to the load terminals through lateral HBs. Each SCC includes two capacitors (C_u, C_d), two unidirectional power switches (S_u, S_d), and two power diodes (D_u, D_d). The proposed topology is a voltage booster in a way that the maximum output voltage can increase to any desirable level. Photovoltaic panels, batteries, and fuel cells can be applied as input power supply in this circuit. Generating a bipolar output voltage with no need to an end side H-bridge

inverter is a benefit of this topology. This feature leads to remarkable decrease of the TSV and makes the converter appropriate to perform in medium/high power applications with low input voltage sources.

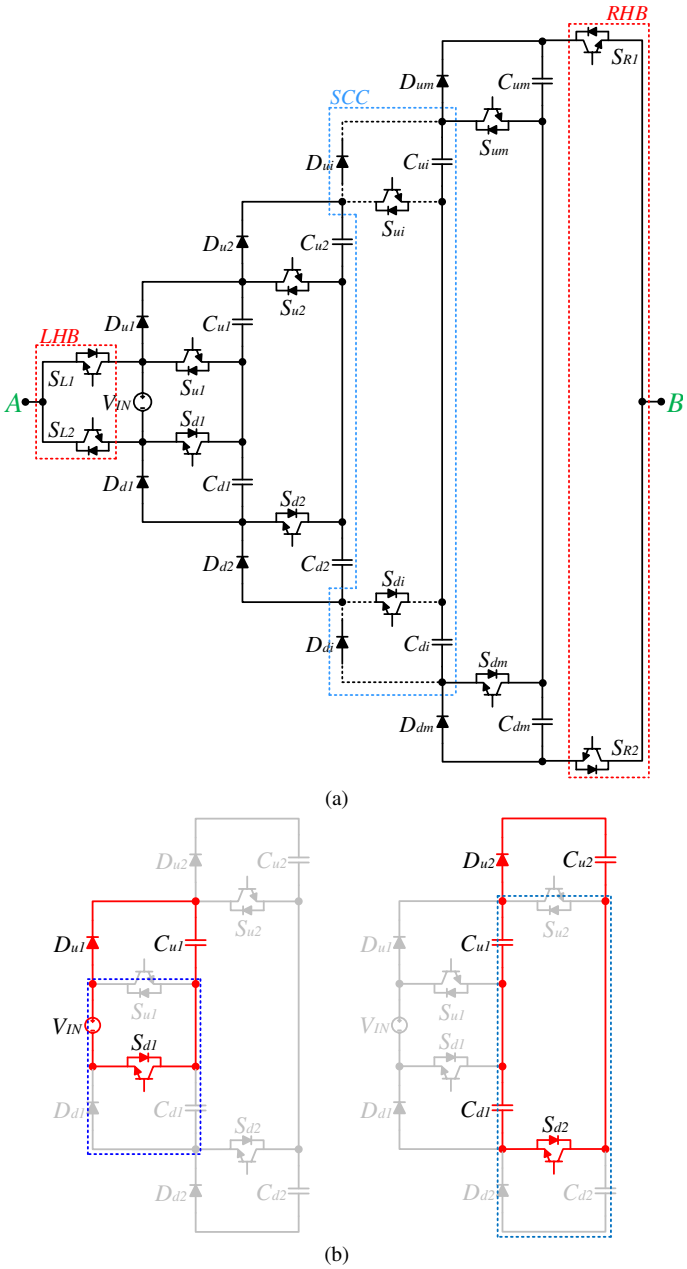


Fig. 2. (a) Circuit configuration of the proposed MLI ($V_{Load}=V_A-V_B$), (b) charging paths of the first and second SCC capacitors

B. Capacitors' Charging Process

According to Fig. 2b, C_{u1} (C_{d1}) is charged through the input power supply by turning S_{d1} (S_{u1}) on. Note that S_{u1} and S_{d1} are switched complementary. For charging C_{u2} (C_{d2}), series combination of the first SCC capacitors is applied through D_{u2} and S_{d2} (D_{d2} and S_{u2}). This procedure continues to charge all of the capacitors. For i^{th} SCC, C_{ui} (C_{di}) can be charged by series combination of $C_{u(i-1)}$ and $C_{d(i-1)}$ through D_{ui} and S_{di} (D_{di} and S_{ui}).

Therefore, by ignoring voltage drop in the charging paths, the voltage across each capacitor is obtained as follow:

$$V_{Cui} = V_{Cdi} = 2^{m-1} \times V_{IN} \qquad i = 1,2,...,m \tag{1}$$

where m is the number of SCCs. The capacitors are discharged across the load, which would be demonstrated in the next subsection. In order to preventing excessive voltage drop of the capacitors at discharging times, capacitance calculations would be presented in section III to restrict the capacitors' voltage ripple in an acceptable range. Thereby, the proposed topology does not require closed-loop controlling method or additional circuit balancer for balancing capacitors' voltage.

C. Operating Principles

The performance principle of a 9-level converter is brought in this subsection. Different voltage levels are produced based on the presented switching model in Table I. Note that 0 and 1 values are indicative of OFF and ON states of the related semiconductors, respectively. The states of the capacitors are shown by "▲", "▼", and "–" which are indicative of charging, discharging and no change modes, respectively.

TABLE I
SWITCHING MODELS AND CHARGING/DISCHARGING STATES OF THE CAPACITORS IN THE PROPOSED 9-LEVEL CIRCUIT

Voltage Levels	Switches								Diodes				Capacitors			
	S_{L1}	S_{L2}	S_{u1}	S_{d1}	S_{u2}	S_{d2}	S_{R1}	S_{R2}	D_{u1}	D_{d1}	D_{u2}	D_{d2}	C_{u1}	C_{d1}	C_{u2}	C_{d2}
$+4V_{IN}$	1	0	0	1	0	1	0	1	1	0	1	0	▲	▼	▲	▼
$+3V_{IN}$	1	0	1	0	0	1	0	1	0	1	1	0	▼	▲	▲	▼
	0	1	0	1	0	1	0	1	1	0	1	0	▲	▼	▲	▼
$+2V_{IN}$	1	0	0	1	1	0	0	1	1	0	0	1	▲	▼	–	▲
	0	1	1	0	0	1	0	1	0	1	1	0	▼	▲	▲	▼
$+1V_{IN}$	1	0	1	0	1	0	0	1	0	1	0	1	▼	▲	–	▲
	0	1	0	1	1	0	0	1	1	0	0	1	▲	▼	–	▲
0	0	1	1	0	1	0	0	1	0	1	0	1	▼	▲	–	▲
	1	0	0	1	0	1	1	0	1	0	1	0	▲	▼	▲	–
$-1V_{IN}$	0	1	0	1	0	1	1	0	1	0	1	0	▲	▼	▲	–
	1	0	1	0	0	1	1	0	0	1	1	0	▼	▲	▲	–
$-2V_{IN}$	0	1	1	0	0	1	1	0	0	1	1	0	▼	▲	▲	–
	1	0	0	1	1	0	1	0	1	0	0	1	▲	▼	▼	▲
$-3V_{IN}$	0	1	0	1	1	0	1	0	1	0	0	1	▲	▼	▼	▲
	1	0	1	0	1	0	1	0	0	1	0	1	▼	▲	▼	▲
$-4V_{IN}$	0	1	1	0	1	0	1	0	0	1	0	1	▼	▲	▼	▲

Fig. 3 shows possible current paths in the positive half cycle. It can be seen that positive voltage levels are generated with lower capacitors (C_{di}) of the SCCs. Note that only the positive half cycle is brought in Fig. 3 and the negative level paths are not demonstrated due to space saving.

D. Modulation Strategy

In this paper, a phase disposition pulse width modulation (PD-PWM) technique is used to control of semiconductor switches. The advantages of this method are uncomplicated to realize and lower total harmonic distortion [21]. According to Fig. 4, for the proposed 9-level converter, eight triangular carrier waves (V_{t1} to V_{t8}) are compared with a reference sinusoidal waveform (V_{ref}) to generate switches gate signals. The carrier waves have the same amplitude (A_t) and frequency (f_t), but their offset voltages are different. V_{t1} to V_{t4} (V_{t5} to V_{t8}) generate required switching pulses to form the positive (negative) half cycle. The algorithm to determine on-state switches in each voltage level is based on Table II.

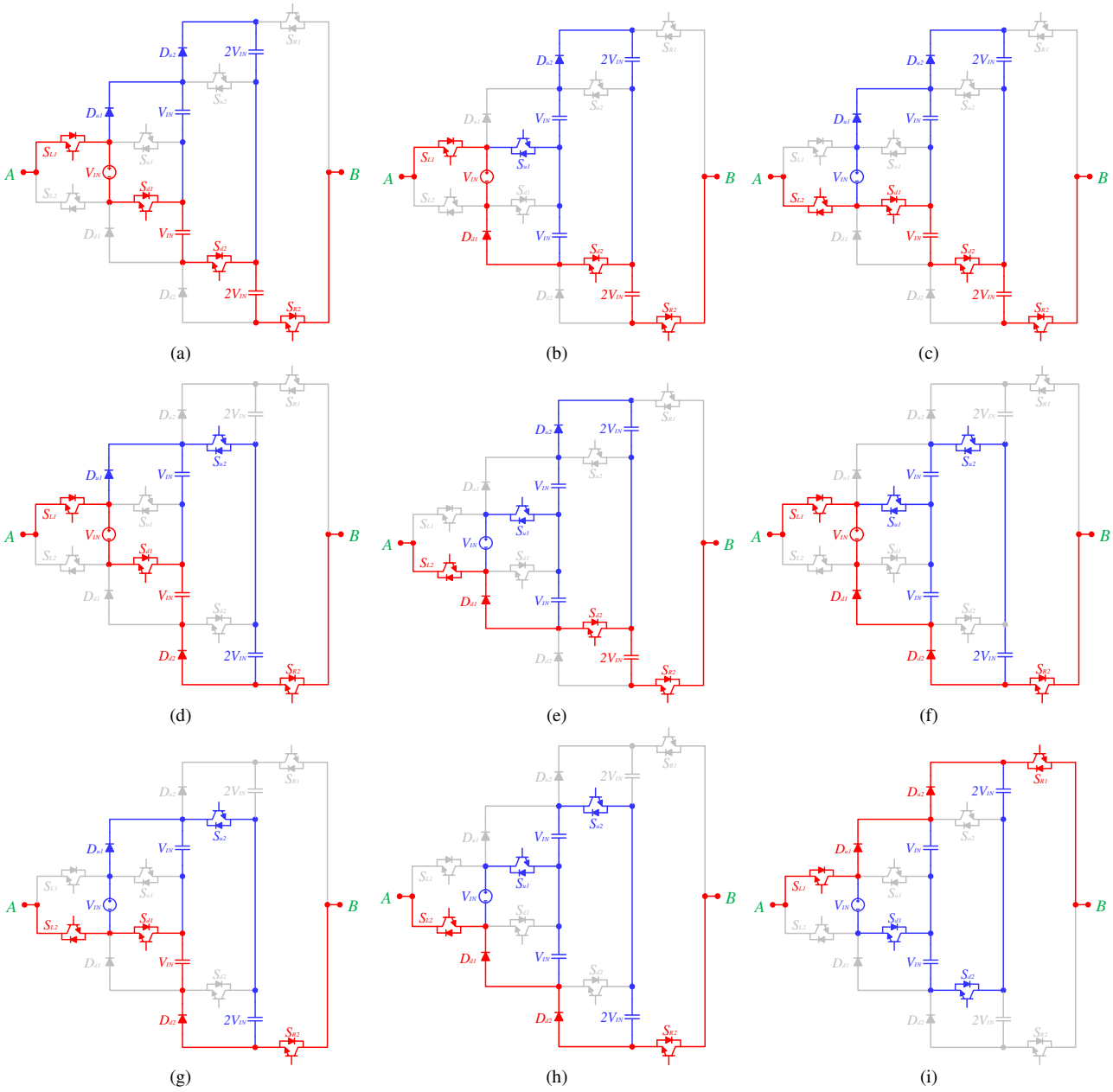


Fig. 3. Current paths for different output voltage levels (a) $+4V_{IN}$ (b) $+3V_{IN}$ (c) $+3V_{IN}$ (d) $+2V_{IN}$ (e) $+2V_{IN}$ (f) $+1V_{IN}$ (g) $+1V_{IN}$ (h) $0V_{IN}$ (i) $0V_{IN}$

III. Capacitances and Efficiency Calculations and Thermal Analysis of the Proposed Converter

A. *Determination of Capacitances*

In switched-capacitor DC-AC converters, the capacitors' voltage ripple should be retained in an acceptable range. The capacitor voltage fluctuation range is inversely proportional to its capacitance, discharging period and load value. Lower ripple leads to lower power loss and higher efficiency of the capacitor [16, 22]. As shown in Table I, there are two switching states for $+3V_{IN}$ (or $-3V_{IN}$) which lead to two different modes for C_{d1} and C_{u1}. A worse case is considered for maximum discharge time in the capacitance calculations. These intervals are t_4-t_3 and t_{10}-t_9 for positive and negative half cycles, respectively in which C_{d1} and C_{u1} are discharged. Similarly, maximum discharging intervals of C_{d2} and C_{u2} are t_5-t_2 and t_{11}-t_8, respectively.

Therefore, the maximum discharging value of each capacitor is attained by [16]:

$$\Delta Q_C = \int_{t_a}^{t_b} I_{Load}\, Sin(2\pi f_{ref} t)\, dt \tag{2}$$

in which $[t_a, t_b]$ is the discharging interval of each capacitor, and I_{Load} is the maximum load current. t_2 to t_5 and t_8 to t_{11} are calculated as follows:

$$t_2 = \frac{sin^{-1}\left(2A_t / A_{ref}\right)}{2\pi f_{ref}} \tag{3}$$

$$t_3 = \frac{sin^{-1}\left(3A_t / A_{ref}\right)}{2\pi f_{ref}} \tag{4}$$

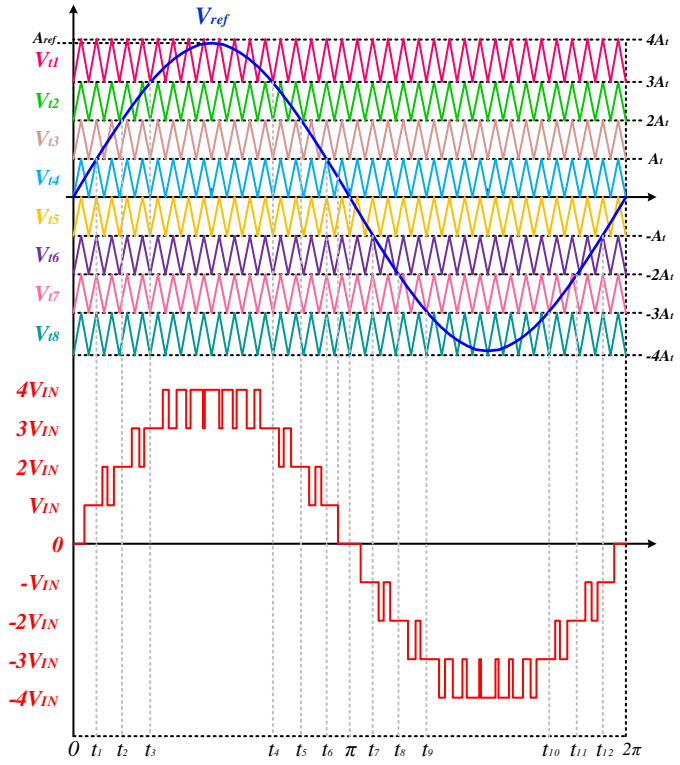


Fig. 4. PD-PWM modulation for the proposed converter

TABLE II
LIST OF THE ON-STATE SWITCHES IN EACH LEVEL

Relationship between V_{ref} and V_{ti}	On-state switches	Output voltage
$V_{ref} > V_{t1}$	$S_{L1} - S_{d1} - S_{d2} - S_{R2}$	$+4V_{IN}$
$V_{t2} < V_{ref} < V_{t1}$	$S_{L1} - S_{u1} - S_{d2} - S_{R2}$	$+3V_{IN}$
	$S_{L2} - S_{d1} - S_{d2} - S_{R2}$	
$V_{t3} < V_{ref} < V_{t2}$	$S_{L1} - S_{d1} - S_{u2} - S_{R2}$	$+2V_{IN}$
	$S_{L2} - S_{u1} - S_{d2} - S_{R2}$	
$V_{t4} < V_{ref} < V_{t3}$	$S_{L1} - S_{u1} - S_{u2} - S_{R2}$	$+1V_{IN}$
	$S_{L2} - S_{d1} - S_{u2} - S_{R2}$	
$V_{t5} < V_{ref} < V_{t4}$	$S_{L2} - S_{u1} - S_{u2} - S_{R2}$	0
	$S_{L1} - S_{d1} - S_{d2} - S_{R1}$	
$V_{t6} < V_{ref} < V_{t5}$	$S_{L2} - S_{d1} - S_{d2} - S_{R1}$	$-1V_{IN}$
	$S_{L1} - S_{u1} - S_{d2} - S_{R1}$	
$V_{t7} < V_{ref} < V_{t6}$	$S_{L2} - S_{u1} - S_{d2} - S_{R1}$	$-2V_{IN}$
	$S_{L1} - S_{d1} - S_{u2} - S_{R1}$	
$V_{t8} < V_{ref} < V_{t7}$	$S_{L2} - S_{d1} - S_{u2} - S_{R1}$	$-3V_{IN}$
	$S_{L1} - S_{u1} - S_{u2} - S_{R1}$	
$V_{ref} < V_{t8}$	$S_{L2} - S_{u1} - S_{u2} - S_{R1}$	$-4V_{IN}$

$$t_4 = \frac{\pi - \sin^{-1}\left(3A_t / A_{ref}\right)}{2\pi f_{ref}} \tag{5}$$

$$t_5 = \frac{\pi - \sin^{-1}\left(2A_t / A_{ref}\right)}{2\pi f_{ref}} \tag{6}$$

$$t_8 = \pi + t_2 \tag{7}$$

$$t_9 = \pi + t_3 \tag{8}$$

$$t_{10} = \pi + t_4 \tag{9}$$

$$t_{11} = \pi + t_5 \tag{10}$$

where f_{ref} and A_{ref} are the frequency and amplitude of reference waveform, respectively. Therefore, by considering k as the maximum acceptable voltage ripple, the capacitances are obtained based on the following relation:

$$C \geq \frac{\Delta Q_C}{k V_{IN}} \tag{11}$$

B. Power Loss Analysis in the Proposed 9-Level Converter

In this subsection, the power losses in the proposed 9-level converter are theoretically calculated. In general, in a switched capacitor converter, three types of power losses are considered, which include:

- Switching losses (P_S)
- Conduction losses caused by parasitic parameters (P_C)
- Power losses caused by capacitors voltage ripple (P_R)

Note that the maximum power losses occur in the output resistive load. Therefore, the calculations are carried out for pure resistive load.

1) Switching Losses (P_S)

The switching loss of a switch is due to overlap of its voltage (V_S) and current (I_S) when its state changes. There is a transition time (t_{on} or t_{off}) until the switch is fully turned on or off. During the transition period, both the switch voltage and current are non-zero. The turn-on power loss ($P_{S,ON}$) and turn-off power loss ($P_{S,OFF}$) of the switch S are obtained as follows [23]:

$$P_{S,ON} = f_S \int_0^{t_{on}} v_S(t)\, i_S(s)\, dt = f_S \int_0^{t_{on}} \left(\frac{V_S}{t_{on}} t\right)\left(-\frac{I_S^{on}}{t_{on}}\left(t - t_{on}\right)\right) dt = \frac{1}{6} f_S V_S I_S^{on} t_{on} \tag{12}$$

$$P_{S,OFF} = f_S \int_0^{t_{off}} v_S(t)\, i_S(t)\, dt = f_S \int_0^{t_{off}} \left(\frac{V_S}{t_{off}} t\right)\left(-\frac{I_S^{off}}{t_{off}}\left(t - t_{off}\right)\right) dt = \frac{1}{6} f_S V_S I_S^{off} t_{off} \tag{13}$$

in which f_S is switching frequency, V_S is the off-state voltage, I_S^{on} is the switch current when the switch becomes fully turned on, and I_S^{off} is the switch current prior to the turn-off of the switch. Therefore, total switching losses for the proposed 9-level converter can be attained as:

$$P_S = \sum_{j=1}^{N_{switch}} \left(P_{Sj,ON} + P_{Sj,OFF}\right) \tag{14}$$

2) Conduction Losses (P_C)

The conduction losses occur due to parasitic impedances of the circuit components including internal on-state resistance of switches (R_{ON}) and diodes (R_D), and equivalent series resistance of capacitors (R_{ESR}) [24]. According to Fig. 3, the equivalent parasitic resistive impedance ($R_{eq,j}$) existing in the current path in each output voltage level (V_j=0, $\pm 1V_{IN}$, $\pm 2V_{IN}$, $\pm 3V_{IN}$ and $\pm 4V_{IN}$) is listed in Table III.

TABLE III
THE EQUIVALENT PARASITIC RESISTANCE FOR EACH LEVEL

Output voltage level (V_j)	Equivalent parasitic resistance ($R_{eq,j}$)
0	$3R_D+R_{ON}$
$\pm1V_{IN}$	$2R_D+2R_{ON}$
$\pm2V_{IN}$	$R_D+3R_{ON}+R_{ESR}$
$\pm3V_{IN}$	$R_D+3R_{ON}+R_{ESR}$
$\pm4V_{IN}$	$4R_{ON}+2R_{ESR}$

According to Fig. 4, while $|V_{ref}|<A_t$, the output voltage level changes between zero and $+1V_{DC}$. In this case, the load current flows through three diodes and one switch (two diodes and two switches) during zero ($+1V_{DC}$) voltage level, as mentioned in Table III. Therefore, the energy loss $E_{0\&1VIN}$ occurring in time interval of $0<t<t_1$ is [24]:

$$E_{0\&1V_{IN}} = \int_0^{t_1}\left[I_{Load}\sin\left(2\pi f_{ref}t\right)\right]^2 \times \left[\left(2R_D+2R_{ON}\right)\frac{A_{ref}\sin\left(2\pi f_{ref}t\right)}{A_t} + \left(3R_D+R_{ON}\right)\left(1-\frac{A_{ref}\sin\left(2\pi f_{ref}t\right)}{A_t}\right)\right]dt \quad (15)$$

Similarly, the same energy losses occur during $t_6<t<t_7$ and $t_{12}<t<2\pi$.

While $A_t<|V_{ref}|<2A_t$, the output voltage level would be $+1V_{DC}$ or $+2V_{DC}$. In each level, the components listed in Table III are involved in the current path. Therefore, the energy loss $E_{1\&2VIN}$ during $t_1<t<t_2$ is calculated as follow:

$$E_{1\&2V_{IN}} = \int_{t_1}^{t_2}\left[I_{Load}\sin\left(2\pi f_{ref}t\right)\right]^2 \times \left[\left(R_D+3R_{ON}+R_{ESR}\right)\frac{A_{ref}\sin\left(2\pi f_{ref}t\right)-A_t}{A_t} + \left(2R_D+2R_{ON}\right)\left(1-\frac{A_{ref}\sin\left(2\pi f_{ref}t\right)-A_t}{A_t}\right)\right]dt \quad (16)$$

The same losses occur during $t_5<t<t_6$, $t_7<t<t_8$ and $t_{11}<t<t_{12}$. The same analysis can be carried out for the energy loss between $t_2<t<t_3$ ($t_3<t<t_4$) when the output voltage level changes between $+2V_{DC}$ and $+3V_{DC}$ ($+3V_{DC}$ and $+4V_{DC}$):

$$E_{2\&3V_{IN}} = \int_{t_2}^{t_3}\left[I_{Load}\sin\left(2\pi f_{ref}t\right)\right]^2 \times \left[\left(R_D+3R_{ON}+R_{ESR}\right)\frac{A_{ref}\sin\left(2\pi f_{ref}t\right)-2A_t}{A_t} + \left(R_D+3R_{ON}+R_{ESR}\right)\left(1-\frac{A_{ref}\sin\left(2\pi f_{ref}t\right)-2A_t}{A_t}\right)\right]dt \quad (17)$$

$$E_{3\&4V_{IN}} = \int_{t_3}^{t_4}\left[I_{Load}\sin\left(2\pi f_{ref}t\right)\right]^2 \times \left[\left(4R_{ON}+2R_{ESR}\right)\frac{A_{ref}\sin\left(2\pi f_{ref}t\right)-3A_t}{A_t} + \left(R_D+3R_{ON}+R_{ESR}\right)\left(1-\frac{A_{ref}\sin\left(2\pi f_{ref}t\right)-3A_t}{A_t}\right)\right]dt \quad (18)$$

Therefore, the total conduction losses for the proposed 9-level converter can be calculated as:

$$P_C = \left(4E_{0\&1V_{IN}} + 4E_{1\&2V_{IN}} + 4E_{2\&3V_{IN}} + 2E_{3\&4V_{IN}}\right)\times f_{ref} \quad (19)$$

3) Power Losses Caused by Capacitors' Voltage Ripple (P_R)

In a switched-capacitor converter, the potential difference between the input power supply (V_{IN}) and capacitor (V_C) during charging intervals leads to P_R losses. The voltage ripple across each capacitor (ΔV_{ripple}) can be stated as follow [16]:

$$\Delta V_{ripple,C} = \frac{1}{C}\int_{t_c}^{t_d} i_C(t)\,dt \quad (20)$$

where $i_C(t)$ and $[t_c, t_d]$ interval are the current and discharging period of the capacitor, respectively. For the proposed 9-level converter $[t_4, t_3]$, $[t_{10}, t_9]$, $[t_5\text{-}t_2]$, $[t_{11}, t_8]$ are the maximum discharging intervals of C_{d1}, C_{u1}, C_{d2}, and C_{u2}, respectively. Therefore, the power losses caused by the capacitors' voltage ripple (P_R) is calculated as follow [25]:

$$P_R = f_{ref}\Big/2\left(\sum_{i=1}^{2}C_{di}\Delta V_{ripple,Cdi}^2 + \sum_{j=1}^{2}C_{uj}\Delta V_{ripple,Cuj}^2\right) \quad (21)$$

Ultimately, considering (14), (19), and (21), the power losses and total efficiency of the proposed 9-level converter are calculated with (22) and (23), respectively:

$$P_{Loss} = P_S + P_C + P_R \quad (22)$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out}+P_{Loss}} \quad (23)$$

in which P_{in} and P_{out} are the converter input and output power, respectively.

The aforementioned losses are obtained numerically at different output power as depicted in Fig. 5a. In this figure, the switching losses (P_S) are multiplied by 10 to be observable. It can be seen that the conduction losses (P_C) dominate the total losses. It should be noted that R_{ON}, R_D, R_{ESR}, t_{on}, t_{off}, f_t and ΔV_{ripple} are considered 0.27 Ω, 0.05 Ω, 0.03 Ω, 58 ns, 58 ns, 4 KHz and 5% respectively for the loss calculations. The theoretical efficiency of the proposed 9-level converter is also brought in Fig. 5b. As it can be seen, the converter efficiency is above 94 % over a wide range of output power (up to 2.5 KW).

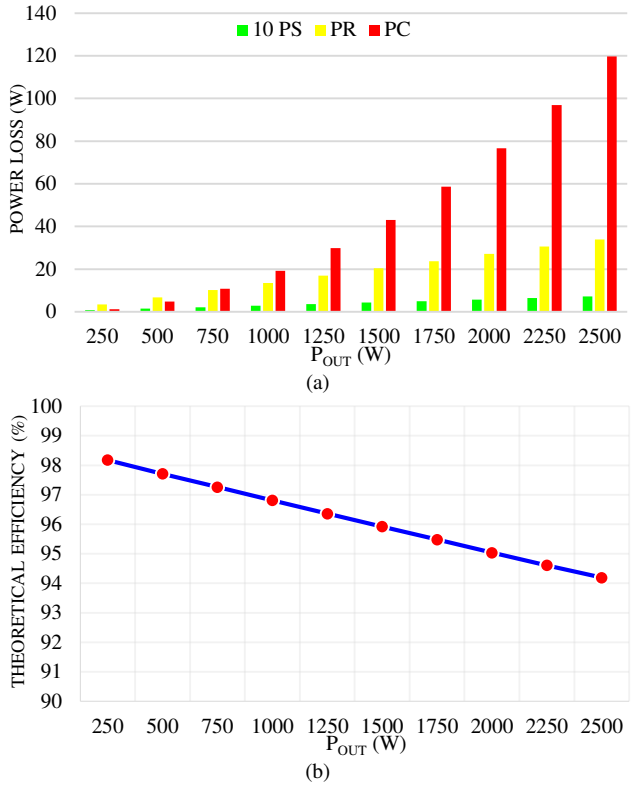


Fig. 5. (a) Power loss distribution, (b) theoretical efficiency at different output power

C. *Thermal Analysis*

The semiconductors losses act as a source of heat which leads to increasing the semiconductors' junction temperature. This influences the efficiency and lifetime of the converter [26]. For safety reasons, the junction temperature should be always under a maximum value, which is specified by the manufacturer [27]. The thermal equivalent block diagram of a single power switch and diode are indicated in Fig. 6a, in which the thermal impedance from junction to case $Z_{th(j-c)}$ is modeled as a four layers foster RC network (Fig. 6b) [28, 29].

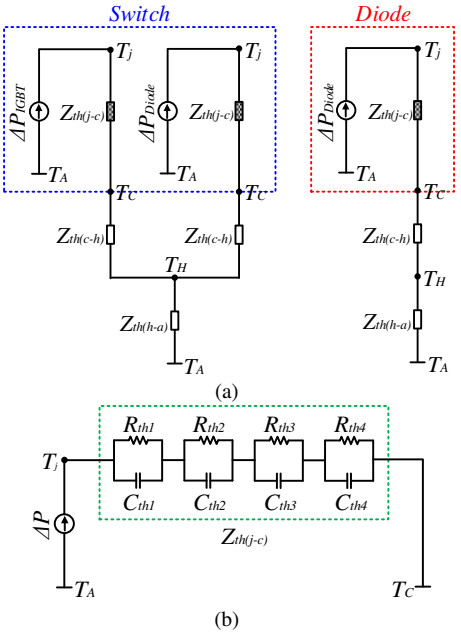


Fig. 6. (a) Thermal model of the semiconductors (b) foster model of the thermal impedance from junction to case

In these figures $Z_{th(j-c)}$, $Z_{th(c-h)}$, and $Z_{th(h-a)}$ are the thermal impedance from junction to case, case to heat sink and heat sink to ambient, respectively. The thermal parameters can be obtained from the manufacturer datasheets. Also T_j, T_C, T_H and T_A are the semiconductor junction, case, heat sink and ambient temperatures, respectively. Based on the semiconductors losses and the thermal model, the junction temperature of the converter semiconductors can be estimated by Matlab [30-32]. Herein, the 2MBI 50F-060 IGBT module manufactured by Fuji Electric is selected for the thermal analysis. It should be noted that the ambient temperature is set to 40 °C and considered constant during the converter operation.

Figs. 7a & 7b show the estimated junction temperatures of the semiconductors in the proposed 9-level converter at 2.5 KW and 10 KW output power, respectively. As it can be seen from the figures, S_{d1} and D_{d1} have the highest junction temperatures compared to the other semiconductors. The same results are valid for the upper semiconductors (i.e. $S_{u1\&2}$, $D_{u1\&2}$, S_{L1} and S_{R1}); because they are switched complementary to the lower semiconductors (see Table I).

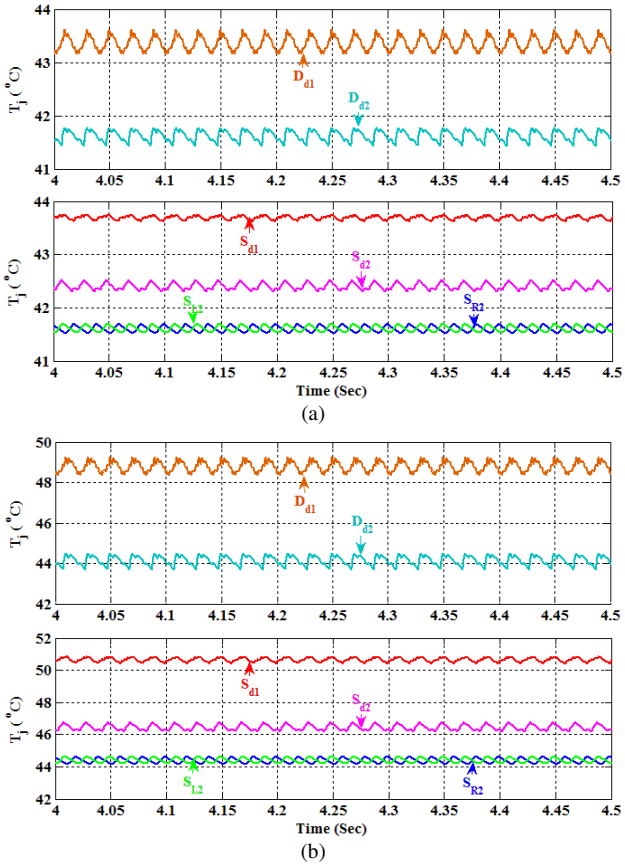


Fig. 7. Estimated junction temperature at (a) 2.5 KW output power, (b) 10 KW output power

IV. Comparison With Existing Topologies

To better illustrate the benefits of the proposed step-up converter, a comparative study is carried out between the proposed circuit and other well-known single source topologies in terms of number of semiconductors, number of capacitors, and devices voltage rating for (2n+1) levels or n-steps (see Table IV and Fig. 8).

According to Figs. 8a & 8b, to produce a definite number of levels, the proposed converter has the least number of active switches, drivers and capacitors among other topologies. This merits reduce size, cost, and complexity of the system. According to Fig. 8c, the TSV comparison of different topologies shows that the proposed circuit has the lowest TSV value due to not applying end side H-bridge. Using an H-bridge converter in [16], [17], [18] topologies for producing a bipolar voltage is considered as a disadvantage, since four H-bridge switches should withstand voltage stresses equal to maximum output voltage. This feature can limit medium/high voltage applications of these converters.

TABLE IV
COMPARISON OF THE PROPOSED CIRCUIT WITH [16], [17], [18], [20] FOR A (2N+1) LEVEL OUTPUT VOLTAGE

Comparing item	[16] (2012)	[17] (2014)	[18] (2016)	[20] (2018)	Proposed
Num. of active switches (or drivers)	3n+1	n+4	3n+1	5n-1	$2Log_2^{2n}$ +2
Num. of diodes	0	2n-2	0	n-1	$2Log_2^{2n}$ -2
Num. of capacitors	n-1	n-1	n-1	n-1	$2Log_2^{2n}$ -2
H-bridge voltage stress	$n\times V_{IN}$	$n\times V_{IN}$	$n\times V_{IN}$	No need	No need
TSV ($\times V_{IN}$)	7n-3	n^2+4n	$0.5n^2$+5n	5n-1	4n

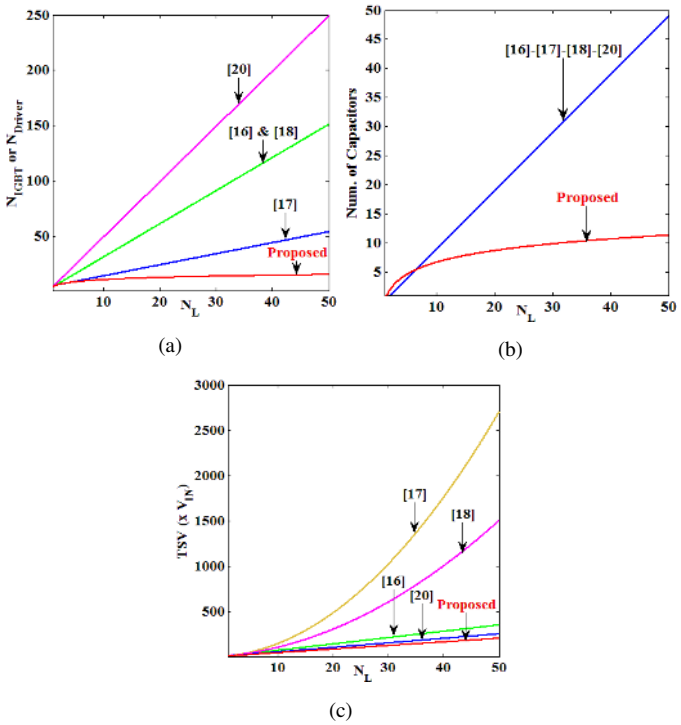


Fig. 8. Comparison of the parameters in terms of number of levels, (a) number of active switches (or drivers), (b) number of capacitors, (c) TSV

V. SIMULATION AND EXPERIMENTAL VERIFICATION

A. *Simulation Results*

For investigating the performance of the proposed single source converter, simulation results are carried out for a 9-level converter using MATLAB. Simulation parameters of the system are listed in Table V. Fig. 9 shows the output voltage and current waveforms under resistive and resistive-inductive loads. The output current is smooth at inductive load due to the filter inductance. Harmonics spectrum in Fig. 9c shows that total harmonic distortion (THD) of the output voltage is 11.83 %.

TABLE V
THE PROPOSED 9-LEVEL CONVERTER PARAMETERS IN MATLAB

Parameter	Name	Value
Elements parameters	Forward voltage drop of diodes (V_F) Internal resistance of diodes (R_D) On-state resistances of switches (R_{ON}) Capacitances (C)	0.3 V 5 mΩ 6 mΩ $C_{u1\&d1}$=2300 µF $C_{u2\&d2}$=4700 µF
Circuit parameters	Input DC source (V_{IN}) Boost ratio (n) Output frequency (f_o) Switching frequency (f_t) Load (Z_L)	70 V 4 50 Hz 4 KHz 50 Ω & 100 mH

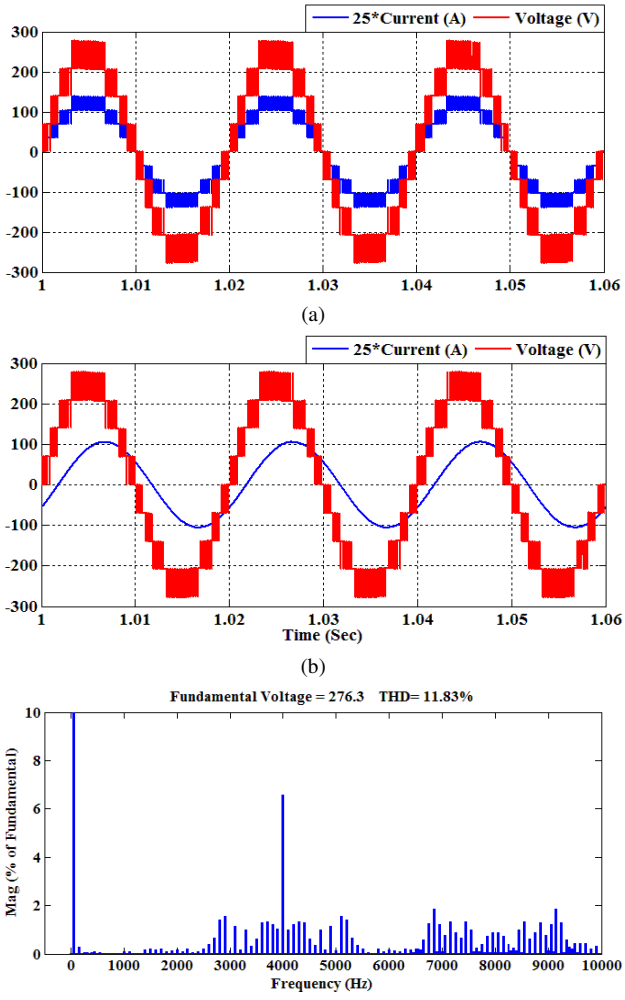


Fig. 9. Simulation results, (a) resistive load (Z_L=50 Ω), (b) resistive-inductive load (Z_L=50 Ω + 100 mH), (c) harmonics spectrum

The voltage waveforms of the circuit capacitors are shown in Fig. 10. The C_{u1} and C_{d1} voltages oscillate between 67.6 to 69.6 volts. Also, the voltage of C_{u2} and C_{d2} varies between 135 to 139.1 volts. Thereby, the capacitors' voltages are changed in an acceptable range without any external balancing circuit or complicated controlling algorithm.

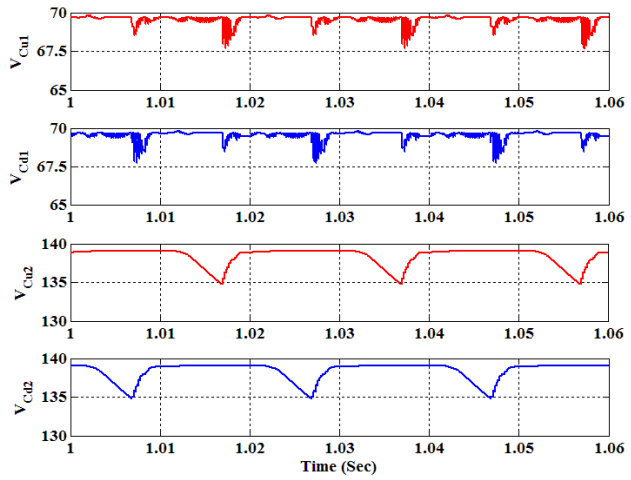
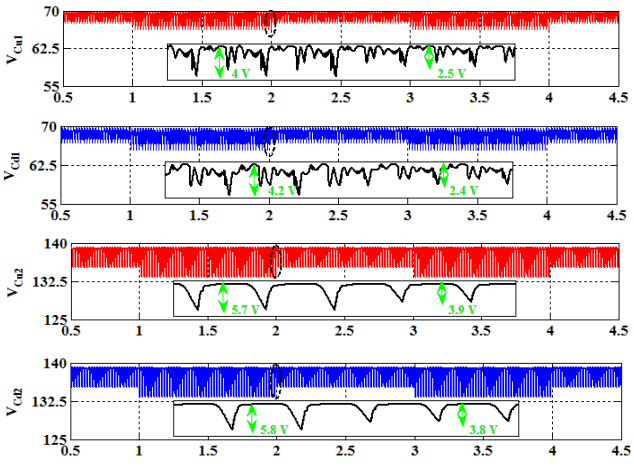


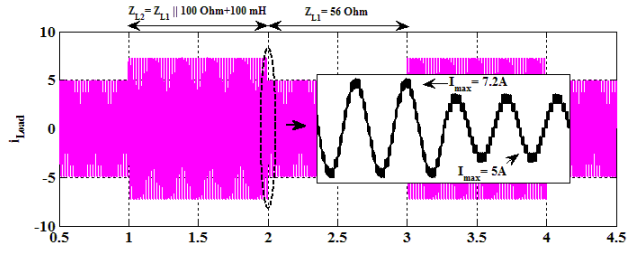
Fig. 10. The capacitors' voltages

The proposed converter is also simulated under sudden change in the load to further validate the good performance of the proposed topology in transition conditions. For this aim, following scenarios (with different power factors) are considered and the results are shown in Fig. 11. As it can be seen from Fig. 11a, the converter capacitors track their reference voltages (neglecting voltage drops in the paths) under sudden load change conditions. It should be noted that the converter input voltage is considered equal to 70 V in both scenarios.

- First scenario: the converter load changes between Z_{L1}=56 Ω and Z_{L2}= Z_{L1} || 100 Ω+100 mH frequently (Fig. 11b).
- Second scenario: the converter load changes between Z_{L1}=50 Ω+100 mH and Z_{L2}=Z_{L1} || 75 Ω+100 mH frequently (Fig. 11c).



(a)



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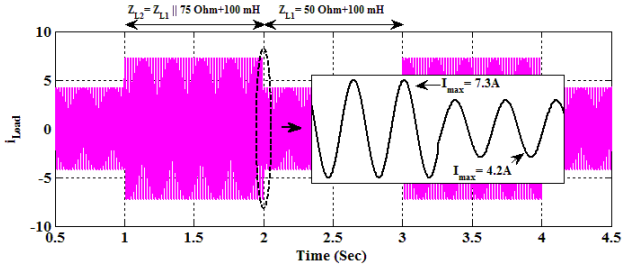
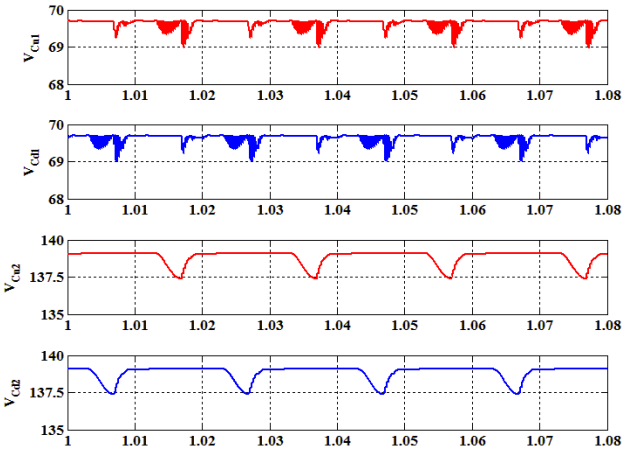


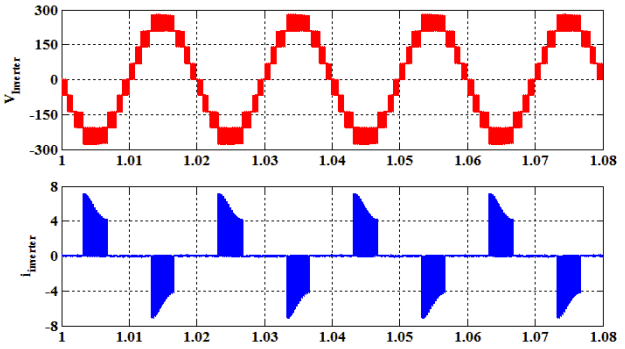
(c)

Fig. 11. The simulation results under sudden change in the load (a) the capacitors' voltages (b) first scenario (c) second scenario

Fig. 12 shows the simulation results of the proposed topology under a diode rectifier bridge which has a capacitor (C_{rec}=1.2 mF) and a resistor (R_{rec}=335 Ω) in parallel on its output. This figure confirms the good performance of the proposed converter under harmonic load conditions.



(a)



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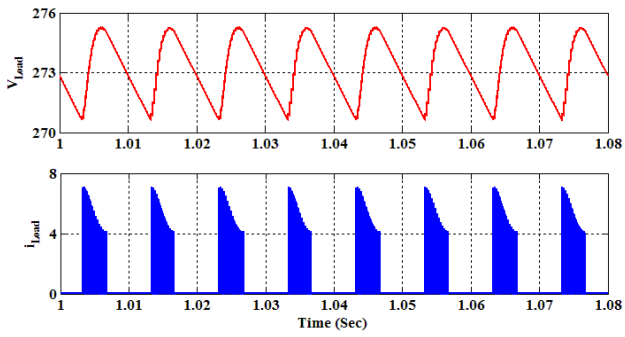


(c)

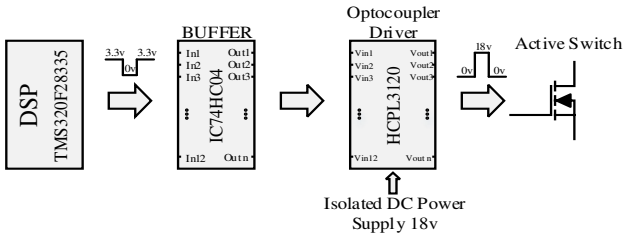
Fig. 12. The simulation results of the (a) capacitors' voltage (b) inverter output voltage and current (c) output voltage and current of the diode–rectifier bridge with R–C load (R_{rec}=335 Ω, C_{rec}=1.2 mF)

B. *Experimental Results*

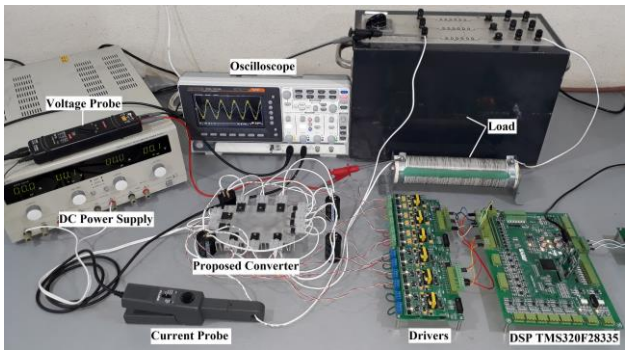
The proposed 9-level converter is also tested experimentally in order to evaluate its performance. The specifications of the prototype are listed in Table VI. In the practical tests, DSP TMS320F28335 processor generates the switches fire pulses. In order to produce ON and OFF pulses for all switches, diagram of Fig. 13a is applied in which the output pulses of the microcontroller are amplified by buffers. The isolation of the power and control sections of the circuit is performed by Optocoupler-driver (HCPL-3120). Ultimately, HCPLs output pulses are exerted between gate and emitter bases of each switch. The laboratory prototype of the proposed converter is shown in Fig. 13b.

TABLE VI
THE SPECIFICATIONS OF THE PROPOSED CONVERTER

Input DC source (V_{IN})	70 V
Boost ratio (n)	4
Output power (P_{out})	1 KW
Output frequency (f_o)	50 Hz
Switching frequency (f_t)	4 KHz
Main switches (MOSFET)	IRFP460
Diodes	RHRP15120
Optocoupler-driver	HCPL-3120
Capacitance	$C_{u1} = C_{d1} = 2300\ \mu F$ $C_{u2} = C_{d2} = 4700\ \mu F$
Main control chip	DSP TMS320F28335
Voltage probe	PINTEK DP-50
Current probe	FLUKE 80i-110s AC/DC



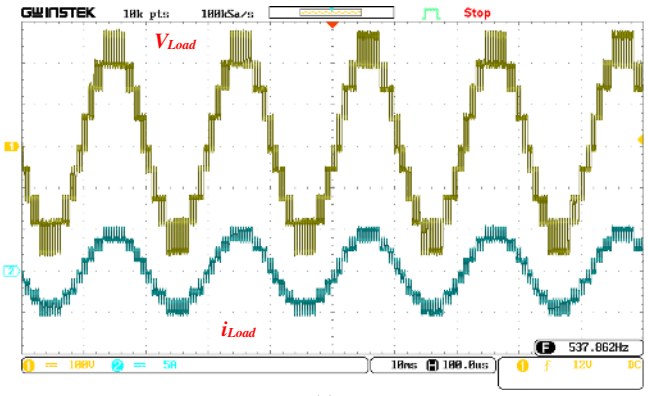
(a)



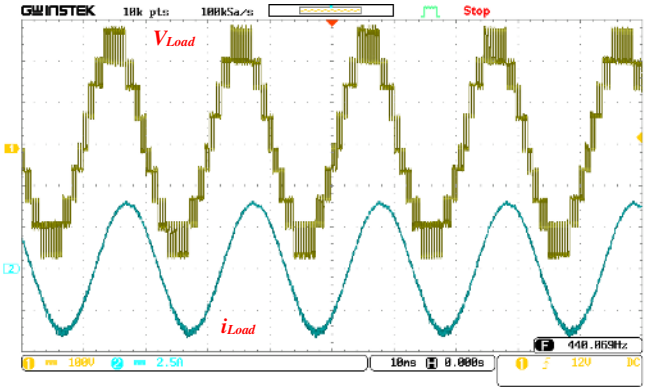
(b)

Fig. 13. (a) Switching schematic of MOSFETs, (b) experimental setup

Figs. 14a & 14b show the output performance of the proposed converter in 50 Hz fundamental frequency under resistive and resistive-inductive loads, respectively. Each voltage step is 70 V and the maximum output voltage is 280 V. Note that a power supply with 70 V magnitude is used to obtain this maximum voltage level. This voltage boosting capability is an important advantage of the proposed circuit. The capacitors' voltages are shown in Fig. 15 which demonstrate the self-balancing potentiality of the proposed circuit.



(a)



(b)

Fig. 14. Experimental waveforms, (a) resistive load (Z_L= 50 Ω) (b) resistive-inductive load (Z_L= 50 Ω + 100 mH)

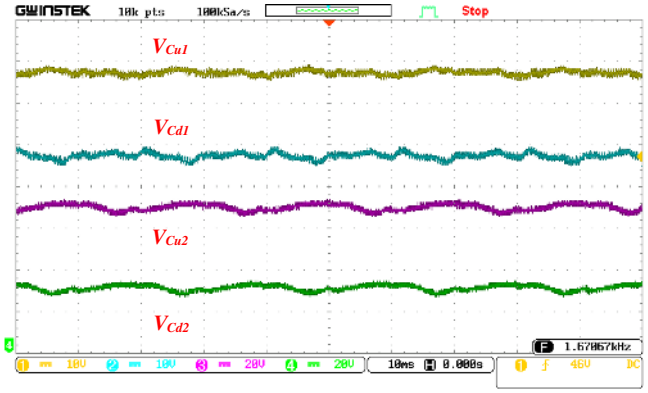


Fig. 15. Capacitors' voltages in the experimental test

Peak inverse voltage (PIV) of each switch in the proposed circuit is shown in Fig. 16. The S_{L1}, S_{L2}, S_{u1}, and S_{d1} switches withstand maximum voltages equal to the input source magnitude. S_{u2} and S_{d2} must tolerate voltage stresses twice the input source magnitude. S_{R1} and S_{R2} must tolerate the maximum output voltage. Thereby, the number of switches with PIV equal to the maximum output voltage has reduced from four (in converters with the end side H-bridge) to two.

Fig. 17 shows the experimental results of the proposed converter under sudden load change conditions (mentioned scenarios in section V.A). The experimental results of the proposed converter under a non-linear load (diode rectifier bridge with a parallel R-C load) are also brought in Fig. 18. These experimental results fully demonstrate excellent self-

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voltage balancing capability of the proposed circuit under different conditions and verify the feasibility and effectiveness of the proposed 9-level single source converter as an alternative for traditional/up to date multilevel converter topologies which are suitable for renewable and sustainable energy applications with low input DC sources.

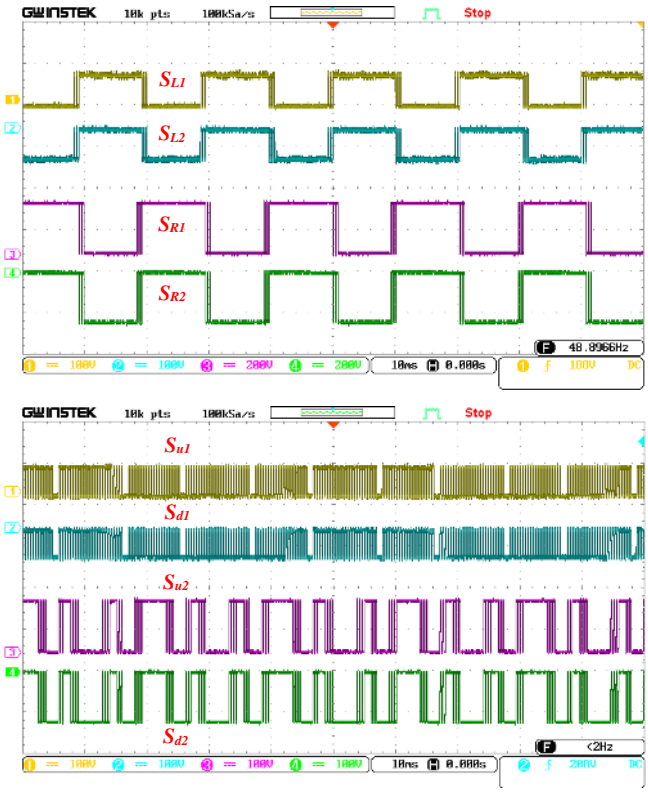
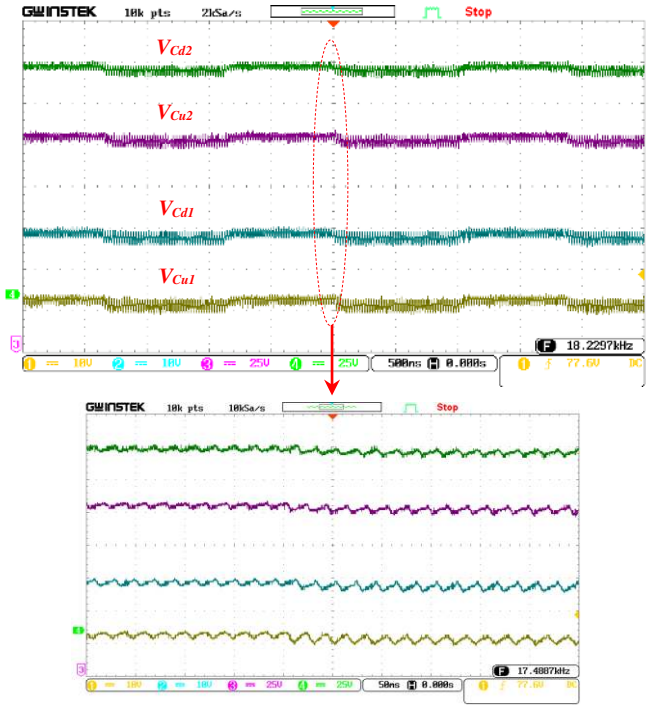
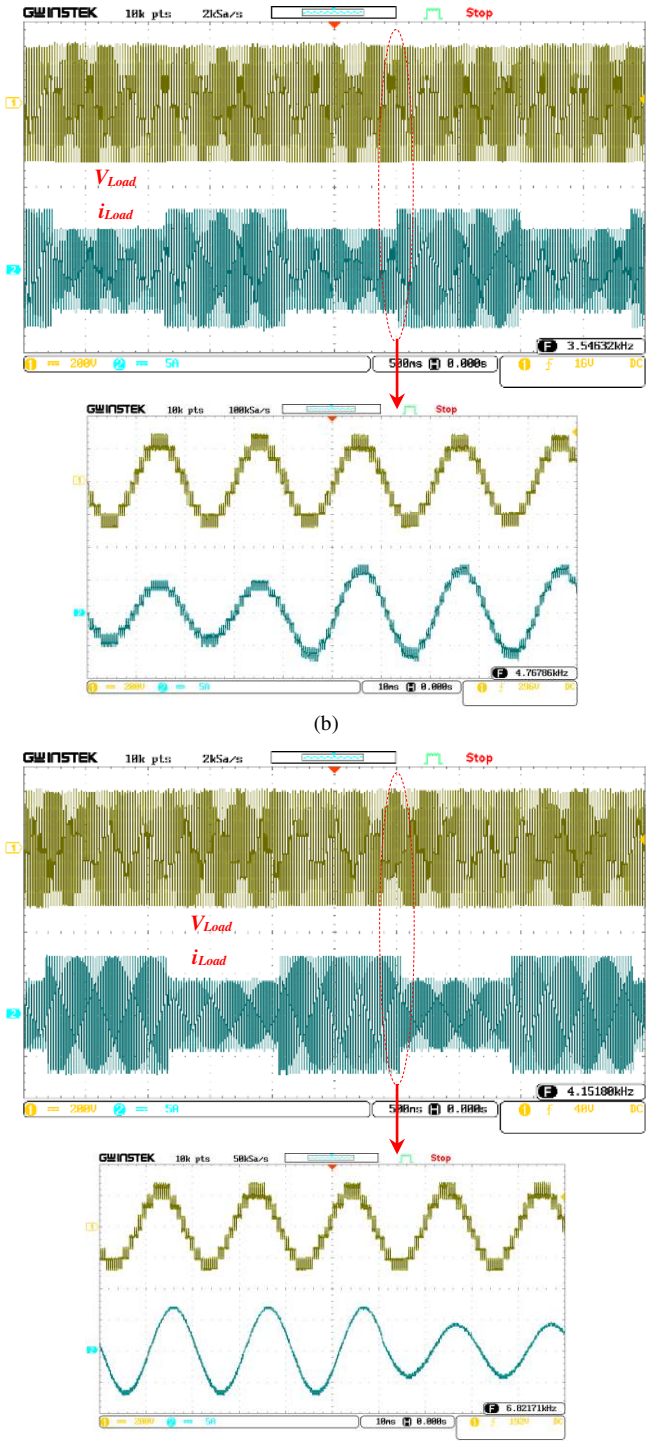


Fig. 16. Experimental results for the switches' voltage waveforms in the proposed circuit



(a)



(b)

(c)

Fig. 17. The experimental results under sudden change in the load (a) the capacitors' voltage (b) first scenario (c) second scenario

The overall efficiency of the proposed 9-level converter is investigated experimentally with different loadings as depicted in Fig. 19. For this aim, DW-6090 Power Analyzer by Lutron Electronics Company has been used. As it can be seen, the lower efficiencies have been recorded with increasing the output power. These high efficiency values are occurred as a result for the few involved components in the current flow paths. The measured efficiencies are in good agreement with theoretical ones.

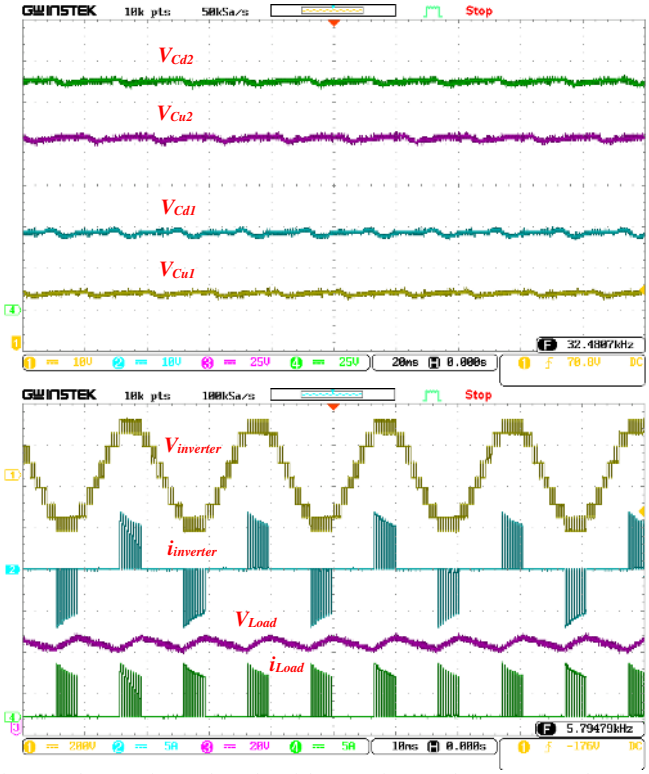


Fig. 18. The experimental results of the capacitors' voltage, output voltage and current under a diode–rectifier bridge with R–C load (R_{rec}=335 Ω, C_{rec}=1.2 mF)

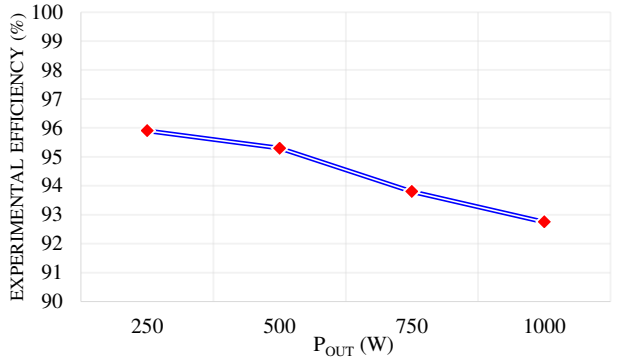


Fig. 19. Experimental converter efficiency

Finally, the proposed converter is compared with other state-of-the-art topologies in terms of the efficiency in Table VII. The data listed in the table demonstrates that the proposed topology has higher efficiency in comparison with the others.

TABLE VII
COMPARATIVE STUDY OF THE MULTILEVEL TOPOLOGIES IN TERMS OF THE EFFICIENCY

Topologies	I_{Load} (A)	P_{out} (W)	Efficiency (%)	
			Theoretical	Experimental
Proposed	1.78	250	98.18	95.9
	3.57	500	97.71	95.3
	5.53	750	97.26	93.8
	7.14	1000	96.81	92.75
[16]	0.5	5.8	85.9	84.9
[17]	3.1	247.5	Not mentioned	89.2
[18]	2	1000	90	87.5
[20]	1.9	182.4	91.7	88.93
[33]	1.29	250	93.8	Not mentioned
	5.15	1000	90.2	
[34]	3.7	219	95.23	94.18

VI. CONCLUSION

In this work a novel step-up single source multilevel inverter has been presented for renewable and sustainable energy applications. Voltage boosting without inductors and transformers, and also generating a bipolar output voltage with no need to end side H-bridge are the most important benefits of this topology. The capacitors charging are carried out in a self-balancing form. Thereby, the proposed inverter does not require additional balancing circuits or complicated modulations. Comparative investigations with other recently-presented topologies indicate that the proposed inverter can reduce the number of circuit elements and the TSV value, which result in cost reduction of the system. The applied modulation strategy, thermal analysis, capacitances and power losses calculations have been presented in details for the proposed circuit. The theoretical and experimental efficiencies have shown that the inverter efficiency is above 92 % up to output power of 1 KW. The 9-level output voltage THD has obtained 11.83 %. Finally, the appropriate performance of the proposed topology under different conditions (such as sudden change in the load and harmonic load) has been verified by simulation and experimental results on a 9-level prototype.

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