A Novel Sub-1 Volt Bandgap Reference with all CMOS

SAMEER SOMVANSHI
EEE Department
BITS-Pilani
Rajasthan
INDIA

Dr.S.C.BOSE
IC Design Group
CEERI-Pilani
Rajasthan
INDIA

Dr. ANU GUPTA
EEE Department
BITS-Pilani
Rajasthan
INDIA

Abstract: - This paper deals with the design of novel sub-1-V bandgap reference circuit using only MOS transistors in 0.18 µm CMOS technology, for a supply voltage of 1.8V. The circuit produces a voltage reference of 466.5 mV at 27^0C with a temperature coefficient of 28.4 ppm/^{0}C in the range of -20 to +120^0C. The power supply rejection of circuit is -30 dB at 8 KHz and this rejection further increase to -50 dB at 10 KHz. Power dissipation is 3.98 uW. The circuit is also tested at four process corners. Circuit is simulated with Eldo SPICE.

Key-Words: - CMOS, bandgap, subthreshold, temperature coefficient, and process corner

1 Introduction

Bandgap reference circuit is widely used to provide stable current and voltage references in analog circuits as well as in mixed signal CMOS circuits. A stable reference circuit should be robust against temperature, power supply and process variations.

Sub-1-V reference generation has got importance due to scaling resulting in shrinkage of MOS dimensions and reduction of power supply to minimize power consumption. The BGR generators that can be operated under 1-V supply have been widely used in ADCs, DRAM's, flash memories and various analog devices. In traditional BGR circuit, bipolar transistors and one or more resistors are used. BJTs that are used in BGR are in parasitic form in CMOS. Resistors occupy large area on the chip and hence increase the cost. On chip tolerance of resistors vary from 20% to 30% [6]. So we have replaced these components with MOS transistors to improve performance of BGR and to save chip area. The combination of different operating regions like subthreshold, linear and saturation of MOS suppresses the temperature dependence of voltage reference. Voltage reference is made immune to temperature, process and voltage variation on the basis of dimensions of MOSFETs in the circuit.

2 Traditional Bandgap Reference

Fig. 1 shows the traditional BGR. It comprises of both PTAT and CTAT sections. Reference voltage is given as

$$V_0 = V_{BE2} + IR_1$$
$$= V_{BE3} + M\, I_2R_2$$

where M is the multiplication factor between the W/Ls of M_4 and M_5. V_{BE} gives CTAT with roughly -1.5 mV/°K at room temperature. PTAT voltage is generated across resistor R_1 and also R_2. Thus, Vo (Vref) is approximately 1.25 V which is nearly equal to bandgap of silicon (1.12 V) at room temperature. We replaced the resistors and BJTs of the following circuit by MOS transistors to achieve efficient performance of reference and save area.

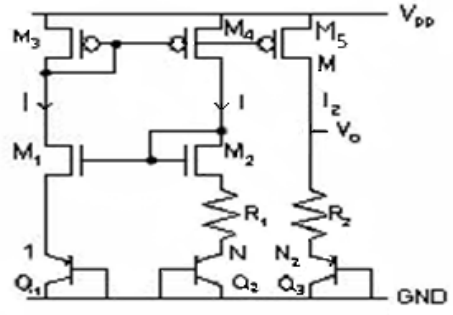

Fig 1.Traditional Bandgap Voltage Reference Circuit

3 Study of MOS in Different Regions of Operation

In subthreshold region, for $V_{gs} < V_{th}$, there flows a finite current but it exhibits exponential dependence on V_{gs} which is given by[3]

$$I_d = \mu \frac{W}{L} V_T^2 \sqrt{\frac{q\varepsilon Nch}{4\Phi b}} \exp\left(\frac{Vgs - Vth - Vc}{nVT}\right) \quad (1)$$

where Vc is the correction term which gives the difference between V_{th} in the strong inversion and subthreshold region.

Φ_b is bulk Fermi level which is dependent on temperature given by [3]

$$\Phi_b = V_T \ln\left(\frac{Nch}{ni}\right) \quad (2)$$

n_i is the intrinsic carrier concentration which is also dependent on temperature given by [3]

$$n_i^2 \; \alpha \; T^3 \exp\left(\frac{-Eg}{KT}\right) \quad (3)$$

In triode region, MOSFET behaves like a resistor whose resistance value is controlled by W/L of the transistor and by the input bias applied so long as $V_{DS}<<2(V_{GS}-V_{th})$[1]. It is given by following expression

$$R_{on} = \frac{1}{\mu Cox(\frac{W}{L})(Vgs-Vth)} \quad (4)$$

without considering the early effect.

Threshold voltage decreases by 2mV for every 1° C rise in temperature which results in increase in the drain current[12]. However, mobility decreases with temperature given by $\mu \alpha T^{-1.5}$ due to lattice scattering (vibration of lattice) in the silicon crystal over -173 °C to +127° C and its effect is dominant one, due to which there is decrease in drain current[10,11] .This can be used to anneal the change in current caused in the subthreshold region.Thus due to decrease in drain current with temperature in triode results in increase in their drain potentials.

For verifying the above equations appropriate transistor configuration was simulated in Cadence environment from -20 °C to +120° C. Figures 2,3 show the Vout (i.e.V_{ds}) of a MOSFET operated in different regions of operations. It can be seen from these figures that MOSFET has PTAT behavior in triode [9] and in subthreshold region it has CTAT behavior [3]. Simulator used is Eldo SPICE with netlist generation in Cadence Virtuoso Schematic.

Following numerical data were obtained:
Change in Vds = - 0.03 mV/C for subthreshold region; that for triode region is +1.66 mV /C.

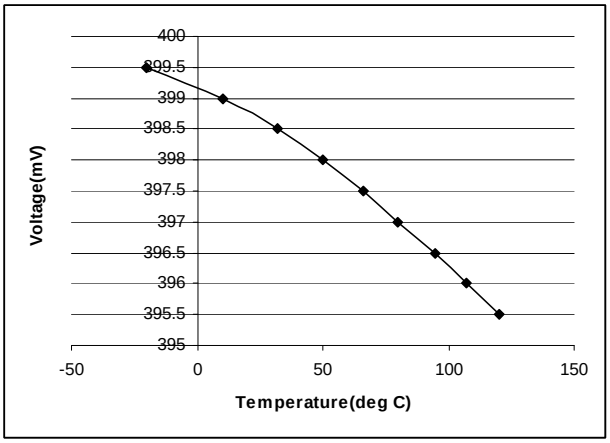

Fig.2 V_{ds} vs. temperature for MOS in subthreshold region

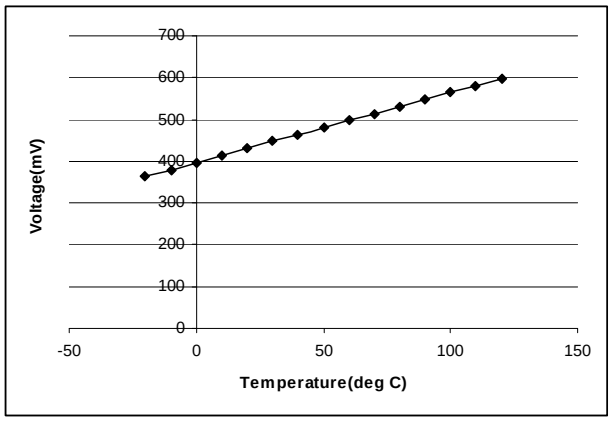

Fig.3 V_{ds} vs. temperature for MOS in linear region

4 CMOS Voltage Reference

The proposed circuit is shown in Fig.4. V_{dd} has been chosen to be 1.8 V for the design and the technology is 180 nm. Supply independent biasing has been obtained by choosing W/Ls = 10µ/20µ for four transistors M_1, M_2, M_3 and M_4 (Fig. 4). This scheme is used for high power supply rejection [1]. All four transistors are always in saturation. Current through the circuit is governed by these four transistors.

M_5 and M_6 are operated in triode region; both behave as voltage controlled resistors. Here, two transistors are used which maintain symmetry in the circuit. The gate bias of 1.10 volt for these transistors obtained from the common gate node of M_1 and M_2 is sufficient to keep M_5 and M_6 in triode region. The MOS M_7 and M_8 are in subthreshold region where they behave as BJTs of traditional BGR. Widths of these transistors need to be very large to ensure that these are in subthreshold region.

$V_{gs7,8}$ of M_7 and M_8 produces CTAT voltage in subthreshold region. $V_{ds\ 5,6}$ of M_5 and M_6 produces PTAT voltage in triode region. We assume that there is no contribution of M_1, M_2, M_3 and M_4 to the variance of V_{ref} with temperature. The final analytical expression of reference over which the addition of both PTAT voltage and CTAT voltage occurs is given by

$$V_{ref} = V_{gs7,8} + V_{ds5,6} \quad (5)$$

$V_{gs7,8}$ is obtained by manipulating equation (1) and $V_{ds5,6}$ by I_dR_{on} , substituting the value of R_{on} from equation (4) resulting into,

$$V_{ref}=nV_T\ln(\frac{Id}{\frac{W8}{L8}Is})+V_{th}+V_c+\frac{Id}{\mu Cox(W6/L6)(Vgs-Vth)} \quad (6)$$

Where $Is = a\mu V_T^2 \sqrt{\frac{q\ e\ N_{ch}}{4\Phi_b}}$

where a is empirical constant which is found by simulation.

Electron mobility is given by [11],

$$\mu(T) = m\, T^{-1.5} \quad (7)$$

where m is proportionality constant .

Taking first order approximation for finding threshold voltage,

$$V_{th}(T) = -0.002\, T + V_{th0} + b \quad (8)$$
$$= -0.002\, T + c$$

Here , $c = (V_{tho} + b)$ is constant

where V_{th0} is the threshold voltage at 0^0C temperature, b is the conversion factor from degree Celsius to degree Kelvin.

The derivative of Is is derived as,

$$\frac{d\ln Is}{dT} = \frac{d[\ln(\mu V_T^2 \sqrt{\frac{q\, e\, N_{ch}}{4\Phi_b}})]}{dT} \quad (9)$$

$$= \frac{(3 + \frac{Eg}{kT})}{8T \ln(\frac{Nch}{T\sqrt{PT \exp(-Eg/2KT)}})} \quad (10)$$

where P is proportionality constant of equation (3)

Taking the derivative of V_{ref} with temperature,

$$\frac{dVref}{dT} = \frac{nk}{q}[T \frac{-(3 + \frac{Eg}{kT})}{8T \ln\left(\frac{Nch}{T\sqrt{PT \exp(-\frac{Eg}{2KT})}}\right)} - \ln\frac{W_8}{L_8} - \ln I_s + \ln I_d] + \frac{Id}{Cox(\frac{W_6}{L_6})} [\frac{-0.002\, T^{\frac{3}{2}}}{m(Vgs+0.002T-V_{th0})^2} + \frac{3\sqrt{T}}{2m(Vgs+0.002T-V_{th0})}] - 0.002 \quad (11)$$

$= 0$ for minimum V_{ref} at temperature 27^0C between -20^0C to $+120^0$C.

Simplifying above equation results into,

$$\frac{nk}{q}[T \frac{-(3 + \frac{Eg}{kT})}{8T \ln(\frac{Nch}{T\sqrt{PT \exp(-Eg/2KT)}})} - \ln\frac{W_8}{L_8} - \ln I_s + \ln I_d] = \frac{-Id}{Cox(\frac{W_6}{L_6})} [\frac{-0.002\, T^{3/2}}{m(Vgs+0.002T-V_{th0})^2} + \frac{3\sqrt{T}}{2m(Vgs+0.002T-V_{th0})}] + 0.002/(nk/q) \quad (12)$$

$$\frac{W_8}{L_8} = \exp\{\frac{q\, I_d\, L_6}{W_6 C_{ox} nk}[\frac{-0.002\, T^{3/2}}{m(Vgs+0.002T-V_{th0})^2} + \frac{3\sqrt{T}}{2m(Vgs+0.002T-V_{th0})}] - \frac{(3 + \frac{Eg}{kT})}{8 \ln(\frac{Nch}{T\sqrt{PT \exp(-Eg/2KT)}})} - \ln I_s + \ln I_d - 0.002/(nk/q)\} \quad (13)$$

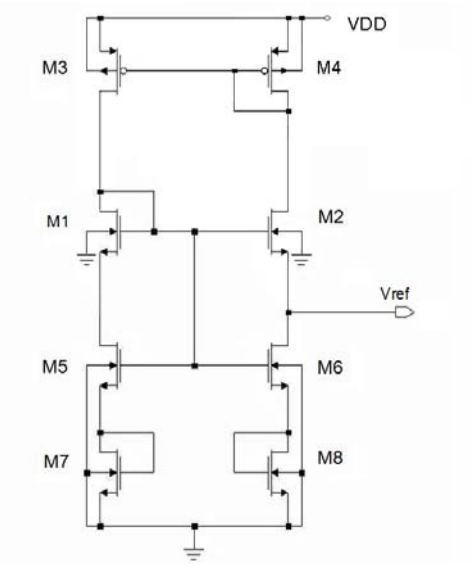

Fig 4. Proposed Bandgap Reference Circuit

From equation (13), we get the dimensions of $M_{7,8}$ with respect to $M_{5,6}$. These values are found and mentioned in experimental results.

5 Experimental Results and Observations

Initial current is set by four transistors M_1, M2, M_3 and M_4. This comes out to be 6.1uA. When this loop is connected in circuit, current changes to 1.11 uA. The ratio is given by equation (13) which is found at temperature 27^0C.

A 180 nm CMOS technology is used. Process parameters and device parameters are obtained from BSIM3 model of given technology. These are N_{ch} = 3.9 x 10^{17} cm^{-3} , n_i = 1.77 x 10^{10} cm^{-3}, E_g is 1.1eV, C_{ox} found at t_{ox} = 4.08 nm, n =1, k is Boltzmann constant, c = - 46 mV, By simulation, we got Id = 1.11 uA, V_{th} = 434.98 mV, Vgs = 306 mV, a = 409.28, m comes around 272.2, mobility at temperature of 27^0C = 0.0523 m^2/V-s, Is = 22.22 nA. Putting all the values in equation (13), the values of W_6/L_6 were varied to get optimum value of W_8/L_8. This ratio comes out to be 33.11. If value of length is 20um, the value of width comes up around 662.2um. This is followed by a graphical approach in which W/Ls of M_5 and M_6 were varied to get the minimum temperature coefficient (figure 5). Accordingly, W/Ls of M_7 and M_8 transistors were also varied so as to get minimum temperature coefficient (figure 6). Simulated values show that W_8 is 618 um. Thus by graphical method a small error of 7.1 % in W_8 is corrected.

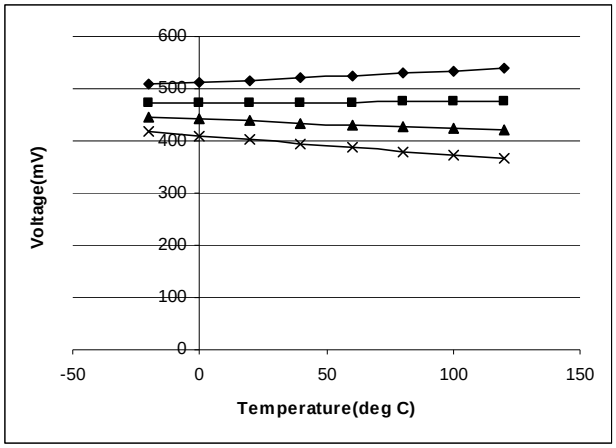

Fig 5. Variation of V_{ref} with temperature for different values of $W/L_{5,6}$

Figure 5 shows the variation of V_{ref} with temperature from -20 to 120 degrees for different values of $W_{5,6}$. In this figure, second curve (from the top) which corresponds to $W/L_{1,2,3,4}$ = 10u , $W_{5,6}$ = 2.13u , $W_{7,8}$= 800u shows least variation with temperature.

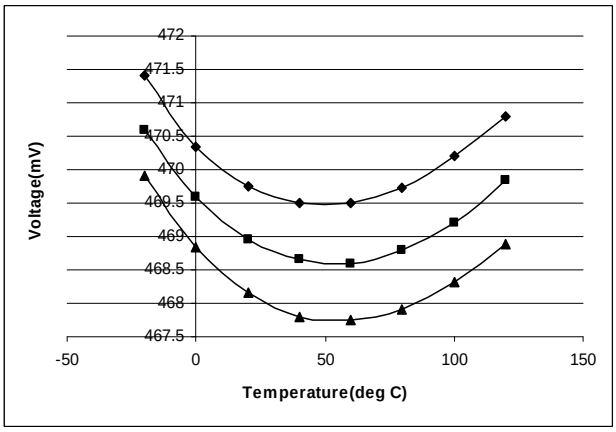

Fig 6.Variation of V_{ref} with temperature for different values of $W_{7,8}$

Widths of M_7 and M_8 are varied from 500u to 700u by keeping other dimensions constant and the results are in depicted in figure 6. From these results it has been observed that for $W_{7,8}$= 600u and 700u variation of Vref with temperature is less compared to other curves. Calculated values of the temperature coefficient for these two curves are 4265.3 ppm and 4594 ppm respectively. Further finer variations led to $W_{5,6}$ = 618µm having temperature coefficient equal to 3987 ppm. Thus final dimensions are

$W/L_{1,2,3,4}$ = 10u /20u,
$W/L_{5,6}$ = 2.13u /20u,
$W/L_{7,8}$ = 618u /20u .

The circuit can also be operated as current source giving a current 1.1 uA and power supply attenuation (dc) is -110 dB.

The output impedance of circuit is 35.61 Mega ohms. The circuit is tested for different resistive and capacitive loads. For resistive load of more than 100 Mega ohms, a small increase in temperature coefficient was found and for capacitive load, PSR actions at 10 KHz for -30 dB. The circuit has been tested for the temperature range as mentioned earlier. The circuit was also tested at four process corners such as FF, SS, FS and SF and checked for the temperature coefficient.

5.1 Temperature Variation from -20 to 120 deg Celsius

Having decided the W/Ls of all the transistor**,** the final temperature variation resulted parabolic behavior (figure 7) with minimum V_{ref} =466.38 mV at 45^0C and maximum of V_{ref} = 468.24 mV at -20^0 C. Small fluctuation of the order of 1.86 mV has been observed in Vref over the total range of temperature. This is equivalent to 28.4 ppm/C or 0.39% which is a very good figure of merit for bandgap reference circuit.

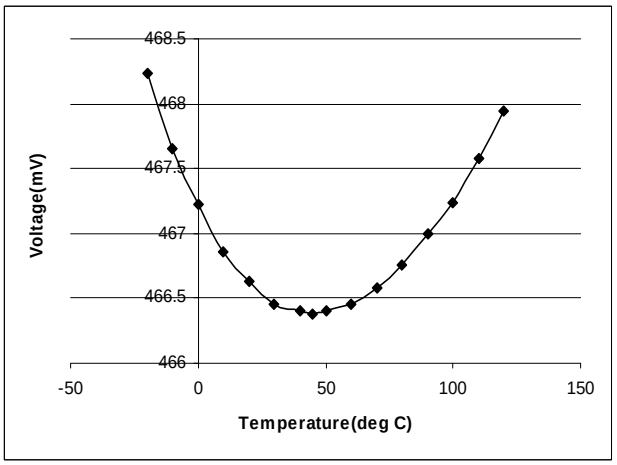

Fig 7. Final variation of Vref with temperature

5.2 Impact of Process Variations

Process parameters such as threshold voltage, mobility, etc. are different functions of temperature at different process corners. So, the bandgap reference should show minimum variation at different process corners. At four process corners (FF, SS, FS and SF) numerical values of variations in V_{ref} (in ppm/^{0}C) obtained are 35, 23.1, 31.1 and 38 respectively. Thus these values show voltage variation at four process corners with respect to temperature well under acceptable standards. Comparison of the present work has been made with other work of sub-1-V generation and summarized in the following table:

	This work	[4]	[7]	[8]
CMOS Technology	0.18 µm	0.25 µm	0.25 µm	0.25 µm
Supply voltage (In Volt)	1.8	0.85	1.2 to 3	0.9
Temperature Coefficient (In ppm/^{0}C)	28.4	58.1	83.33	19.5
Temperature range (^{0}C)	-20 to +120	-20 to +120	-20 to +100	0 to +100
Defined at all process corners	Yes	No	No	No
Use of only MOS transistors	Yes	No	Yes	No

6 Conclusions

The design of reference with Vref of 466.5 mV with Vdd = 1.8 V, temperature coefficient of 28.4 ppm/C, PSR of -30dB at 8 KHz has been done successfully. The proposed circuit contains 9 MOSFETs and has no resistors and BJTs. This has been done using in 0.18 µm CMOS technology. Layout is extracted in Cadence environment which is verified through DRC and LVS.Post layout simulations are presented after PEX extraction. This circuit can be efficiently used as voltage reference in the chip; also it can be used to provide bias to any of the transistors in the circuit. Circuit is tested at different loads such as resistive and capacitive. It is efficiently able to drive the loads. The circuit can also be operated as current source giving a current 1.11 uA and power supply attenuation (dc) is -110 dB .The architecture for reference generation presented here proves to be robust against process, supply voltage and temperature (PVT).

Summary of circuit performance:

Technology	0.18 um CMOS
Supply Voltage(VDD)	1.8 V
Voltage reference (at 27 ^{0}C)	466.5 mV
Temperature coefficient	28.4 ppm/^{0}C
Power supply rejection	-30 dB at 8KHz
Power Dissipation	3.98 uW
Layout Area	0.22 mm^2

Post Layout Simulations:

Temperature coefficient	38 ppm/^{0}C
Power supply rejection	-27 dB at 8 KHz
Power Dissipation	3.88 uW
Voltage reference(at 27 ^{0}C)	463.46 mV

7 Acknowledgements

The authors wish to thank to the reviewers of this paper which helped in modification of it. The authors wish to thank Dr.H.D.Sharma (Scientist, CEERI-Pilani) for his sincere help. The authors also wish to thank Mr.Rakesh Dhakla and Mr. Balraj Singh for their help in making circuit simulations.

8 References

[1] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, First Ed., New Delhi: Tata McGraw -Hill, 2004.

[2]Toshihiro MATSUDA, Ryuichi MINAMI, Akira KANAMORI, Hideyuki IWATA, Takashi OHZONE,Shinya YAMAMOTO, Takashi IHARA and Shigeki NAKAJIMA' "A Temperature and Supply Voltage Independent CMOS Voltage Reference Circuit" IEICE Transactions on Electronics Vol.E88-C,no.5 May 2005.

[3] G.Giutolist, G.Palumbo, M.Criscione, F.Cutri, "A New Voltage Reference Topology Based on subthreshold MOSFETs" IEEE Journal of Solid-State Circuits, Vol. 38, no.1 January 2003.

[4]M.D. Ker, J.S.Chen and C.Y. Chu, "A CMOS

Bandgap Reference Circuit for Sub-1-V Operation without Using Extra Low-Threshold-Voltage Device,"IEICE Trans. Electron., Vol.E88-C,no.11 November 2005.

[5]Tao Li, Bhaskar Mitra and Kabir Udeshi,"A Low Voltage Bandgap Reference Circuit with Current Feedback" EECS 413 Project.

[6]R. Dehghani and S.M. Atarodi, "A New Low Voltage Precision CMOS Current Reference with No External Components," IEEE Tran. on Circuits and Systems- II: Analog and Digital Signal Processing, vol. 50, no. 12, pp. 928-932, Dec. 2003.

[7]Tetsuya HIROSE, Toshimasa MATSUOKA, Kenji TANIGUCHI, Tetsuya ASAI, Yoshihito AMEMIYA, "Ultralow-Power Temperature-Insensitive Current Reference Circuit" Department of Electrical Engineering,Hokkaido University.

[8]M.D.Ker, J.S.Chen, "New Curvature-Compensation Technique for CMOS Bandgap Reference With Sub-1-V Operation" Circuits and Systems, 2005.ISCAS2005. IEEE International Symposium on Vol.4 Page(s): 3861 - 3864, 23-26 May 2005.

[9] Afshin Haft-Barbadian, "Basic and advanced current references" University of Toronto.

[10]Millman, Halkias, *Integrated Electronics- Analog and Digital Circuits and Systems*, Tata McGraw-Hill.

[11] B. Streetman, S. Banerjee, *Solid State Electronic Devices*, Pearson Education

[12]A. Sedra , K. Smith , *Microelectronics Circuits*, Oxford University Press,2004.