A novel technique to determine the gate and drain bias dependent series resistance in drain engineered MOSFET's using one single device

A Novel Technique to Determine the Gate and Drain Bias Dependent Series Resistance in Drain Engineered MOSFET's Using One Single Device

Jan A. M. Otten and François M. Klaassen

Abstract— **A new measurement method is explained for the extraction of the source and drain series resistance of drain engineered MOSFET's from their low frequency ac characteristics as a function of gate and drain bias using only *one single MOSFET*. Experimental results indicate, the effect of drain voltage dependent series resistance is relevant both in the ohmic and in the saturation region of the MOSFET. In addition the new measurement method is extended in such a way that it can be used to measure the series resistance as a function of gate bias only at low drain bias. Comparison of this single transistor measurement technique with other methods, needing a set of identical transistors with different channel lengths, shows that our method gives equal results. Finally attention is also given to the modeling of the series resistance in the ohmic and saturation region. For both regions simple, accurate compact model expressions have been derived.**

I. Introduction

THE parasitic source and drain resistances (R_s and R_d, respectively) give a serious limitation to the maximum current of drain engineered devices like the Lightly Doped Drain (LDD) or the Double Diffused Drain (DD) MOSFET. Because of the influence of the series resistance on the device characteristics, it is necessary to measure the value of the series resistance. In the past few years several techniques [2]–[4] have been presented to measure the effective channel length and series resistance of MOSFET's, some even as a function of the gate voltage at low drain bias [5], [6]. They have been developed because of the inaccuracy involved in using standard methods as MOSFET channel dimensions are reduced to below 1.0 μm.

Though already a measurement method was presented recently [7], based on the 'paired V_g method' [6], to measure the drain voltage dependent R_d, it was already demonstrated [8] that this 'paired V_g method' can give incorrect results even at low drain bias. In addition applying this method at higher drain voltages, the neglect of lateral electric field will increase the error [9]. In spite of the inaccuracy of this latter method it gives us an indication that R_d is indeed drain voltage dependent. In [9] it was shown by means of device simulations that this is indeed the case. In this paper the drain and gate voltage modulation of the series resistance is analyzed in detail with emphasis on the new measurement technique.

The organization of this paper is as follows: the second section discusses the determination of R_d as a function of drain bias by means of a two dimensional numerical simulation using MINIMOS 5.1 [10]. In this simulation method the series resistance is extracted from the dissipated heat in the source or drain region of the MOSFET. The third section explains the theory behind the new measurement technique, both for the measurement of the drain series resistance as a function of the drain bias as for the measurement of the total series resistance at low drain bias as a function of gate bias only using one single device. In the fourth section, measurement results for submicron MOSFET's are given and compared to simulations and other measurement techniques. The last section deals with the compact modeling of the series resistance as a function of terminal bias.

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II. Simulation and Analysis of the Source and Drain Series Resistance

In this section a simulation method will be presented to calculate the value of the drain or source series resistance as a function of the terminal voltages. The final goal of this section is to give the reader some understanding about the influence of series resistance on the MOSFET's characteristics and the importance of correct series resistance measurement.

The series resistance is calculated from the dissipated heat in the drain or source junction of the MOSFET. The total dissipated heat in the MOSFET with drain current I_{drain} under neglect of the bulk and gate current equals

$$P_h = I_{\text{drain}} * V_{\text{ds}} = I_{\text{drain}}^2 * (R_s + R_{\text{ch}} + R_d). \quad (1)$$

Under isothermal and static conditions, the local heat dissipation (H) in a semiconductor without electromagnetic radiation can be written as [11]

$$H = H_{\text{joule}} + H_{\text{thomson}} + H_{\text{rec}}$$

where

$$\begin{aligned} H_{\text{joule}} &= \rho_n \vec{J}_n \cdot \vec{J}_n + \rho_p \vec{J}_p \cdot \vec{J}_p \quad (2)\\ H_{\text{thomson}} &= -qT(\nabla P_n \cdot \vec{J}_n + \nabla P_p \cdot \vec{J}_p)\\ H_{\text{rec}} &= qR[-\phi_n + \phi_p + T(P_n + P_p)]. \end{aligned}$$

The first term represents the Joule heat. The Joule heat always contributes a positive term to the total heat generation.

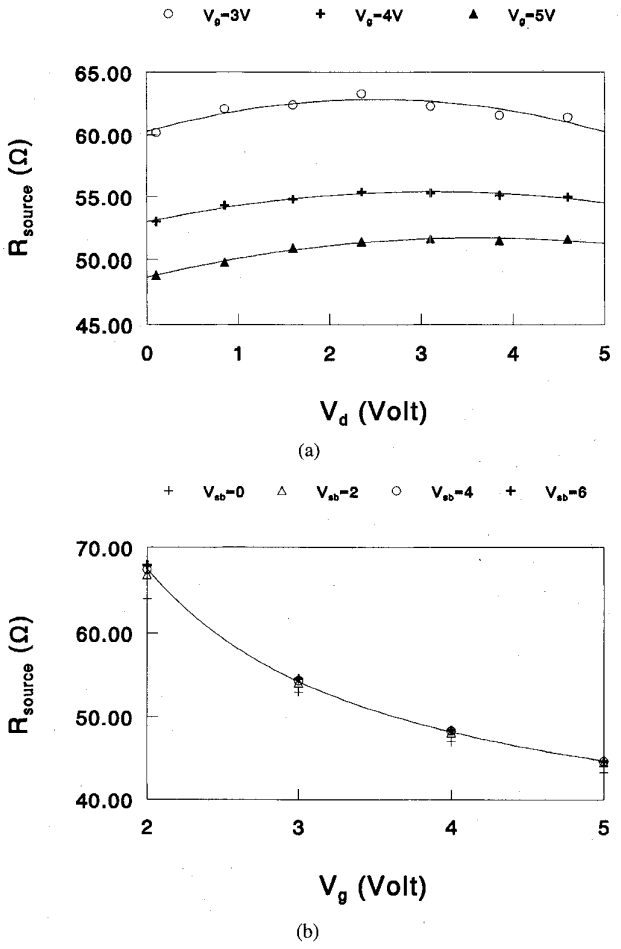

Fig. 1. (a) Source series resistance as a function of drain bias at different values of gate bias. (b) Source series resistance as a function of gate bias at several values of bulk bias ($L_{\text{eff}} = 0.25$ μm, $W_m = 10$ μm).

The second term represents the Thomson heat and the Peltier effect. The last term represents the recombination heat.

According to Wolbert [12] the largest heat generation term in a SOI device in the stationary case is the Joule heat. The recombination heat generation occurs only close to the drain in case of some avalanche. The recombination heat generation is about four orders of magnitude smaller than the Joule heat generation. This is of course also true for an LDD MOSFET. The Thomson heat only occurs at regions with large gradients in the thermo-electric powers $P_{n,p}$. This is near the source and drain where large gradients in carrier concentration result in large gradients in $P_{n,p}$. Generally the Thomson heat is about one to two orders less than the Joule heat generation. Since temperature gradients are not taken into account, (2) can be simplified giving

$$H = \rho_n \vec{J}_n \cdot \vec{J}_n + \rho_p \vec{J}_p \cdot \vec{J}_p + qR(\phi_p - \phi_n). \tag{3}$$

Calculating the dissipated heat in the appropriate sections of the device, the source, drain or channel resistance can be calculated. Integration of (3) over the source and drain area yields the source and drain series resistance

$$R_s = \frac{\int H_{\text{source}} \partial^3 r}{I^2_{\text{drain}}}$$

$$R_d = \frac{\int H_{\text{drain}} \partial^3 r}{I^2_{\text{drain}}}. \tag{4}$$

In Fig. 1(a) and (b), some plots of the series resistance are shown at several bias conditions. In this case the source and drain series resistance was calculated using (4). From Fig. 1(a) we deduce that R_s is nearly drain voltage independent, even for LDD MOSFET's with effective channel lengths down to 0.25 μm. Furthermore the source and drain series resistance is nearly independent of bulk bias as shown in Fig. 1(b). The latter observation is in agreement with others [13], [14]. In their measurement methods L_{eff} is found by measuring the response of the device resistance to V_{sb}, while the gate bias is fixed. By changing the bulk bias, the threshold voltage is changed. However this change in the value of the threshold voltage depends on the value of the effective channel length and is not the same for each MOSFET introducing errors in the extraction of the effective channel length and series resistance.

Utilizing the dissipation method to extract the series resistance one can argue about the definition of effective channel length of the MOSFET: Which part of the drain junction belongs to the channel and what part belongs to R_d. Normally one assumes that at low drain voltages ($V_d \leq 0.10$ V) the electrical conductivity of the transition regions of the device (between source/channel and drain/channel) is almost uniformly modulated by the gate voltage. The result is that the real channel length will be slightly larger than the metallurgical channel length. In literature [5] the following criterion for L_{eff} is used at low drain voltage. To this purpose, the mobile carrier concentration, integrated orthogonally to the Si-SiO_2 interface (in the middle of the channel) is compared with the integrated mobile carrier concentration in the drain, respectively the source. The channel is now assumed to terminate at the point where the integrals are equal. Using the above definition one also assumes that each mobile carrier gives the same contribution to the conduction, which is of course not true. The criterion of course must be that the channel resistance per unit length must equal the resistance per unit length in that part of the source and drain which are added to the effective channel length.

In Fig. 2 a plot is shown of the integrated dissipated heat (integrated from the Si-SiO_2 interface toward the substrate) in a LDD MOSFET as a function of the lateral coordinate. This integrated dissipated heat is proportional to the resistance per unit length. At low drain voltage, the dissipated heat per unit length reaches its maximum value in the middle of the channel. Increasing the drain bias, the maximum value of the dissipated heat per unit length moves toward the drain. Since even at low drain voltage the dissipated heat and thus also the conduction in the channel is not homogeneously distributed it becomes clear that the definition used in [5] is of little practical use.

To avoid problems with the definition of the effective channel length during the simulations it is better to use the metallurgical channel length as the effective channel length. In that case it is also very simple to define the source and drain series resistance. The source and drain series resistance simply equals the ratio of the dissipated heat in the source and drain junction and the square of the drain current, as defined by (4).

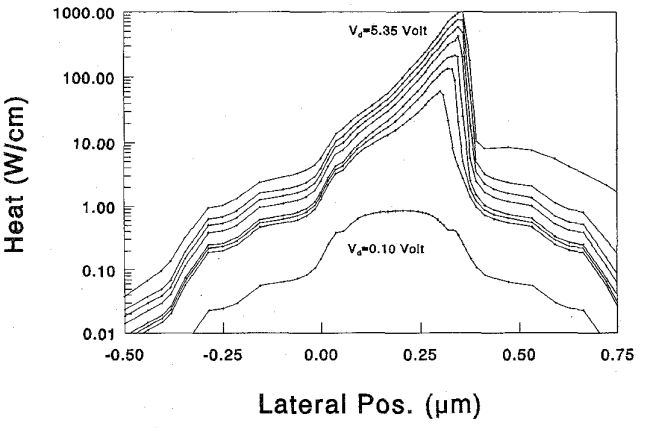

Fig. 2. Integrated dissipated heat per unit length as a function of lateral coordinate. The heat is integrated perpendicular to the oxide-semiconductor interface. The metallurgical channel boundary is located at $X = 0.06$ μm and $X = 0.31$ μm. The drain voltage step is 0.75 V. ($V_g = 5$ V, $L_{\text{eff}} = 0.25$ μm, $W_m = 10$ μm).

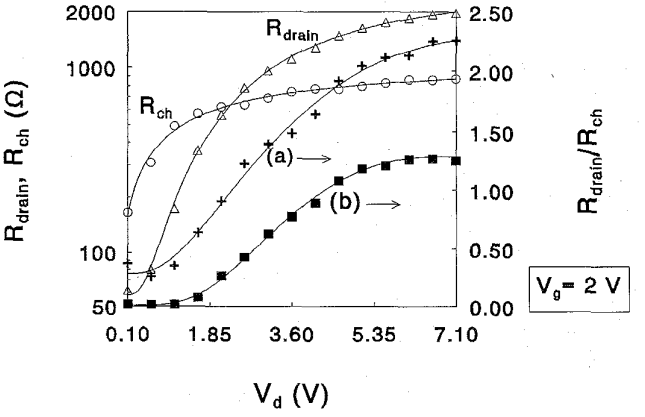

Fig. 3. Drain series resistance, channel resistance and their ratio (curve a) for a N-channel LDD MOSFET as a function of the drain bias ($L_{\text{eff}} = 0.25$ μm, $W_{\text{eff}} = 10$ μm, $V_g = 2$ V). For comparison also the ratio of R_{drain} and R_{ch} is given for a MOSFET with a mask channel length of 5.0 μm (curve b).

Another important issue is that the drain series resistance increases with drain voltage even in the ohmic region of the MOSFET. As shown in Fig. 3 the ratio of the drain series resistance and the channel resistance increases with drain bias quite dramatically. As long as the MOSFET is in its ohmic region the drain series resistance increases due to velocity saturation. At the onset of saturation (saturation voltage $V_d \approx 1.5$ V) the drain series resistance already equals the channel resistance for this type of MOSFET. For comparison also the ratio (b) for a MOSFET with a mask channel length of 5.0 μm is given. Even in this case the drain series resistance easily exceeds the channel resistance in saturation. The conclusion is that the drain series resistance increases considerably with drain bias. Therefore it is important that we can measure R_d as a function of drain bias. In the next section we pay attention to the measurement theory behind our novel measurement technique used to measure among others $R_d(V_d)$.

III. A Novel Method to Measure R_d and R_s

As seen in the previous section one of the difficulties of determining the value of the series resistance at different bias conditions is the consistent definition of the intrinsic device. Thus a physical quantity to define the intrinsic device is needed. However our new measurement technique avoids the direct definition of the intrinsic device: i.e., the series resistance R_d and R_s is not extracted using an analytical model to describe the intrinsic device. Nevertheless a physical quantity is still needed to define the intrinsic device in a consistent way. For this purpose the influence of series resistance on the small signal behavior of the MOSFET will be used. In Appendix A the influence of series resistance on the small signal behavior for a arbitrary N-terminal device is given. In this section the results of Appendix A are applied to a MOSFET.

The commonly used equations [14] to relate the intrinsic transconductance G_{mi} and conductance G_{di} to the measured transconductance G_m and conductance G_d (taking the source as reference) are

$$G_{mi} = \frac{G_m}{1 - G_m * R_s - G_d * (R_s + R_d)}$$

$$G_{di} = \frac{G_d}{1 - G_m * R_s - G_d * (R_s + R_d)}. \tag{5}$$

However, the above equations are not generally valid. The voltage drop in R_s and R_d in addition to the gate-source and drain-source voltages modulates the substrate-source voltage. This effect can be very important for MOSFET's and has to be included. Also in the case of gate and drain voltage dependent series resistances, the derivative of the series resistances with respect to the gate, respectively the drain bias, has to be included too in the above equations. Deriving new equations to express G_{mi} and G_{di} in terms of R_s, R_d, G_m and G_d the following assumptions are used:

- The gate and substrate current are neglected and therefore the current I_{drain} through R_s, R_d and the MOSFET channel is the same.
- R_s and R_d are both gate voltage dependent and R_d is also drain bias dependent.

Taking the source as reference, the following conductances can be defined

$$G_m = \frac{\partial I_{\text{drain}}}{\partial V_g}$$
$$G_d = \frac{\partial I_{\text{drain}}}{\partial V_d} \tag{6}$$
$$G_b = \frac{\partial I_{\text{drain}}}{\partial V_b}$$

where G_b is the substrate transconductance (control of V_b on I_{drain}). The relationship between the intrinsic and extrinsic terminal voltages of the MOSFET is shown in Fig. 4 and is given by

$$V_g' = V_g - I_{\text{drain}} * R_s$$
$$V_d' = V_d - I_{\text{drain}} * (R_s + R_d) \tag{7}$$
$$V_b' = V_b - I_{\text{drain}} * R_s.$$

An incremental change of the current $\tilde{I}_{\text{drain}}$ can now be expressed in terms of the intrinsic conductances and an incremental change in the terminal voltages $(\tilde{V}_g, \tilde{V}_d, \tilde{V}_b)$

$$\tilde{I}_{\text{drain}} = G_{mi} * \tilde{V}_g + G_{di} * \tilde{V}_d + G_{bi} * \tilde{V}_b \tag{8}$$

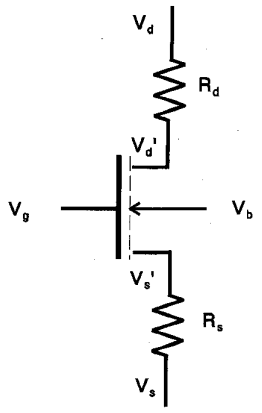

Fig. 4. Definition of the intrinsic and extrinsic MOSFET terminal biases and series resistance.

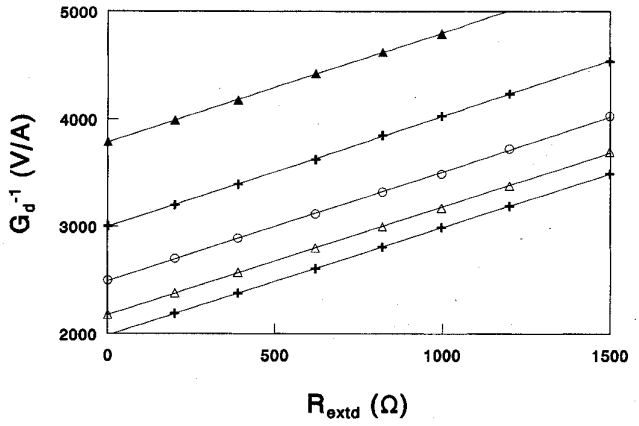

Fig. 5. Slope of G_d^{-1} versus externally added series resistance $R_{\rm extd}$ at different values of drain bias ($V_g = 5$ V, $V_d = 0.10$ (lower curve), 0.35, 0.60, 0.85, 1.10 (upper curve) V).

Combining (7) and (8) the following expressions for G_d, G_m, and G_b are derived

$$G_m = \frac{G_{mi} - (G_{bi} + G_{mi}) * I_{\rm drain} * \frac{\partial R_s}{\partial V_g} - G_{di} * I_{\rm drain} \frac{\partial (R_s + R_d)}{\partial V_g}}{1 + G_{di} * (R_s + R_d) + (G_{mi} + G_{bi}) * R_s} \tag{9}$$

$$G_b = \frac{G_{bi} - (G_{mi} + G_{bi}) * I_{\rm drain} \frac{\partial R_s}{\partial V_b} - G_{di} * I_{\rm drain} \frac{\partial (R_s + R_d)}{\partial V_b}}{1 + G_{di} * (R_s + R_d) + (G_{mi} + G_{bi}) * R_s} \tag{10}$$

$$G_d = \frac{G_{di} * \left(1 - I_{\rm drain} \frac{\partial R_d}{\partial V_d}\right)}{1 + G_{di} * (R_s + R_d) + (G_{mi} + G_{bi}) * R_s}. \tag{11}$$

It is easily seen that the above equations are a generalization of (5). According to (11) it is possible to determine $\partial R_d / \partial V_d$ and the quotient of G_{di} and $(G_{mi} + G_{bi})$ using a simple measurement technique. The whole measurement principle is based on the measurement of a conductance as a function of an externally added series resistance at the drain or source terminal as explained below.

Suppose we add an external resistance $R_{\rm extd}$ at the drain terminal. Equation (11) can now be written as

$$G_d^{-1} = \frac{1 + G_{di} * (R_s + R_d + R_{\rm extd}) + (G_{mi} + G_{bi}) * R_s}{G_{di} * \left(1 - I_{\rm drain} \frac{\partial R_d}{\partial V_d}\right)}. \tag{12}$$

However to keep the internal bias conditions (thus also the current $I_{\rm drain}$) and the intrinsic conductances unchanged when an external drain series resistance is added, the external drain bias has to be adapted. Then it becomes clear that a plot of G_d^{-1} versus the externally added series resistance $R_{\rm ext1}$ yields a straight line with its slope equal to

$$\frac{\partial G_d^{-1}}{\partial R_{\rm extd}} = \frac{1}{\left(1 - I_{\rm drain} \frac{\partial R_d}{\partial V_d}\right)}. \tag{13}$$

In Fig. 5 the measured reciprocal value of G_d is plotted as a function of an externally added drain series resistance at a fixed gate bias and at different values of drain bias. From (13) the value of $\partial R_d / \partial V_d$ can easily be obtained. The same principle can be used to obtain the quotient of G_{di} and $(G_{mi} + G_{bi})$. Now the external series resistance $R_{\rm exts}$ has to be added to the source terminal. The slope of the plot of G_d versus R_d then equals

$$\frac{\partial G_d^{-1}}{\partial R_{\rm exts}} = \frac{G_{mi} + G_{bi} + G_{di}}{G_{di}\left(1 - I_{\rm drain} \frac{\partial R_d}{\partial V_d}\right)}. \tag{14}$$

The same method of adding external series resistance at the source and/or drain terminals can be used to determine $\partial R_s / \partial V_g, G_{mi}/G_{di}$ and G_{bi}/G_{mi}. The expression for $\partial R_s / \partial V_g$ is for instance (see Appendix B)

$$\frac{\partial R_s}{\partial V_g} = \left(\frac{G_{mi}}{G_{di}} - \frac{G_m}{G_d}[1 - I \partial R_d / \partial V_d]\right) \frac{I_{\rm drain}^{-1}}{2 + \frac{G_{mi} + G_{bi}}{G_{di}}}. \tag{15}$$

In Appendix B it is shown how to obtain the series resistance as a function of gate bias at low drain bias from the above expression. Since the derivative of R_s with respect to gate bias can be measured we can discriminate between the intrinsic and the extrinsic MOSFET. In this way we are able to determine $R_s(V_g)$ from one single MOSFET.

First we focus our attention on the determination of $R_d(V_g, V_d)$. The value of $R_d(V_g, V_d)$ is solved by calculating the integral at constant gate bias

$$R_d(V_d, V_g = V_{g1}) = R_d(0, V_g = V_{g1}) + \int_0^{V_d} \left(\frac{\partial R_d}{\partial V_d}\right) dV_d'. \tag{16}$$

To solve this integral we have to determine the value of the drain series resistance at $V_d = 0$ V. Using the fact that at low drain bias ($V_d \leq 50$ mV) the value of the drain series resistance equals the value of the source series resistance (for symmetrical devices), the value of R_d at low drain bias can be estimated by using a well known measurement method such as described in [5], [8] or using the new method described in Appendix B. The value of R_d at a certain gate voltage now equals half the value of the total series resistance.

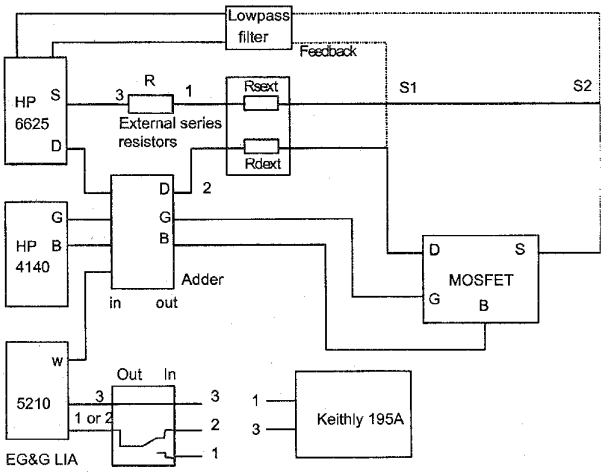

Fig. 6. Basic measurement setup for conductance measurement. As can be seen, the source is used as reference.

This method is of course not restricted to MOSFET's only. The method of taking the derivative of the series resistance with respect to the terminal voltages into account in the 'conductance equations', can be applied to all kind of semiconductor devices giving at least a better understanding of the intrinsic behavior of the device.

IV. Measurement Results

In this section the above measurement method is applied to simulated and measured data of a sub micrometer N-channel MOSFET. For our measurement we used LDD N-channel MOSFET's with a gate oxide thickness of 15 nm. The devices were supplied by Philips Research Laboratories, Eindhoven. The channel and doping profile for the simulation have been generated with Suprem IV [16]. For the device simulation the 2-D device simulator Curry [17] using the same mobility model as MINIMOS [10] was used. The conductances were measured using a Princeton Applied Research model 5204 Lock-In amplifier. The terminal voltages were supplied using a HP4140B pA/dc voltage source and a HP6625A System power supply. Via the sense of this latter power supply the dc voltage at the drain was kept constant, independent of the value of the external added series resistance R_{extd} or R_{exts}. The whole setup was controlled by a computer via the IEEE-bus; an overview is shown in Fig. 6. During the measurements we add up to eight values of the external series resistors to the drain and the source.

A. The Gate Bias Dependent Series Resistance

A goal of the measurement technique described in this paper is to determine the series resistance from single transistor measurements. The first step is to measure the derivative of the series resistance as a function of the gate bias according to (15). In Fig. 7 the result is shown. From this plot we determine the gate voltage dependent part of the series resistance. A good semi-empirical model for this series resistance as a function of gate bias at low drain bias, as derived in the next section,

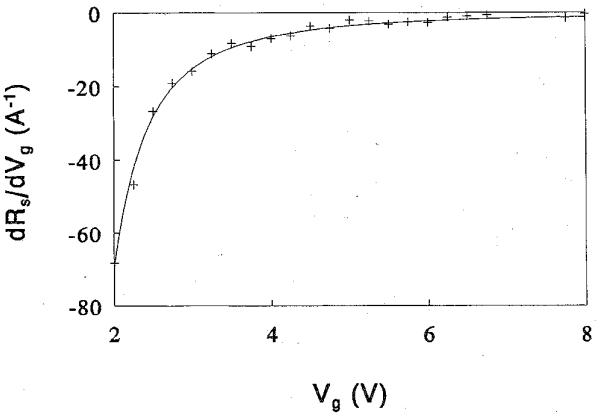

Fig. 7. The measured derivative of the source series resistance as a function of gate bias at $V_d = 0.10$ V. ($W_m = 10\mu$m, $L_m = 0.80$ μm). The solid line has been calculated according to our model.

TABLE I
Coefficients of Empirical Models to Fit the Measured Mobility and Series Resistance. The Column 'Single' Refers to Parameters Obtained Using One Single Mosfet, the Column 'Set' Refers to Parameters Obtained Using a Set of Transistors. The Parameters θ_a and θ_d Are the Mobility Reduction Parameters of the Transversal Electric Field as Defined in Appendix B

Model parameters	Single	Set
β	$2.21 * 10^{-3}$ A/V^2	$2.23 * 10^{-3}$ A/V^2
θ_a	0.45 V^{-1}	0.43 V^{-1}
θ_d	0.0095 V^{-2}	0.0107 V^{-2}
a_0	45.30 Ω	108 Ω
a_1	1740 Ω/V	53.6 Ω/V
a_2	15.0 V	-0.1 V

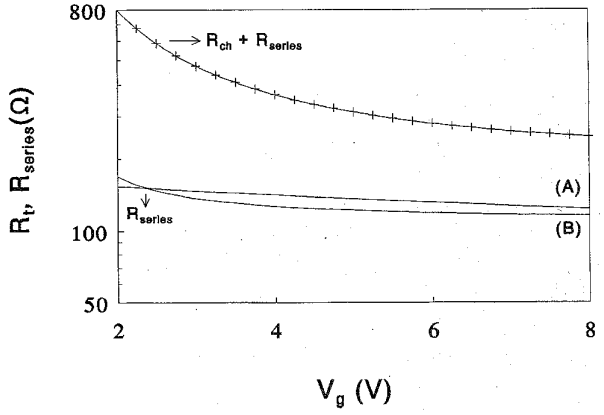

Fig. 8. The measured MOSFET total resistance and series resistance as a function of gate bias at $V_d = 0.10$ V ($W_m = 10$ μm, $L_m = 0.80$ μm). The series resistance curve (A) is the determined series resistance using a set of identical MOSFET's, curve (B) is derived from the single transistor measurement technique.

equals

$$R_{\text{series}} = a_0 + \frac{a_1}{a_2 + V_g - V_{\text{th}}}. \tag{17}$$

Therefore the derivative of R_{series} with respect to gate bias equals

$$\frac{\partial R_{\text{series}}}{\partial V_g} = \frac{-a_1}{(a_2 + V_g - V_{\text{th}})^2}. \tag{18}$$

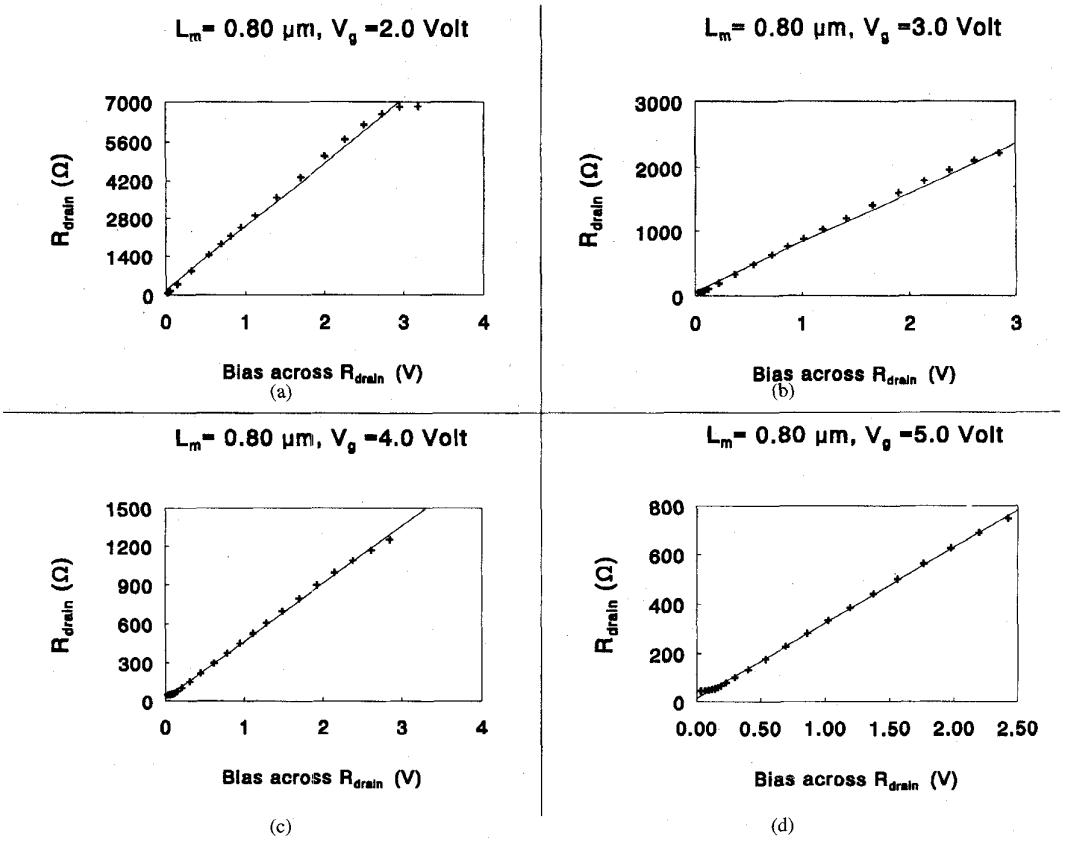

Fig. 9. (a) Drain current as a function of drain bias. (b)–(d) The derivative of the drain series resistance with respect to the drain bias and increase of R_d as a function of the drain bias. The value of gate bias is 4, 5 and 6 V, respectively ($W_m = 2$ μm, $L_m = 0.70$ μm).

The two coefficients (a_1, a_2) represent the gate voltage dependent part of the series resistance and can be determined from a plot like shown in Fig. 7. After a_1 and a_2 have been determined, the intrinsic MOSFET parameters can be determined independently from the series resistance using the method described in Appendix B. Finally the value of a_0 is found by subtracting the channel resistance and the gate bias dependent series resistance part from MOSFET total resistance. The final result is shown in Table I. In this table the determined compact model parameters are compared with the compact model parameters determined from a set of identical MOSFET's with different channel lengths. Though the coefficients for the series resistance model differ a lot, the actual series resistance, as shown in Fig. 8, is almost the same. The average difference is about 10%. The advantage using this single transistor measurement technique is that no longer the difference in threshold voltage between the MOSFET's with different channel length can affect the obtained series resistance value. Also gate corner effects introducing different average channel mobility in an L-array of MOSFET's, can no longer introduce errors in the determination of R_{series}.

B. The Drain Bias Dependent Series Resistance

Next we are going to focus on the behavior of the drain series resistance as a function of drain and gate bias. In this case we used an LDD N-channel MOSFET with a gate mask length of 0.7 μm and a mask channel width of 2.0 μm. In Fig. 9(a) a the drain current is given as a function of the drain bias for different gate bias. In this case the saturation voltage lies between 1.60 and 2.50 V, dependent on the gate bias.

Fig. 9(b)–(d) give the derivative and the increase of the drain series resistance as a function of drain bias at different gate bias. As expected the drain series resistance increases monotonously as a function of the drain bias. Furthermore the increase of the drain series resistance is the largest at the smallest gate bias. For all gate voltages, the simulated increase in the drain series resistance as shown in Fig. 10 is larger than the measured one as shown in Fig. 9. This can be understood as follows. First there can be a substantial difference between the simulated doping profile and the doping profile of the real devices. Also in our simulations we simply assume that the whole drain junction is part of the drain series resistance. However, in our novel measurement technique, the difference between series resistance and intrinsic channel resistance is inherent to our method. So during our measurements distinction between the intrinsic MOSFET and series resistance on a more physical base is used.

Similar results have been obtained for MOSFET's with different channel length. In general an accurate measurement of R_d versus V_d is only possible for MOSFETS with a rather short channel length ($L_m \leq 1$ μm) and when the MOSFET is below saturation. A short channel length is needed owing to the fact that in these devices the conductance is rather large and the ratio of R_d and R_{ch} is large.

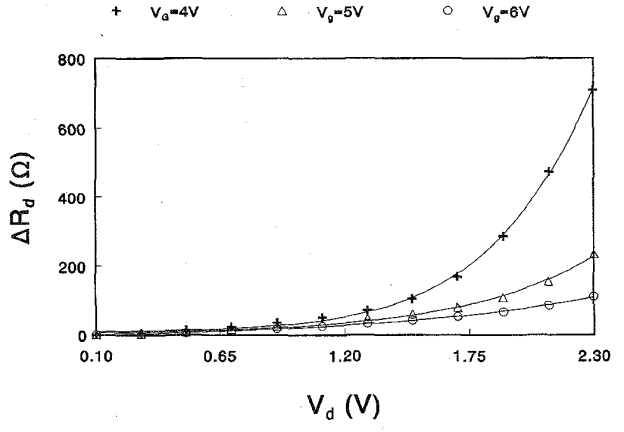

Fig. 10. Simulated increase in the drain series resistance as a function of drain bias at different values of gate bias ($W_m = 10\ \mu$m, $L_m = 0.70\ \mu$m).

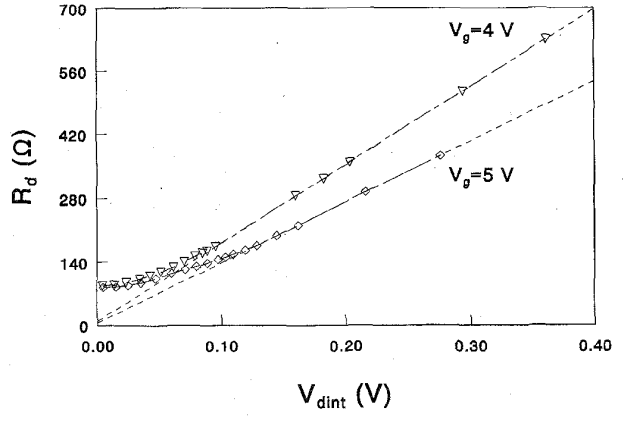

Fig. 11. Measured drain series resistance at different gate bias as a function of the drain bias across this series resistance V_{dint}($W_m = 2\ \mu$m, $L_m = 0.70\ \mu$m).

Despite problems with the measurement accuracy when the MOSFET is working in saturation, we tried to measure $\partial R_d/\partial V_d$ in the above region. First the measurement accuracy was increased by increasing the value of the external series resistance considerably ($R_{extd} = 200 * i\,\Omega$, $i = 1..8$). In addition the ac voltage applied to the drain terminal was increased from 20 to 100 mV. To avoid effects of higher harmonics, a bandpass filter centered around the frequency of the ac voltage is used. In this case the measurements were repeated 60 times for each bias point. From these 60 measurements per bias point, the average value is obtained. The result is shown in Fig. 11 where we plotted the value of R_d versus the voltage across this resistance V_{dint}. Now we see that the drain series resistance increases nearly linearly with bias V_{dint} for $V_{dint} \geq 0.10$ V. Obviously the drain series resistance increases due to velocity saturation. More attention to this behavior is given in the next section, where this characteristic is used to model R_{drain} in a very effective way.

V. Modeling

In this section attention is paid to the modeling of the series resistance as a function of the gate and drain bias in both the ohmic and saturation region. First attention is paid to the source and drain series resistance at low drain bias as a function of gate bias. Finally attention is paid to the drain series resistance.

A. Modeling of the Gate Bias Dependent Series Resistance

In [18] it was found that the value of the source and drain series resistance is mainly determined by the current flow near the oxide-semiconductor interface. Calling this spreading resistance therefore seems questionable. Instead we split the accumulation resistance into two parts. The part of the accumulation resistance beneath the thin gate oxide will be called R_{ac1}, the low-doped part beneath the offset spacer R_{ac2}. Now suppose that the gate thickness equals h, as shown in Fig. 12. According to [21] the capacitance C_{ac2} of this configuration approximately equals

$$C_{ac2} = \frac{2\epsilon_{ox}W}{\Pi} \ln\left(\frac{h}{t_{ox}}\right). \tag{19}$$

Here we assumed that the length of the offset spacer x_{ac2} is approximately equal to the gate thickness h. The value of accumulation resistance beneath the offset spacer therefore equals

$$R_{ac2} = \frac{\Pi h^2}{2\mu_{ac}\epsilon_{ox}W \ln\left(\frac{h}{t_{ox}}\right)(V_g - V_{th})}. \tag{20}$$

In (20) only t_{ox} and the accumulation mobility μ_{ac} are a function of the distance to the gate edge. Because of the increase of the doping concentration toward the source and drain contact, the accumulation mobility will decrease with increasing distance to the gate edge. No exact data is however known for this accumulation mobility as a function of the doping concentration and therefore this effect could not be taken into account. Therefore (20) is only a first approximation of the series resistance beneath the offset spacer. Besides the two gate bias dependent accumulation resistances R_{ac1} and R_{ac2}, there also exists a resistance R_{par} in parallel with these accumulation resistances due to a current conduction deeper in the junctions. Assuming that this resistance is nearly gate voltage independent, the gate voltage part of the source and drain series resistance equals

$$R_{part}(V_g) = \frac{R_{par}R_{ac}}{R_{par} + R_{ac}} = \frac{R_{par}K_{ac0}}{K_{ac0} + R_{par}(V_g - V_{th})}. \tag{21}$$

In the above equation the sum of the accumulation resistances were assumed to equal

$$R_{ac1} + R_{ac2} = \frac{K_{ac0}}{V_g - V_{th}}. \tag{22}$$

In the latter equation K_{ac0} represents a technology dependent parameter. The final result is a good physics based model expression for the series resistance as a function of gate bias (at small drain to source bias). Therefore according to (21) the sum of R_{source} and R_{drain} equals

$$\begin{aligned} R_{series} &= R_{source} + R_{drain} \\ &= a_0 + \frac{a_1}{a_2 + (V_g - V_{th})}. \end{aligned} \tag{23}$$

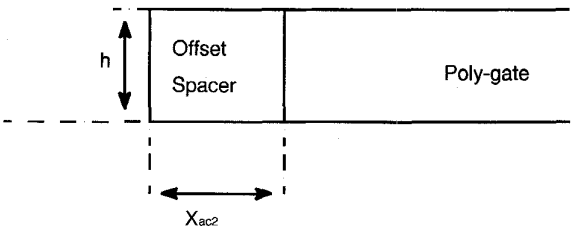

Fig. 12. Calculation of the effective oxide thickness beneath the offset spacer in a conventional LDD MOSFET.

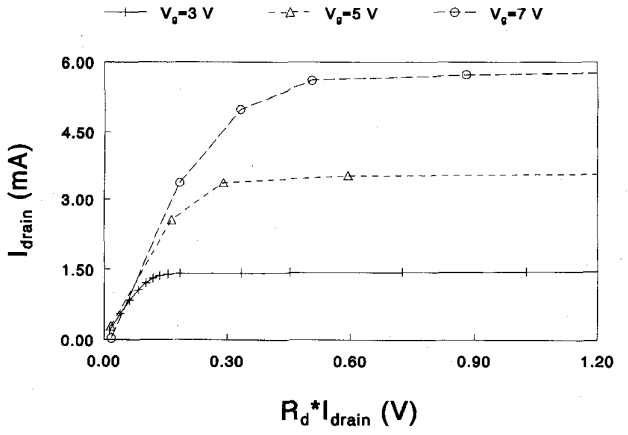

Fig. 13. Drain current versus voltage across drain series resistance at different gate voltages ($W = 10$ μm, $L_m = 0.80$ μm, $t_{ox} = 125$ Å).

with V_{th} being the threshold voltage at low drain bias, $a_1 = 2K_{ac0}$ and $a_2 = K_{ac0}/R_{par}$. In the above the contact and sheet resistance is represented by a_0, and the accumulation resistance and parallel resistance by the second righthand term. In the previous section it was already shown that the above equation perfectly fits the measured data. Therefore for use in a compact circuit-level model the result given by (23) is very useful.

B. Modeling of the Drain Bias Dependent Drain Series Resistance

In Fig. 13 the voltage characteristics of the drain series resistance is plotted. From this figure it looks possible to model the current-voltage characteristics as a FET. However the disadvantage of this approach is the number of parameters involved for correct modeling of the characteristics. Furthermore these model parameters must be known before the model parameters of the intrinsic MOSFET can be estimated. To reduce the number of parameters and measurements to be performed, another approach has to be used, presented below.

Simulations have shown [18] that the main current path in the MOSFET is located near the oxide/semiconductor interface. It was found that 80% of the dissipated heat is located within 0.04 μm from this interface. Therefore, the relevant doping profile of the source/drain junction can be considered as one-dimensional. Further we assume that the increase in the drain series resistance is completely due to velocity saturation caused by an increase in the lateral electric field. The decrease of the lateral mobility due to velocity saturation can be modeled as [19]

$$\mu = \frac{\mu_0}{\left[1 + \left(\frac{\mu_0 E_x}{v_s}\right)^{\beta}\right]^{1/\beta}} \tag{24}$$

with v_s being the saturated velocity and $\beta = 2$ for electrons and $\beta = 1$ for holes. Several authors [19], [20] have shown that taking $\beta = 1$ results in good modeling results, even for N-doped regions. Further assuming that the tail of the LDD junction can be approximated by a linear doping profile [18], the value of the drain series resistance in case of a N-channel MOSFET equals

$$\begin{aligned} R_{ldd} &= \int_0^{x_{ldd}} \frac{\rho}{A}dx \\ &= \int_0^{x_{ldd}} \frac{1 + \theta_{c1}V_{d1}}{Aq\mu_0(N_d + kx)}dx \\ &= \frac{1 + \theta_{c1}V_{d1}}{Aq\mu_0 k} \ln\left(\frac{N_{d0} + k * x_{ldd}}{N_d}\right) \end{aligned} \tag{25}$$

where x_{ldd} is the length of the LDD region, V_{d1} the potential across the LDD region, N_{d0} the doping concentration at the beginning of the LDD profile (near the channel) and θ_{c1} equals

$$\theta_{c1} = \frac{\mu_0}{v_s x_{ldd}}. \tag{26}$$

Further we assume that the lateral electric field is nearly constant in the LDD region and thus can be approximated by V_{d1}/x_{ldd}. From (25) we now can derive that the drain series resistance increases linearly with the bias across the drain. So at constant gate bias for the drain series resistance as a function of drain bias we can write

$$R_{drain}(V_{d1}) = R_{d0} + \alpha V_{d1} \tag{27}$$

where α is a function of $(N_{d0}, k, v_s, x_{ldd}, \mu_0)$. The above result was tested using device simulations for both N- and P-channel devices. Using the dissipation method the drain series resistance was calculated as a function of the bias drop across this resistance. As shown in Fig. 14 the above derivation is indeed in accordance with the simulations. Only at high gate bias and at low bias across $R_{drain}(V_{d1})$ some deviations are noticeable.

From Fig. 14 we see that α decreases with increasing gate voltage. This is due to the fact that with increasing gate bias, the accumulation in the LDD region increases and therefore the resistance decreases. Increasing the bias V_{d1} across the drain series resistance, the value of the lateral electric field will increase less rapidly than would be the case at lower gate voltage. At this lower electric field the value of the drain series resistance will be lower too. Device simulations show that a good fit of α as a function of gate bias is given by the following empirical equation

$$\alpha(V_g) = \frac{C_0}{(C_1 + (V_g - V_{th}))} \tag{28}$$

where C_0 and C_1 are modeling parameters and V_{th} is the low drain bias threshold voltage. The correctness of the above description of drain series resistance was checked using a wide range of LDD doping profiles, both for N- and P-channel

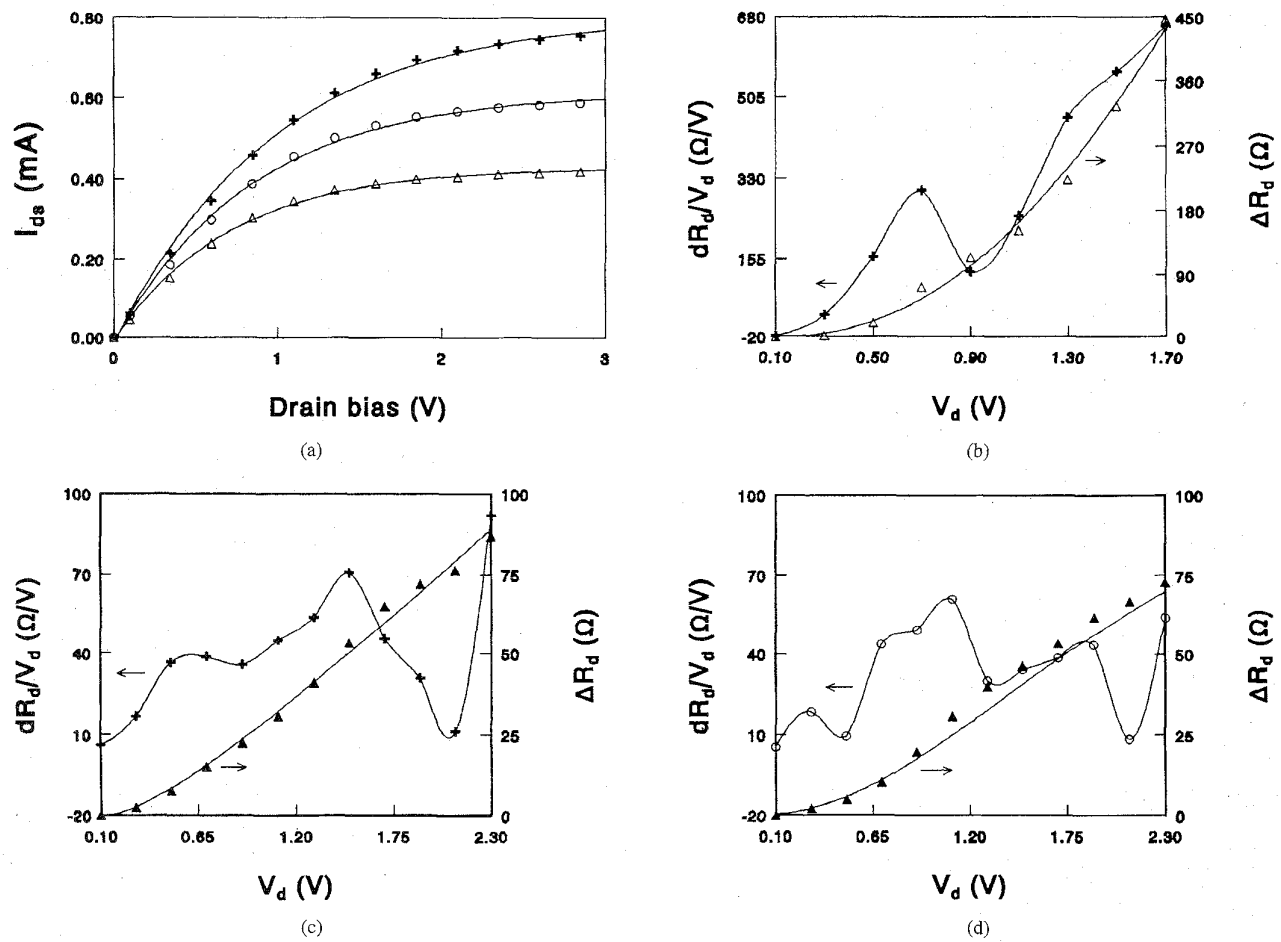

Fig. 14. Drain series resistance as a function of the bias across the resistance for several values of the gate bias. ($L_m = 0.80$ μm, $W_m = 10$ μm).

devices and confirmed. For a symmetrical device, the value of the drain series resistance at low drain bias equals the source series resistance. The semi-empirical model for the drain series resistance now equals

$$R_{\text{drain}}(V_g, V_d) = R_{\text{source}}(V_g) + \frac{C_0}{C_1 + (V_g - V_{\text{th}})} V_{d1}. \quad (29)$$

This equation is of course only valid in the ohmic and saturation region. In the subthreshold region the drain series resistance must equal the value of the source series resistance, independent of the drain bias.

VI. Conclusion

A measurement method has been presented to measure the bias dependent series resistance using only one single MOSFET. Though already a single transistor measurement method exists [6] to measure R_{series} as a function of gate bias at low drain bias, this method gives rather poor results. In addition until now it was not possible to measure the drain series resistance as a function of the drain bias using one single MOSFET. Though for this purpose already a measurement method exists [7], that method is based on wrong assumptions.

The great advantage of our method is the fact that for the measurement of the ratio of the intrinsic conductances no compact model description is needed. Only a relation between G_{mi} and G_{bi} had to be derived. The measurement principle is based on the discrimination between the intrinsic and extrinsic behavior of the MOSFET. By adding external source and drain series resistance and using a clever measurement principle several auxiliary quantities can be measured. The result is that both the drain and gate bias dependency of the series resistance can be measured. However in practice the method is limited to moderate values of drain bias.

Results have been presented for N-channel MOSFET's with an effective channel lengths down to 0.45 μm, giving good results. Experiments have shown that the accuracy of the method for the measurement of $R_{\text{series}}(V_g)$ at low drain bias is comparable to measurement methods using an identical set of MOSFET's. The measurement accuracy at higher drain bias (MOSFET is still working in the ohmic region) is limited due to degradation effects occurring during the measurements and the resolution of the measurement equipment. Though extremely time consuming we have been able to measure R_d in the saturation region. It was found that the drain series resistance increases linearly with the bias across this resistance.

As far as the measurement of R_d as a function of drain bias is concerned, we have to notice that in general our measurements give a value comparable to simulated values. However there are practical problems in comparing the measurements with simulated values. First the simulated doping profiles can

differ from the realized ones. Next the non correct calculation of the accumulation mobility during the device simulations can introduce an error. In our simulations we also explicitly define the intrinsic MOSFET by assuming that the drain series resistance extends across the whole drain junction. Our measurement technique, however, discriminates between the intrinsic and extrinsic device without any model assumptions about the intrinsic device. Therefore quantitative comparison of simulations and measurements is not easy.

APPENDIX A

Consider a device with N terminals (Fig. 15). At each terminal there is a voltage dependent series resistance (R_i), which can be a function of the N terminal voltages (V_i). An incremental change in the terminal current I_i can now be expressed in an incremental change of the extrinsic terminal voltage V_i

$$\partial I_i = \sum_1^N a_{ij} \partial V_j' \tag{30}$$

with the terms $a_{i,j}$ and V_j' being equal to

$$\begin{aligned} a_{ij} &= \frac{\partial I_i}{\partial V_j'} \\ \partial V_j' &= \partial V_j - R_j \partial I_j - I_j \partial R_j. \end{aligned} \tag{31}$$

Rewriting the above equation in a matrix form, the quantity $\partial I_i / \partial V_j$ can be solved

$$[X] = [I + B]^{-1}[A - C * Y]. \tag{32}$$

Here, the quantities B, A, C and Y are defined as

$$\begin{aligned} X_{ij} &= \frac{\partial I_i}{\partial V_j} \\ Y_{ij} &= \frac{\partial R_i}{\partial V_j} \\ B_{ij} &= a_{ij} * R_j \\ C_{ij} &= a_{ij} * I_j. \end{aligned} \tag{33}$$

In some cases by adding external series resistances, it is possible to determine $Y_{i,j}$ as a function of the terminal voltages. In the special case of a MOSFET it is even possible to measure the change in the drain series resistance R_d as a function of the drain and gate bias. Also it is possible to determine $R_s(V_g)$ and $R_d(V_g, V_d)$ using one single MOSFET.

APPENDIX B
MEASURING $\partial R_s / \partial V_g$

In (15) the only unknown parameter that we can not measure directly is the ratio of G_{mi} and G_{di}. After all, the ratio of $(G_{mi} + G_{bi})/G_{di}$ can be determined from (14) and $\partial R_d / \partial V_d$ from (13).

A good approximation of the MOSFET's current-voltage characteristic for a N-channel device in strong inversion is

$$I_{\text{drain}} = \frac{\beta}{f}\left(V_g - V_{\text{th}} - \frac{1}{2}[1+\delta]V_d\right)V_d \tag{34}$$

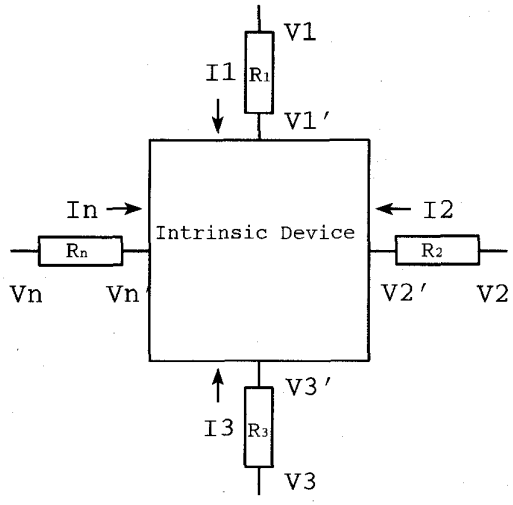

Fig. 15. Arbitrary N-terminal device with N bias dependent series resistors.

with

$$V_{\text{th}} = V_{t0} + \gamma(\sqrt{2\phi_f + V_{sb}} - \sqrt{2\phi_f}) \tag{35}$$

$$\begin{aligned} f = 1 &+ \theta_a(V_g - V_{\text{th}})^{\frac{1}{3}} + \theta_d(V_g - V_{\text{th}})^2 \\ &+ \theta_b(\sqrt{2\phi_f + V_{sb}} - \sqrt{2\phi_f}). \end{aligned} \tag{36}$$

In general the function f describes the channel mobility reduction due to the transversal electrical field. In (36) this mobility reduction is modeled as a function of the gate and bulk bias. Of course also another approximation could have been taken.

Using (34) the following conductances can be calculated.

$$G_{mi} = \frac{\beta V_d}{f}\left[1 - \left(V_g - V_{\text{th}} - \frac{1}{2}[1+\delta]V_d\right)\frac{f_1}{f}\right] \tag{37}$$

$$G_{bi} = \frac{K\beta V_d}{f}\left[1 - \left(V_g - V_{\text{th}} - \frac{1}{2}[1+\delta]V_d\right)\frac{f_1 - \theta_b}{f}\right] \tag{38}$$

$$G_{di} = \frac{\beta}{f}(V_g - V_{\text{th}} - [1+\delta]V_d). \tag{39}$$

In (37)–(39), δ is the body effect coefficient and K is the so called body effect factor

$$K = \frac{\partial V_{\text{th}}}{\partial V_{sb}} = \frac{\gamma}{2\sqrt{2\phi_f + V_{sb}}}. \tag{40}$$

The variable f_1 equals

$$f_1 = \theta_a(V_g - V_{\text{th}})^{-0.66} + 2\theta_d(V_g - V_{\text{th}}).$$

In general the mobility reduction parameter θ_b is much smaller than the mobility reduction parameter θ_a. Also a decrease of the channel mobility due the bulk bias is only noticeable at a high bulk bias. Therefore at a low drain bias, (37)–(39) can be rewritten as ($\theta_b = 0$)

$$G_{mi} = \frac{\beta V_d}{f}\left[1 - (V_g - V_{\text{th}})\frac{f_1}{f}\right] \tag{41}$$

$$G_{bi} = \frac{K\beta V_d}{f}\left[1 - (V_g - V_{\text{th}})\frac{f_1}{f}\right] \tag{42}$$

$$G_{di} = \frac{\beta}{f}(V_g - V_{\text{th}}). \tag{43}$$

The conclusion is that at low drain bias the ratio of G_{bi} and G_{mi} equals K. This last results remains valid as long as the MOSFET is working in its ohmic region. At low drain voltage the ratio of $(G_{mi}+G_{bi}+G_{di})/G_{di}$ can be rewritten as

$$\frac{G_{mi}+G_{bi}+G_{di}}{G_{di}} = \frac{(1+K)G_{mi}+G_{di}}{G_{di}} = 1+\frac{(1+K)G_{mi}}{G_{di}}. \quad (44)$$

From this latter equation, the ratio of G_{mi}/G_{bi} is easily determined.

In principle we are now able to measure the derivative of the series resistance with respect to the gate bias at low drain bias. The only problem that remains, is the determination of the integration constant. That problem is however quite simple to solve because one can measure the change of the MOSFET's channel resistance with gate bias

$$\frac{\partial R_{\rm ch}}{\partial V_g} = \left(\frac{\partial R_t}{\partial V_g} - \frac{\partial R_{\rm series}}{\partial V_g}\right) = \frac{1}{\beta V_{gt}^2}(f_1 V_{gt} - f) = \frac{1}{\beta}\left(\theta_d - \frac{2}{3}\theta_a V_{gt}^{-1\frac{2}{3}} - V_{gt}^{-2}\right). \quad (45)$$

Substitution of $X^{-1} = (V_g - V_t)^{\frac{1}{3}}$ in (45) gives

$$\frac{\partial R_{\rm ch}}{\partial V_g} = \frac{1}{\beta}\left(\theta_d - \frac{2}{3}\theta_a X^5 - X^6\right). \quad (46)$$

From a plot of $\partial R_{\rm ch}/\partial V_g$ versus X the coefficients θ_a, θ_d and β are estimated. Because the intrinsic resistance of the MOSFET ($R_{\rm ch}$) is known now, the value of the series resistance at a low drain voltage is the difference between R_t and $R_{\rm ch}$.

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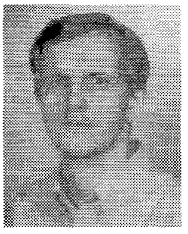

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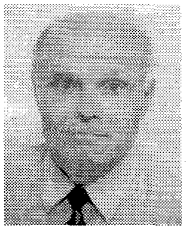

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From 1961 until 1993, he has been at the Philips Research Laboratories of Eindhoven, The Netherlands. During this period he was with the Research Laboratories of Northern Telecom, Ottawa, Ontario, Canada, for several years. In 1982, he was appointed as chief-scientist of Philips Research. Major subjects of his research activities have been, successively: photoconductive layers for video cameras, noise in various types of transistors, UHF MOSFET tetrodes, physical electronics of IC components (I^2L, BICMOS, MOSFET scaling, small-size devices of s-RAM) and circuit-level MOSFET modeling. Among his numerous publications is a book on Compact transistor modeling for IC design (Springer-Verlag, Vienna). Since 1971 he is working as part-time Professor in Microelectronics at the Technical University of Eindhoven and after retiring at Philips also at the RWTH of Aachen, Germany. He has been the promoter of 15 Ph.D. candidates and has been responsible for 60 M.Sc. Theses.

Dr. Klaassen has been serving, since 1980, as Regional Editor and later as Editor of *Solid State Electronics* (Elsevier Science).