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Research Article

A Novel Three-Input Field Effect Transistor with Parallel Switching Function Using T-Shaped Channel

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In this article, a novel three-input field effect transistor with parallel switching function (PSF-TiFET) is proposed. The channels of the new device consist of a vertical subchannel and two horizontal subchannels. The two horizontal subchannels are manufactured over the vertical subchannel by using smart-cut process. The top gate is located above the two horizontal subchannels. The front gate and back gate below the two horizontal subchannels are located on the two sides of the vertical subchannel, respectively. Each of the all three gates has roughly the same control area on the channel, and thus, the all three gates have roughly the same effect on the device channel. Due to its special structure, the new device is logically equivalent to three conventional single-input transistors in parallel. Compared with the traditional field effect transistors with a single-input terminal, the new device can be used to simplify the circuit with the reduced transistor number. The impacts of body thickness, gate oxide thickness, and work function on device performance are investigated, and then the device optimizations are carried out. The current characteristic of the device is theoretically analyzed. Silvaco TCAD simulations show that the theoretical analysis agrees well with the TCAD simulation results. This work explores the feasibility of multi-input devices, which would facilitate its development.

1. Introduction

With shrinking device dimensions, the conventional transistor encounters significant challenges. The transistor with two-input terminals has attracted researchers' attentions owing to its potential to replace conventional transistors [1], since they can reduce the number of transistors [2–5]. However, there is still room for further improvements, such as the channel shape of the device and the number of input terminals.

In this article, we propose a novel three-input field effect transistor with parallel switching function (PSF-TiFET). The proposed PSF-TiFET device is logically equivalent to three conventional single-input transistors in parallel. Therefore, the circuit can be simplified to reduce the transistor count by using PSF-TiFETs, thus reducing power consumption. Due to the special channel structure of the new device, compared with the traditional field effect transistor, the control area of the gate on the channel is greatly increased, and thus, the turn-on current of the device is increased. The PSF-TiFET device can be fabricated by adding a few process steps based on the traditional dual-gate FinFET process, which indicates that the new device process can be compatible with the mainstream FinFET process. Silvaco TCAD is used to optimize device performance by selecting appropriate device parameters. A lookup table model of the optimized PSF-TiFET device is established for SPICE circuit-level simulations. Taking three-input NAND and three-input NOR as examples, the circuit performances obtained by SPICE simulations show that the circuit based on the new device has better comprehensive performance than the circuit using the conventional single-input devices.

The remainder of this article is organized as follows. Section 2 describes the structure and parameters of the proposed device. The fabrication flow for PSF-TiFET is also included in Section 2. The current characteristics of the new device are analyzed theoretically, and the results are verified by Silvaco TCAD simulations in Section 3. In Section 3, the

device optimizations are also described. In Section 3, a lookup table model based on the proposed PSF-TiFET is constructed, and then, logic cells are simulated with the proposed SPICE model. Finally, the conclusion of this work is included in Section 4.

2. Device Structure and Fabrication Flow

In this section, the structure and parameters of the proposed device are introduced, and then, the fabrication flows of the PSF-TiFET are presented.

2.1. The Structure and Parameters of the PSF-TiFET Device. The 3D view of the PSF-TiFET is shown in Figure 1(a), while Figure 1(b) is a cross-sectional view of the device. The PSF-TiFET device has three independent biasing input terminals: top gate, front gate, and back gate. As shown in Figure 1(b), we can see that the channel of the new device is composed of two horizontal subchannels (marked as Subchannel 1 and Subchannel 3) and a vertical subchannel (marked as Subchannel 2). The top gate and front gate control Subchannel 1. The front gate and back gate control Subchannel 2, while the top gate and back gate control Subchannel 3.

HfO_2 is used as the gate oxide material to reduce the gate-body leakage current [6]. The gates of the device use the material TiN, because the metal gate would eliminate the poly depletion problem of the polysilicon gate [7]. The channel of the PSF-TiFET device is undoped to avoid degrading of carrier mobility [8]. The source and drain regions use high doping concentrations [9].

The parameters of the PSF-TiPFET device are summarized in Table 1. The high doping concentrations N_d and N_s of both source and drain regions are selected as $2.0 \times 10^{19}\,\text{cm}^{-3}$. L_g is the channel length of the device. H_{fin1} is the fin height of the vertical subchannel (Subchannel 2), while H_{fin2} is the height of the horizontal subchannels (Subchannel 1 and Subchannel 3). In Table 1, the gate oxide thickness T_{ox}, body thickness Ts_i of the channel, and the gate work function Φ_m have been selected to optimize the performance of the PSF-TiFET according to the switching current ratio and turn-on current of the device.

2.2. The Fabrication Flow of the PSF-TiFET Device. The PSF-TiFET process is fully compatible with the FinFET process, only adding some steps on the basis of the traditional FinFET manufacturing process for a double-independent gate device, as shown in Figure 2.

First, undoped wafers are thermally oxidized [10], and then, the back gate areas of the device are selectively opened on the wafer by electron beam (EB) lithography. The silicon film is etched to form a sidewall of the vertical channel, as shown in Figure 2(a). After wafer cleaning, a high-K dielectric layer is deposited on the surfaces of the vertical sidewall by using atomic layer deposition (ALD) processing, and then, a chemical mechanical polishing (CMP) process is performed to remove extra part of the gate oxide layer, as shown in Figure 2(b).

The front gate areas of the PSF-TiFET are formed by EB lithography. After narrowing the fin-resist-mask width by O_2 ashing, fin-hard-masks are formed by reactive ion etching (RIE). Followed by the silicon film etching, the ALD process is conducted to form high-k dielectric gate oxide on the other sidewall surfaces, as shown in Figure 2(c), and then, the gate oxide of the front gate is formed on the other sidewall, as shown in Figure 2(d).

TiN as a gate material is uniformly deposited on the sidewalls of the Si fins by using the pressure-optimized reactive sputtering, as shown in Figure 2(e). To etch the connected TiN film at the top of the Si fin, RIE is carried out. By this step, the traditional double-independent gate FinFET has been fabricated, as shown in Figure 2(f).

On the basis of a traditional dual-independent-gate FinFET process, the PSF-TiFET can be fabricated by adding a few processing steps. In order to reduce the manufacturing difficulty, we directly deposit a high-K dielectric layer on the top of the vertical channel as the gate oxide layer, as shown in Figure 2(g). The two horizontal subchannels of the PSF-TiFET are fabricated by the smart-cut process [11]. CMP processing is employed to ensure the thickness of the horizontal subchannels, as shown in Figure 2(h). A high-K dielectric layer is deposited on the horizontal channel surfaces by using atomic layer deposition processing. Finally, TiN as a gate material is uniformly deposited by using the pressure-optimized reactive sputtering, as shown in Figure 2(i).

3. Results and Discussion

In this section, taking N-type PSF-TiFET as an example, the current characteristics of the device are theoretically analyzed, and then, the performances of the device are verified by using Silvaco TCAD simulations. In the TCAD simulation, CVT (the Lombardi constant voltage and temperature) mobility integration model, the FERMIDIRAC (Fermi-Dirac carrier statistics) carrier statistics model, and SRH (Shockley–Read–Hall) composite model are considered.

3.1. The Switching Modes of the PSF-TiFET Device. The PSF-TiFET device has three independent input terminals named as top gate, front gate, and back gate. Each terminal has two input logic states “0” and “1,” and the corresponding voltage is 0 V or 0.8 V, respectively. Therefore, there are eight kinds of switching states, as shown in Figure 3. When all the three input terminals are set as 0 V, the device is turned off. When one of all the three input terminals is 0.8 V, the device would be turned on. In this article, the source is biased to 0 V for N-type PSF-TiFET.

3.2. Threshold Voltage of the PSF-TiFET Device. One of the most important parameters of the transistor is the threshold voltage (V_{th}), which directly affects the drain current of the transistor [12]. The threshold voltage of a transistor can be approximated by

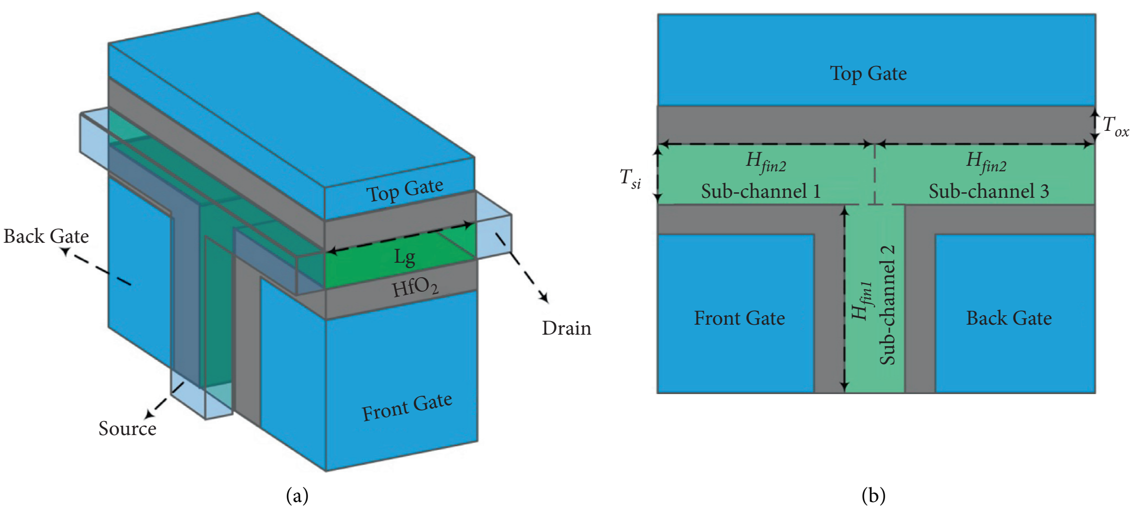


Figure 1: The structure of the PSF-TiFET device. (a) 3D view and (b) cross-sectional view.

Table 1: The optimized parameters of PSF-TiFET.

Parameter	Value
Source doping (N_s)	$2 \times 10^{19}\,\mathrm{cm}^{-3}$
Gate length (L_g)	24 nm
Fin height 2 (H_{fin2})	43 nm
Body thickness (T_{si})	6 nm
Drain doping (N_d)	$2 \times 10^{19}\,\mathrm{cm}^{-3}$
Fin height 1 (H_{fin1})	40 nm
Gate oxide thickness (T_{ox})	2 nm
Gate work function (Φ_m)	4.70 eV (N-type) 4.85 eV (P-type)

$$Vth = Vinv + \Phi m + \frac{Q^D}{C_{OX}} + V^{QM} - V^{SCE}, \quad (1)$$

where V_{inv} is a constant that represents the limited availability of inversion charges in the undoped channel, Φ_m is the difference between work function of electrode and silicon, Q^D is the depletion charge in the channel, C_{ox} is the gate capacitance, V^{QM} models the quantum-mechanical increase in the threshold voltage, and V^{SCE} models the short channel effect [13].

Q^D is relatively small in undoped or lightly doped channels, while C_{ox} has also little effect on the threshold voltage. Since the transverse electric field is low in undoped FinFETs with silicon thickness greater than 5 nm [14], V^{QM} can be negligible when T_{si} is in the 5–8 nm range. Therefore, in the optimization of the PSF-TiFET device, the threshold voltage is adjusted by selecting the appropriate gate work function.

It is worthwhile to note that a strong channel coupling effect is found in our T-shaped channel. For Subchannel 1, the threshold voltage of the top gate or front gate is a function of the voltage of another gate [15]. Similarly, for Subchannel 2, the threshold voltage of the front gate or back gate is a function of the voltage of the other gate, while for Subchannel 3, the threshold voltage of the top gate or back gate is also a function of another gate. For the threshold voltage of Subchannel 1, the effect factor ($\gamma_{f\text{-}t\text{-Subchannel 1}}$) of the front gate to the top gate is given by

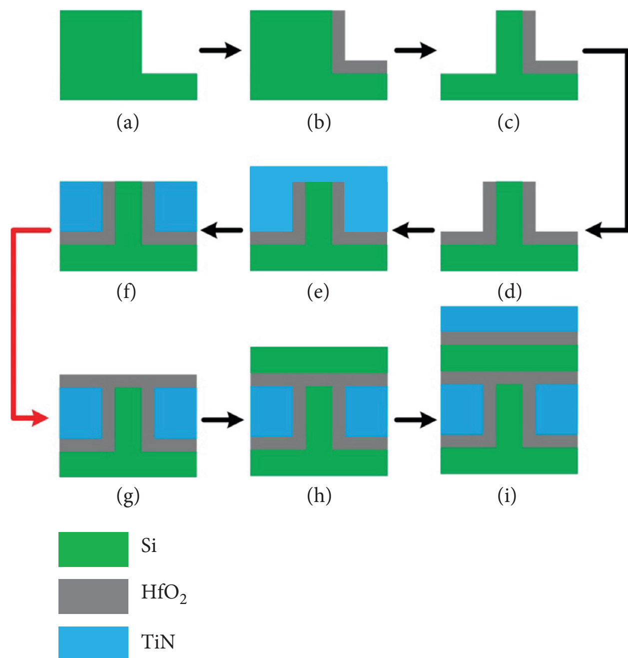


Figure 2: The fabrication flow of the PSF-TiFET device. (a) Formation of a right sidewall of the Si-fin channels, (b) the formation of high-K dielectric layer on the right sidewall, (c) formation of another left sidewall of the Si-fin channels, (d) formation of the gate oxide of the front gate on the left sidewall, (e) TiN deposition, (f) gate separation by RIE, (g) formation of the oxide layer on the top gate, (h) formation of a horizontal channel by using smart-cut processing, and (i) formation of the high-K dielectric layer and the top gate.

$$\gamma_{f-t-\text{Subchannel1}} = \frac{\partial V_{tht-\text{Subchannel1}}}{\partial V_{fgs}} \cong \frac{12T_{ox}}{12T_{ox} + 24T_{si}} = \frac{Tox}{T_{ox} + 2T_{si}}, \quad (2)$$

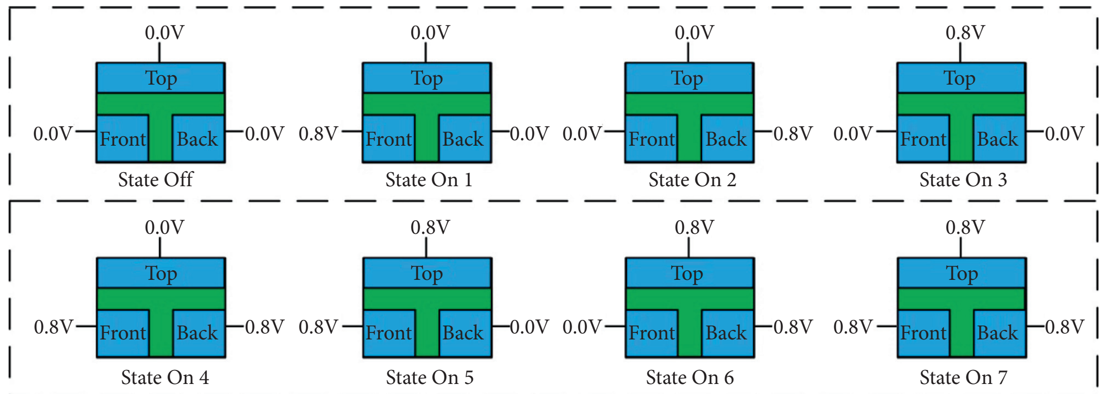


Figure 3: Eight kinds of switching states of the N-type PSF-TiFET device.

where $V_{tht\text{-Subchannel 1}}$ is the threshold voltage of the top gate for Subchannel 1, V_{fgs} is the front gate to source voltage, and T_{ox} and T_{si} are the thickness of the gate oxide and Subchannel 1, respectively. By using TCAD simulations, it is found that the threshold voltage of the top gate for Subchannel 1 is not completely linear as the front gate to source voltage varies, as shown in Figure 4.

The threshold voltage ($V_{tht\text{-Subchannel1}}$) of the top gate for Subchannel 1 can more precisely be expressed, which is given by

$$V_{tht-\text{Subchannel1}} = V_{tht0-\text{Subchannel1}} - \gamma_{f-t-\text{Subchannel1}} \cdot V_{fgs} - A \cdot V_{fgs} - B \cdot V_{fgs}^2 - C \cdot V_{fgs}^3, \quad (3)$$

where $V_{tht0\text{-Subchannel 1}}$ is the threshold voltage of the top gate for Subchannel 1 when the front gate to source voltage is 0 V, and A, B, and C are fitting parameters.

The analytical model of (3) and the TCAD simulation results of threshold voltage of the top gate for Subchannel 1 are compared in Figure 4. From Figure 4, the theoretical analysis agrees well with the TCAD simulation results.

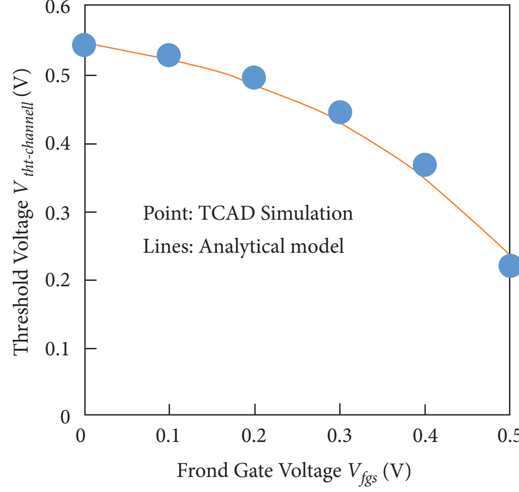


Figure 4: The analytical model and TCAD simulation results of the threshold voltage of the top gate for Subchannel 1.

3.3. Current Model of the PSF-TiFET Device When One of the Three Input Terminals Is Activated.

The total current of the PSF-TiFET device is composed of the currents through all the three subchannels, which can be expressed as

$$I_{ds} = I_{ds\,1} + I_{ds\,2} + I_{ds\,3}, \quad (4)$$

where I_{ds} is the total current of the device, and I_{ds1}, I_{ds2}, and I_{ds3} are currents through Subchannel 1, Subchannel 2, and Subchannel 3, respectively.

The three gates of the PSF-TiFET device have almost the same effect on the corresponding subchannels. Therefore, we take one gate as an example to address its current model. We assume that the top gate to source voltage V_{tgs} is set as 0.8 V, while both the front gate to source voltage V_{fgs} and the back gate to source voltage V_{bgs} are set as 0 V (i.e., Turn-on State 3 as shown in Figure 4). Figure 5 shows the current density distribution of the device at Turn-on State 3. From Figure 5, Subchannel 1 and Subchannel 3 have large current density (I_{ds1} and I_{ds3}) because of the activated top gate, while Subchannel 2 has hardly any current distribution because

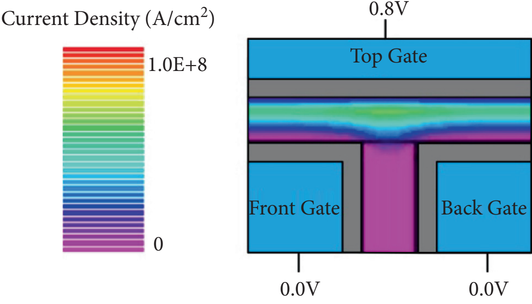


Figure 5: The current density distribution of the PSF-TiFET device at $V_{ds} = 0.8$ V when the V_{tgs} is set as 0.8 V and both V_{fgs} and V_{bgs} are set as 0 V.

the front gate and back gate are set as 0 V. Therefore, there is almost no crosstalk between subchannels when one input terminal is activated.

The current model of the PSF-TiFET device can be addressed in the subthreshold region and strong inversion region, respectively, when the device changes from turn-off state to Turn-on State 3. Taking Subchannel 1 as an example,

the current model of the PSF-TiFET device in the subthreshold region is given by

$$I_{Sub1s} = D \cdot \frac{H_{fin} \cdot T_{si}}{L_g} \cdot exp^{V_{tgs}+\lambda \cdot V_{ds}-V_{tht0-\text{Subchannel1}}/n \cdot V_T} \cdot \left(1 - exp^{-V_{ds}/V_T}\right), \quad (5)$$

where I_{Sub1s} is the current through Subchannel 1 in the subthreshold region only when the top gate is activated, D and λ are fitting parameters, n is the subthreshold slope parameter [16], and V_T is the thermal [17]voltage.

The current model of the PSF-TiFET device in the strong inversion region is given by

$$I_{D1s} = E \cdot \frac{H_{fin} \cdot T_{si}}{L_g} \cdot \left(V_{tgs} - V_{tht0-\text{ Subchannel1}}\right)^{\alpha} \cdot \left(1 + \beta \cdot V_{ds}\right), \quad (6)$$

where I_{D1s} is the current through Subchannel 1 in the strong inversion region only when the top gate is activated, and E, α, and β are fitting parameters.

Figure 6 plots the simulated curve of the drain current of the PSF-TiFET device as a function of V_{tgs}, where V_{ds} is 0.8 V, while both the front gate to source voltage V_{fgs} and the back gate to source voltage V_{bgs} are set as 0 V. We sweep V_{tgs} from 0 V to 0.8 V. Figure 6 also plots the calculated results of the drain current of the PSF-TiFET device by using subthreshold model equation (5) and the strong inversion region (6). The result shows that the theoretical formula of the drain current agrees well with the TCAD simulation results.

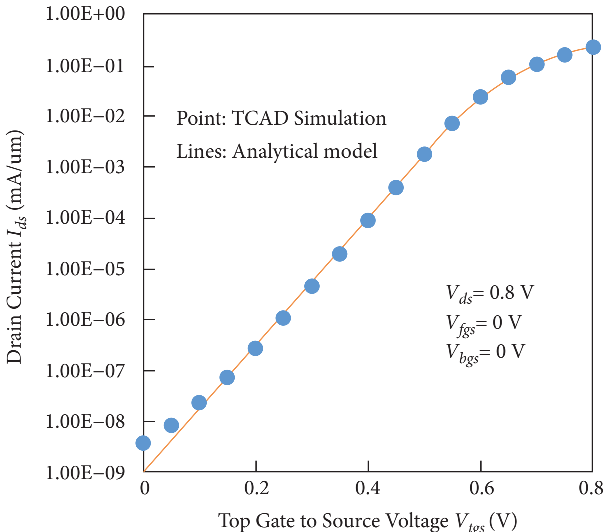


Figure 6: The simulation and calculated results of the current through Subchannel 1 and Subchannel 3 versus V_{tgs} with $V_{ds} = 0.8$ V and $V_{fgs} = V_{bgs} = 0$ V.

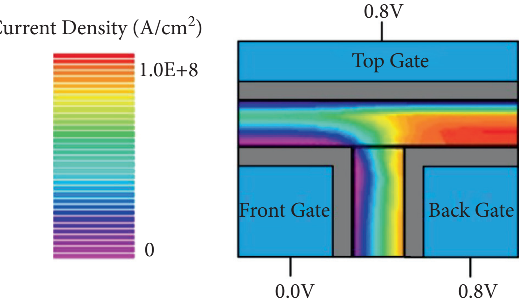


Figure 7: The current density distribution of the PSF-TiFET device at $V_{ds} = 0.8$ V at Turn-on State 6.

3.4. Current Model of the PSF-TiFET Device When Two of the Three Input Terminals Are Activated. Figure 7 shows the current density distribution of the device at Turn-on State 6, where both top gate and back gate are set as 0.8 V, while the front gate is set as 0 V. Subchannel 1 and Subchannel 2 are activated by a single gate that is the top gate and back gate, respectively, and thus, the current density through Subchannel 1 and Subchannel 2 is approximately the same. From Figure 7, Subchannel 3 is activated by both top and back gates and thus has a much higher current density than the other two subchannels. Since Subchannel 1, Subchannel 2, and Subchannel 3 are connected together, the connection becomes a transition region for current density. Crosstalk can be ignored because the area of the transition region is small compared to the subchannel.

The PSF-TiFET device changes from the turn-off state to the turn-on state, when the top gate and back gate are shorted tied and scanned from 0 V to 0.8 V, while the front gate to source voltage is set as 0 V. The current through Subchannel 1 and Subchannel 2 can be described by (5) and (6). The current through Subchannel 3 in the subthreshold region and strong inversion region is given by the following equations, respectively:

$$I_{Sub3\ d} = F \cdot \frac{H_{fin} \cdot T_{si}}{L_g} \cdot \frac{\varepsilon_{ox}}{T_{ox}} \cdot {V_T}^2 \cdot exp^{V_{tgs}-V_{th\ d3}/n \cdot V_T} \cdot \left(1 - exp^{-V_{ds}/V_T}\right), \quad (7)$$

where I_{Sub3d} is the current of the device through Subchannel 3 in the subthreshold region when $V_{tgs} = V_{bgs}$, F is the fitting parameter, ε_{ox} is the dielectric constant of the gate oxide, and V_{thd3} is the threshold voltage of Subchannel 3 when $V_{tgs} = V_{bgs}$ [18].

$$I_{D3\ d} = G \cdot \frac{H_{fin} \cdot T_{si}}{L_g} \cdot \left[\left(V_{tgs} - V_{th\ d3}\right)^{\omega} - 8r \cdot {V_T}^2 \cdot exp^{V_{tgs}-V_{ds}-(V_{th\ d3}-0.05)/V_T}\right], \quad (8)$$

where I_{D3d} is the current through Subchannel 3 in the strong inversion region when $V_{tgs} = V_{bg}$, G and ω are fitting parameters, and r is a structural parameter [19].

We can add the currents of the three subchannels to obtain the total current model of the device through (4). The drain current of the device versus the top gate to source voltages is shown in Figure 8, where V_{ds} is set as 0.8 V, V_{fgs} is set as 0 V, and the back gate is short-tied with the top gate. The calculation results of the theoretical formula of drain current are validated by TCAD simulations with a good agreement.

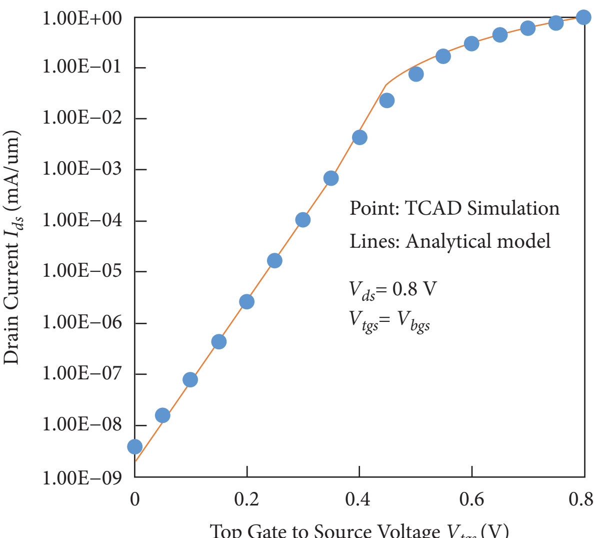


Figure 8: The simulation and calculated results of the current versus V_{tgs} with $V_{ds} = 0.8$ V and $V_{fgs} = 0$ V.

3.5. The Performance Optimization of PSF-TiFET Devices. In order to obtain high performances, taking N-type PSF-TiFET as an example, we explore the effect of device parameters on device performance by changing the body thickness, the thickness of the gate oxide layer, and gate work function.

The proposed device is logically equivalent to three conventional single-input transistors in parallel. Therefore, in order to achieve good performance, the device current should be as large as possible, when only one gate is set as 0.8 V. What's more, the subthreshold slope of the PSF-TiFET device should also be considered. The subthreshold slope S is given by [20]

$$S = \frac{\partial V_{tgs}}{\partial \log_{10} I_{Sub}} = \ln 10 \cdot \frac{KT}{q} \cdot \frac{\partial V_{tgs}}{\partial \Psi_s}, \tag{9}$$

where I_{Sub} is the current of the PSF-TiFET in the subthreshold region, ψ_s is the surface potential at the gate electrode. Only when one input terminal is activated, the subthreshold slope can use the following equation as a reference [21, 22]:

$$S = 60 \cdot \frac{0.5T_{ox} + T_{si} + 0.5T_{ox}}{0.5T_{ox} + T_{si}} = 60 \cdot \left(1 + \frac{0.5T_{ox}}{0.5T_{ox} + T_{si}}\right). \tag{10}$$

According to (10), we can select suitable body thickness T_{Si} and gate oxide thickness T_{ox} to optimize the subthreshold slope S of the PSF-TiFET device.

3.5.1. Effect of Gate Work Function on the Current Characteristics. When all gates are set as 0 V, the device is turned off, and the current is called as the turn-off current I_{off}. When at least one gate is set as 0.8 V, the device is turned on, and the current is called as the turn-on current I_{on}.

It can be seen from (1) that the threshold of the PSF-TiFET becomes larger as the gate work function Φ_m is increased. Therefore, a suitable threshold of the PSF-TiFET can be adjusted by selecting the gate work function.

It can be seen from (6) that I_{on} is decreased as the threshold of the PSF-TiFET is increased. Therefore, the I_{on} of the PSF-TiFET can be changed by selecting the different gate work functions. Figure 9 shows the effect of gate work function on the current characteristics, where both V_{fgs} and V_{bgs} are set as 0 V.

It can be seen from Figure 9 that as the gate work function Φ_m is increased from 4.65 eV to 4.85 eV, both I_{off} and I_{on} of the device are decreased, while the switch current ratio I_{on}/I_{off} is increased. When the gate work function Φ_m is 4.75 eV, I_{on} will be less than 0.15 mA/um, which is too small for a FinFET device, and thus, the gate work function Φ_m should be selected as <4.75 eV.

From Figure 9, the switching current ratio exceeds 5×10^7 when the gate work function Φ_m is 4.70 eV, which is acceptable for a FinFET device. Therefore, in order to obtain a large I_{on} and an acceptable I_{on}/I_{off}, Φ_m is set at 4.70 eV in our work.

3.5.2. Effect of Body Thickness and Gate Oxide Thickness on the Turn-On Current. In this subsection, the effects of body thickness T_{si} and gate oxide thickness T_{ox} on the PSF-TiFET performance are explored. Figure 10 shows the effects of body thicknesses and gate oxide thicknesses on the turn-on current, where V_{tgs} is set as 0.8 V, while V_{fgs} and V_{bgs} are set as 0 V.

It can be seen from Figure 10 that I_{on} is gradually enhanced, as the body thickness T_{si} is increased from 5 nm to 7 nm. However, I_{on} exhibits a continuous decrease trend as T_{ox} is increased from 2 nm to 5 nm.

3.5.3. Effect of Body Thickness and Gate Oxide Thickness on the Switching Current Ratio. Figure 11 shows the switching current ratio for different body thicknesses and gate oxide thicknesses, where V_{tgs} is set as 0.8 V, while V_{fgs} and V_{bgs} are set as 0 V. It is observed that the switching current ratio is decreased as body thickness T_{si} is increased. The switching current ratio is increased as T_{ox} is decreased from 5 nm to 2 nm. In order to obtain a large I_{on} and an acceptable I_{on}/I_{off}, optimized T_{si} and T_{ox} are set to 6 nm and 2 nm, respectively.

3.6. Drain Induced Barrier Lowering (DIBL) of the PSF-TiFET. DIBL is defined as the threshold voltage shift due to drain variation. For the top gate of the PSF-TiFET, DIBL is calculated from the following equation:

$$\text{DIBL} = \frac{\Delta V_{tht-\text{Sub}-\text{channel1}}}{\Delta V_{ds}}. \tag{11}$$

The drain current of the PSF-TiFET is shown in Figure 12, where V_{fgs} and V_{bgs} are set as 0 V, and the top gate is swept from 0 V to 0.8 V. According to (11), the DIBL of the device is about 21.33 mV/V. This is mainly due to the thin

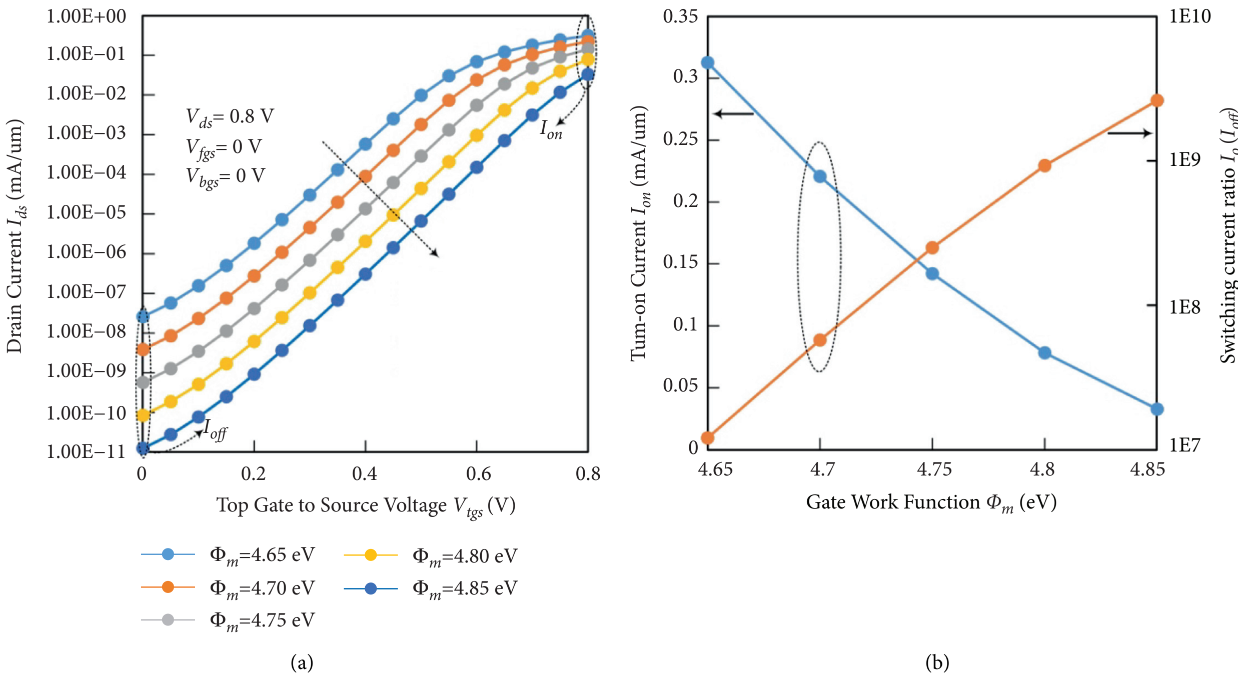


Figure 9: (a) The drain current I_{ds} and (b) turn-on current I_{on} and switching current ratio I_{on}/I_{off} with different work functions when both V_{fgs} and V_{bgs} are set as 0 V.

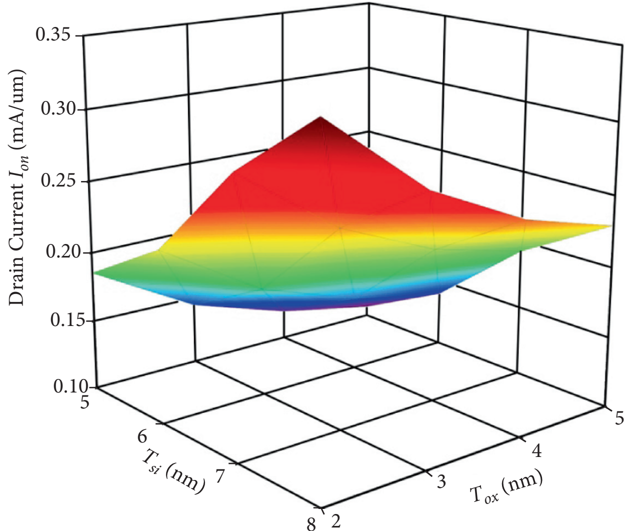


Figure 10: The turn-on current I_{on} with different T_{si} and T_{ox} at Turn-on State 3.

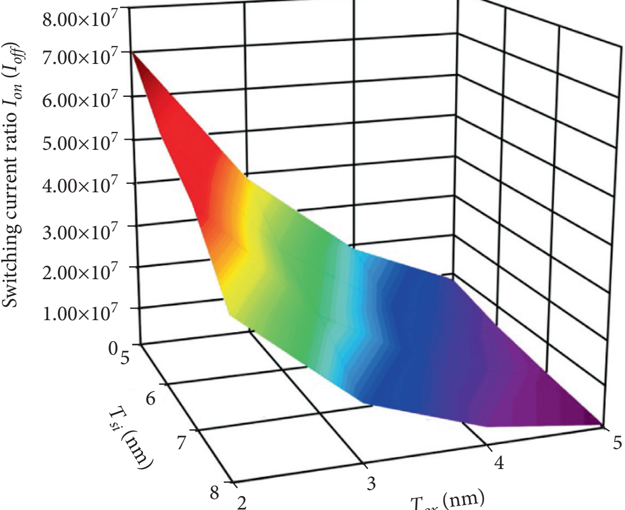
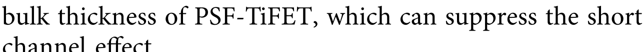


Figure 11: The switching current ratio I_{on}/I_{off} with different T_{si} and T_{ox} at Turn-on State 3.



bulk thickness of PSF-TiFET, which can suppress the short channel effect.

3.7. Current Characteristics of the Optimized Device. Table 2 gives the current of the N-type PSF-TiFET in the eight switching states. From Table 2, when all gates are set as 0 V, the device is turned off, and its turn-off current (I_{off}) is 3.85×10^{-9} mA/um. When at least one gate is set as 0.8 V, the device is turned on. Since the three gates have almost the same effect on the subchannel, the turn-on currents of the device are almost the same when one gate is activated (i.e., Turn-on State 1, Turn-on State 2, and Turn-on State 3). From Table 2, the minimum turn-on current (I_{on}) is 0.21 mA/um, and thus, minimum switching current ratio I_{on}/I_{off} is 5.45×10^7.

When both gates are activated (i.e., Turn-on State 4, Turn-on State 5, and Turn-on State 6), the turn-on current is 0.93 mA/um. When all three gates are activated (i.e., Turn-on State 7), the maximum turn-on current of the device is 2.13 mA/um.

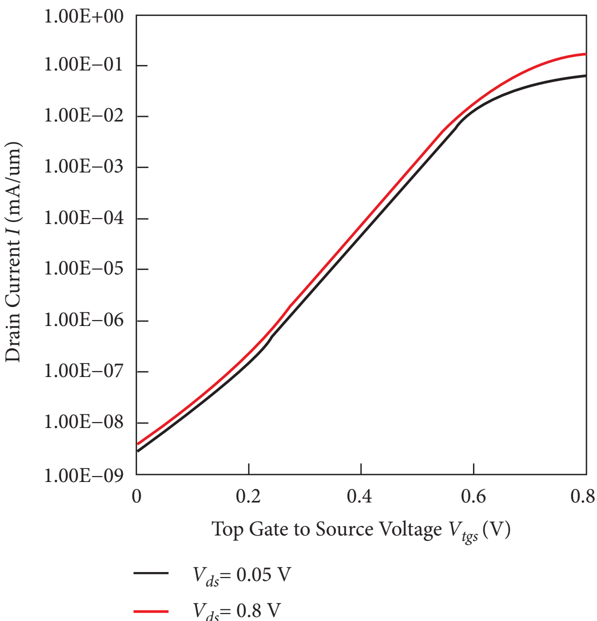


Figure 12: Drain current of the PSF-TiFET with different V_{ds}, where V_{fgs} and V_{bgs} are 0 V.

Table 2: The turn-on current and turn-off currents of the N-type PSF-TiFET.

Switching States	V_{tgs} (V)	V_{fgs} (V)	V_{bgs} (V)	I_d (mA/um)	Current States
Turn-off State	0	0	0	3.85×10^{-9}	Current State 1
Turn-on State 1	0	0.8	0	0.22	
Turn-on State 2	0	0	0.8	0.21	Current State 2
Turn-on State 3	0.8	0	0	0.22	
Turn-on State 4	0	0.8	0.8	0.93	
Turn-on State 5	0.8	0.8	0	0.93	Current State 3
Turn-on State 6	0.8	0	0.8	0.93	
Turn-on State 7	0.8	0.8	0.8	2.13	Current State 4

Therefore, according to the drain current of the device, the eight switching states of the device can be divided into four different current states.

Table 3 gives the current of the P-type PSF-TiFET in the eight switching states. From Table 3, when all gates are set as 0.8 V, the device is turned off, and its turn-off current (I_{off}) is 1.12×10^{-9} mA/um. When at least one gate is set as 0 V, the device is turned on. Since the three gates have almost the same effect on the subchannel, the turn-on current of the device is almost the same when one gate is activated (i.e., Turn-on State 1, Turn-on State 2, and Turn-on State 3). From Table 3, the minimum turn-on current (I_{on}) is 0.20 mA/um, and thus, minimum switching current ratio I_{on}/I_{off} is 1.79×10^6.

When both gates are activated (i.e., Turn-on State 4, Turn-on State 5, and Turn-on State 6), the turn-on current is 0.70 mA/um. When all three gates are activated (i.e., Turn-on State 7), the maximum turn-on current of the device is 1.46 mA/um.

Therefore, according to the drain current of the device, the eight switching states of the device can be divided into four different current states.

3.8. Logic Cells Using PSF-TiFET Devices. It can be seen from the switching states of the PSF-TiFET device that the proposed PSF-TiFET devices make it possible to merge three traditional single-input devices in parallel. Therefore, three parallel transistors in the pull-down or pull-up network of the logic gate can be merged with a single PSF-TiFET device to get a compact low power implementation of the same Boolean function.

A three-input NOR gate using static complementary logic consists of 6 single-input devices, as shown in Figure 13(a). The three parallel transistors in the pull-down can be merged by using a PSF-TiFET device, as shown in Figure 13(b).

In order to perform the circuit simulation of the PSF-TiFET device in the SPICE simulator, we need a SPICE model for the PSF-TiFET device. The SPICE model based on the lookup table is an appropriate choice for a new device. We use TCAD simulator to extract data of the PSF-TiFET device and set the lookup table [23]. Then, a Verilog-A lookup model is built for the circuit-level simulation. Simulation waveforms of the three-input NOR logic cell is shown in Figure 14.

Table 3: The turn-on current and turn-off currents of the P-type PSF-TiFET.

Switching States	V_{tgs} (V)	V_{fgs} (V)	V_{bgs} (V)	I_d (mA/um)	Current States
Turn-off State	0.8	0.8	0.8	1.12×10^{-7}	Current State 1
Turn-on State 1	0.8	0	0.8	0.21	
Turn-on State 2	0.8	0.8	0	0.20	Current State 2
Turn-on State 3	0	0.8	0.8	0.21	
Turn-on State 4	0.8	0	0	0.70	
Turn-on State 5	0	0	0.8	0.70	Current State 3
Turn-on State 6	0	0.8	0	0.70	
Turn-on State 7	0	0	0	1.46	Current State 4

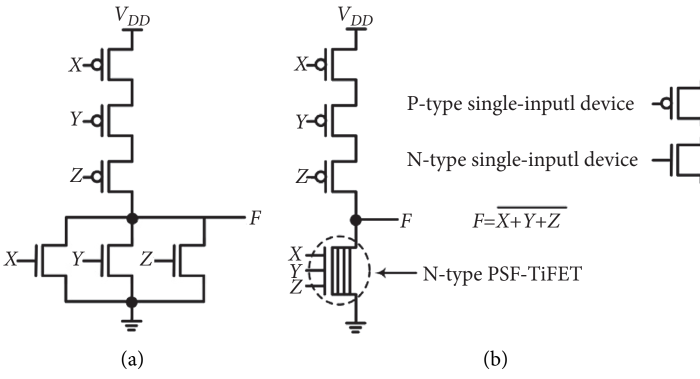


Figure 13: The three-input NOR gate using (a) the single-input device and (b) the PSF-TiFET device.

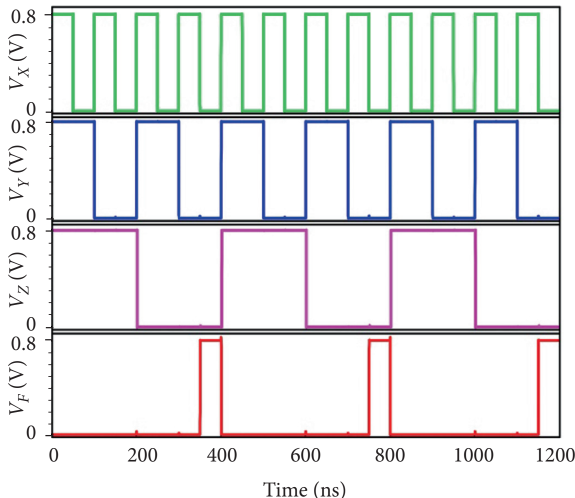


Figure 14: The simulated waveforms of the three-input NOR.

Table 4: The power consumption, delay, and power delay product of the three-input NOR logic cell using PSF-TiFET device are compared with using single-input devices.

NOR	Power consumption (nW)	Delay (pS)	Power delay product (zJ)
PSF-TiFET device	33.63	124.6	4190.29
Single-input devices	73.28	87.8	6364.24

The power consumption, delay, and power delay product of the three-input NOR logic cell using PSF-TiFET device are compared with using single-input devices in Table 4. From Table 4, the power consumption and power delay product of the three-input NOR logic cell using the PSF-TiFET device are smaller than single-input devices with an acceptable delay penalty.

A three-input NAND gate using static complementary logic consists of 6 single-input devices, as shown in Figure 15(a). The three parallel transistors in the pull-down

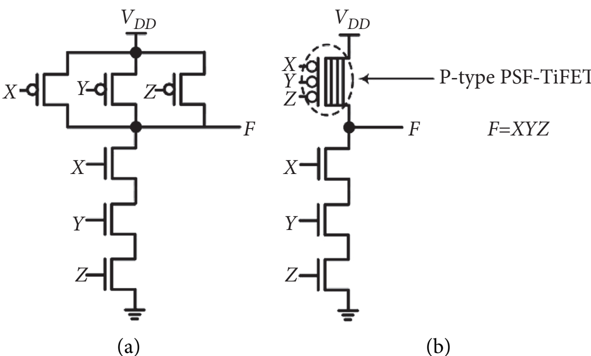


Figure 15: The three-input NAND gate using (a) the single-input device, and (b) the PSF-TiFET device.

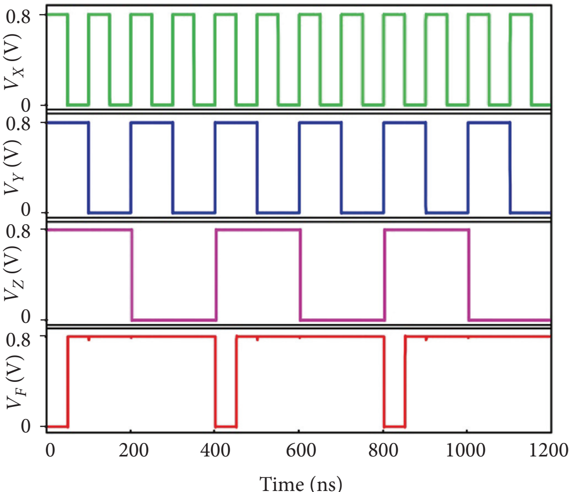


Figure 16: The simulated waveforms of the three-input NAND.

Table 5: The power consumption, delay, and power delay product of the three-input NAND logic cell using PSF-TiFET device are compared with using single-input devices.

NAND	Power consumption (nW)	Delay (pS)	Power delay product (zJ)
PSF-TiFET device	10.40	171.7	1785.68
Single-input devices	18.47	118.5	2188.70

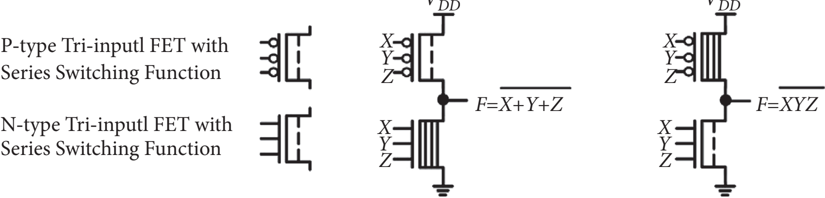


Figure 17: The three-input NOR gate and the three-input NAND gate based on the devices with series switching function and PSF-TiFET devices.

can be merged by using a PSF-TiFET device, as shown in Figure 15(b). Simulation waveforms of the three-input NAND logic cell are shown in Figure 16.

The power consumption, delay, and power delay product of the three-input NAND logic cell using PSF-TiFET device are compared with using single-input devices in Table 5. From Table 5, the power consumption and power delay product of the three-input NAND logic cell using the PSF-TiFET device are smaller than single-input devices with an acceptable delay penalty.

PSF-TiFET devices behave like the OR function, and thus, they are suitable for merging parallel single-input devices in pull-up or pull-down network of the logic gate. In order to merge series single-input devices, we need a kind of device that behave the AND function. In other words, we can design a new device with series switching function to further simplify the circuit with PSF-TiFET devices in the future. As shown in Figure 17, it is possible to implement the three-input NAND gate and NOR gate using only two devices.

4. Conclusions

In this article, we propose a novel field effect transistor with three-input terminals. The special channel structure of the new device increases the coupling area between both sides of the subchannels. With suitable gate work function, body thickness, and gate oxide thickness, the PSF-TiFET devices have excellent performance with the parallel switching function. The SPICE simulation model has also been established for the optimized device to circuit-level simulations. The purpose of this article is to propose a three-input device that can simplify the circuit and provide a new idea for the future design of integrated circuits.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this article.

Acknowledgments

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