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A Novel Three-Phase Switched-Capacitor Five-Level Multilevel Inverter with Reduced Components and Self-Balancing Ability

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Abstract: This paper proposes a step-up 3-ϕ switched-capacitor multilevel inverter topology with minimal switch count and voltage stresses. The proposed topology is designed to provide five distinct output voltage levels from a single isolated dc source, making it suitable for medium and low-voltage applications. Each leg of the proposed topology contains four switches, one power diode, and a capacitor. The switching signals are also generated using a staircase universal modulation method. As a result, the proposed topology will operate at both low and high switching frequencies. To highlight the proposed topology's advantages, a comparison of three-phase topologies wasperformed in terms of the switching components, voltage stress, component count per level factor, and cost function withthe recent literature. The topology achieved an efficiency of about 96.7% with dynamic loading, and 75% of the switches experienced half of the peak output voltage (V_{DC}), whereas the remaining switches experienced peak output voltage ($2V_{DC}$) as voltage stress. The MATLAB/Simulink environment was used to simulate the proposed topology, and a laboratory prototype was also built to verify the inverter's theoretical justifications and real-time performance.

Keywords: cost function; multilevel inverter; pulse width modulation; switched capacitor; total standing voltage

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1. Introduction

In recent years, research has focused on renewable energy sources in order to conserve conventional energy resources and avoid global warming and climate change. Renewable energy sources, such as photovoltaic, windmills, and ocean, are the future of the energy system and a true solution to the world's energy concerns, since they have a significant factor in technological and economic advancement and prosperity. This renewable energy source is one of the most promising long-term energy sources [1,2]. Inverters, which use DC-to-AC power conversion techniques, are used to generate, transmit, distribute, and utilize electric power. After considering the shape of the output voltage waveform, inverters are classed as two-level, three-level, PWM inverters, and multilevel inverters (MLIs). MLI has a major benefit over other inverters due to its lower dv/dt stress, less electromagnetic interference, enhanced power quality, and increased efficiency. MLI topologies, such as the neutral point clamped (NPC), the flying capacitor (FC), and the cascaded H-bridge

(CHB),are some of the most common and classic topologies. These topologies have been used extensively in a wide variety of applications in energy storage and electrical conversion systems. NPC and FC inverters are responsible for the introduction of the balanced charging problem of DC link capacitors. In order to generate higherlevel output, the CHB design necessitates the utilization of a significant number of discrete DC voltage sources. In addition to this, each of these traditional topologies calls for an increasing quantity of semiconductor components in proportion to the number of output levels. Because of these factors, the reduction in semiconductor components as well as passive parts has become a key priority. This lessens the size and weight of the entire system, as well as the conduction and switching losses, and increases the efficiency of the system overall [3,4]. In contrast to NPC, FC, CHB, and MMC, which have been commercialized in medium- and high-voltage applications, SC-based MLIs (SCMLIs) have primarily been developed for low/high voltage applications because they have the advantages of voltage-boosting capability as well as the voltages of self-balanced capacitors. As a result, the switched-capacitor (SC) architecture, which has gained increased attention from researchers in recent years to improve input voltage, eliminate switching components, and lower the requirements of DC sources, is the greatest invention. Therefore, researchers havestarted focusing on switched-capacitor multilevel inverter (SC-MLI) topologies. These SCMLIs are categorized as single-stage or two-stage topologies.

A single-stage SCMLI generates a bipolar waveform, and as a result, it offers the opportunity to incorporate power switches that require fewer PIVs, despite the fact that the total number of power switches across all levels is relatively high.As an illustration, the SCMLI that was proposed in ref. [5] makes use of switches with PIV, which is restricted to the input voltage, but it provides a waveform with a low resolution and a low voltage gain. It synthesizes seven levels with many switching components. A self-balanced MLI topology is presented in this paper to achieve the lowest possible TSV and PIV for switches that have the capability of staircase multilevel bipolar voltage generation. This type of SCMLI is also quite popular. It is developed by inserting an SC-based circuit. By doing away with the end-side H-bridge inverter, the suggested construction ensures that every component can tolerate voltage stress, which is equivalent to the input DC voltage [6,7]. Both topologies exhibit peak inverse voltage (PIV) within the supply voltage but employ more switches. A single-stage eight-switch SCMLI is proposed in ref. [8], which results five different levels at its output terminal. Despite this, it has the lowest voltage gain, and only a few of its switches are able to sustain high-voltage stress.

During the first stage of a two-stage SCMLI, a unipolar multilevel waveform is generated, and then, an H-bridge (or an equivalent) is used to unfold it into a bipolar waveform. The amplitude of the output voltage causes significant voltage stress, which is felt by these H-bridge switches for high-voltage AC power supplies.The structures that are suggested in refs. [9,10] are examples of topologies that have two stages. The SCMLI structure that was proposed in ref. [9] is an easily expandable one; however, it has a very large component count, and it provides a modest voltage gain while exhibiting a high CF.

For instance, the series/parallel SCMLI that was described by Hinago et al. [10] is capable of producing 2n + 3 different levels of ac output voltage, where n is the number of SC cells, and each level is comparable to the dc input voltage. In addition, the voltages of the capacitors in this SCMLI are automatically adjusted without the use of any additional balancing circuits or control algorithms. Moreover, it has large TSV and switching components.

A seven-level boost-ANPC inverter with eight switches is the subject of investigation in ref. [11], where it is abbreviated as 7L-Boost-ANPC. Compared to the typical multilevel inverter family, the dclink voltage need is lowered byhalf, and both the active and passive components can be scaled back for generalpurpose applications (such as rolling mills, fans, pumps, marine appliances, mining, traction, and grid-connected renewable energy, etc.). An ANPC 7L self-voltage balancing inverter (7L-SVBI) has a high gain and places low voltage stress on the switches. Despite this, they still necessitate a great deal of both active

and passive components, in addition to a larger dc link voltage, which is presented in ref. [12]. The input voltage can be increased using the two-stage topology described in refs. [12,13]. These topologies, however, include HB, which increases voltage stress and switching components.

A three-phase active neutral point clamped topology has been devised in recent years [14–16]. The first attempt to increase the voltage gain of a typical seven-level ANPC by 1.5 was madeby the author in ref. [14]. This was accomplished by suitably integrating a floating capacitor. It is common knowledge that two-stage boosting MLIs, which are excellent choices for photovoltaic power plants, are susceptible to damage as a result of the high voltage stress that is placed on the switches of the second stage. Single-stage boosting MLI, which requires a reduced number of switches, diodes, and capacitors, was proposed in ref. [15] for use in applications related to renewable power generation. For the generation of five different voltage levels, it onlyneeds a single capacitor and nine switches. Additionally, it lowers the voltage stress, which is placed on the switches.Researchers are investigating a novel six-switch five-level boost-ANPC inverter (5L-Boost-ANPC) for generalpurpose applications (such as rolling mills, fans, pumps, marine appliances, mining, tractions, and most notably, grid-connected renewable energy, etc.), which reduces the dc link voltage requirement to half of conventional 5L-NPC and 5L-FC family, as well as reducing the number of active and passive components [16]. In ref. [17], an MLI with five levels and grid connectivity is introduced. A shunt active filter is built to keep the system's actual power flow unimpeded.Moreover, the topology has an advantage in terms of ability enhancement.A three-phase hybrid cascaded modular multilevel inverter topology is presented in ref. [18]. Because of the benefits offered by the topology, the number of power switches, losses, installation space, voltage stress, and cost of the converter are all reduced. It enables transformerless operation for renewable energy environments, such as photovoltaic (PV) systems connected to a microgrid system, which optimizes power quality and improves reliability. In ref. [19], a single-phase 13-level switching-capacitor multilevel boost inverter (SCMLBI) with fewer switches and a voltage boost gain of six times is given. The primary objective of this research is to demonstate a single DC source SCMLBI topology, which, when coupled with an appropriate sinusoidal pulse modulation (SPWM) approach, is capable of producing an AC output voltage that has a low level of harmonic distortion.

The SCMLI given in refs. [20,21] requires more switching to generate five levels. This topology has a smaller part count, and a higherlevel output can be achieved by cascading upgraded HB modules. There is only one isolated DC power source employed. Although an asymmetrical design generates more levels than a symmetrical operating mode, the easily available DC sources of varying magnitudes remain a worry even though an asymmetrical configuration generates more levels. Therefore, single-phase topologies are being advocated, since they are capable of functioning in either arrangement. Ref. [22] outlines an asymmetrical structure, which has a lower source count than previous models. These single-phase topologies can also be run in three-phase mode. Compared with traditional topologies, the switch count and gate drive count of the three-phase hybrid cascaded modular multilevel inverter (HCMMLI), which is described in ref. [18], are both significantly decreased. In ref. [23], there is a presentation of a single DC source hybrid seven-level three-phase architecture, which uses a hybrid control technique to increase efficiency. Ref. [24] presents a proposal for a three-phase symmetrical architecture, which uses fewer components. An improved control approach for renewable energy resources in microgrids that are gridconnected via voltage-sourced converters (VSCs) is provided in refs. [25–28]. Ahigh-gain SC capacitor scheme with 13 stages is described in ref. [29]. One of the main problems with this design is that one capacitor is being utilized to charge another capacitor.

To address the aforementioned issues, this study offers a new three-phase MLI design, which possesses minimum switching components, reduced voltage stress, and the ability to step up the input voltage.

The assets of the proposed topology (PT) are as follows:

a. The topology has voltage boosting capability.
b. Capacitors are inherently self–balanced.
c. Reduced voltage stress across the switching components.
d. It requires only an isolated DC source for the generation of five-level (line-to-line) voltages.
e. The minimum number of switches is ensuredfor any level of generation.
f. It can be operated for a wide range of power factors.
g. The suggested topology provides a lower TSV value, lowering overall costs.

The following structure guides this paper. Section 2 discusses the specifics of the design, the underlying operating principle, and the recommended range of capacitance values. Section 3 discusses the modulation strategy of the proposed topology in detail. An evaluation of the power losses in the SC topology is presented in Section 4. Section 5 provides a comparative analysis with state-of-the-art topology to demonstrate its usefulness. Section 6 presents the results of the simulations and the experiments. Finally, Section 7 discusses the conclusion part of the proposed topology.

2. Proposed Single Source Three-Phase Topology

2.1. Explanation of the SCMLI Topology

The PT five-level 3-ϕ SCMLI is displayed in Figure 1. Each phase leg of this inverter possesses four power semiconductor switches, one capacitor, and one power diode. To prevent the supply voltage from being accidentally shorted out, the SC cell's switches operate in a complimentary manner. The supply voltage (V_{DC}) is common to all phases X ($X \in$ phase R, phase Y, phase B). The proposed topology synthesizes five levels of the line-to-line voltage (0, $\pm 1V_{DC} \pm 2V_{DC}$). All switches' voltage stresses are well below the supply voltage, except for S_{X4}, where it is twice as high. The simple switching pattern for various modes of activity for phase R is introduced in Table 1. Switches' on/off states are represented by the numbers 0 and 1.

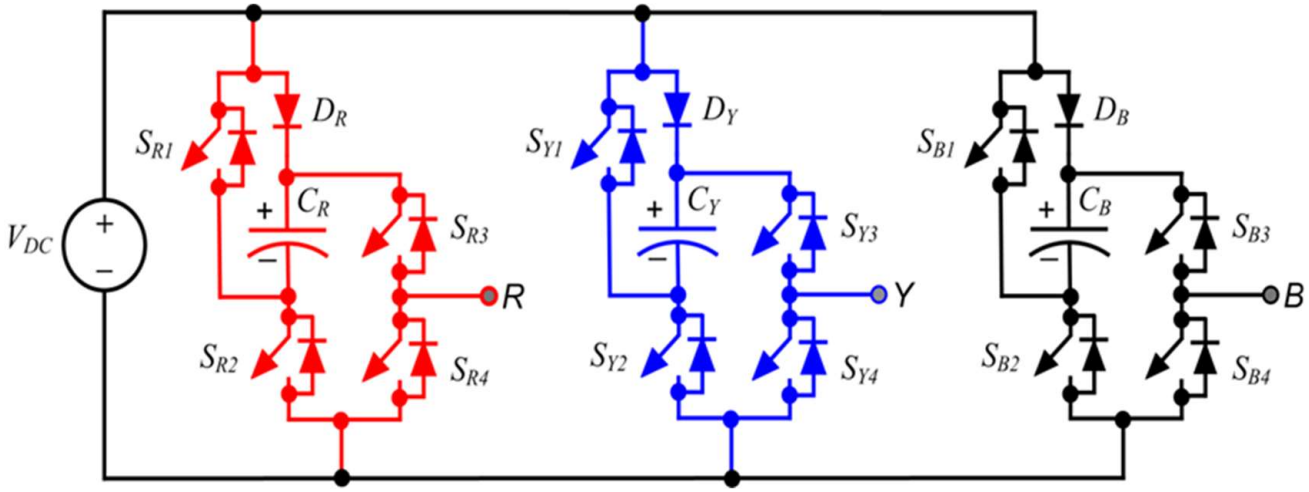


Figure 1. Proposed five level SCMLI topology.

Table 1. Different switching modes and their corresponding positive pole voltages for phase leg "R".

Switching Mode	Active Switch				Pole Voltage per Phase Leg $v_{Rn}(t)$
	S_{R1}	S_{R2}	S_{R3}	S_{R4}	
δ_1	0	1	0	1	0
δ_2	0	1	1	0	$+1V_{DC}$
δ_3	1	0	1	0	$+2V_{DC}$

2.2. Working Principle

The operating principle of the PT can be depicted with the assistance of per phase leg (say phase R), as shown in Figure 2. Since each phase leg of the PT is identical, the comparative analysis for the other two phases can be extended. As a result, the idea of using onlyone phase leg is considered to be more illuminating. The activity of the single-phase leg is clarified in the accompanying mode. In every mode of activity, the inverter synthesizes a specific voltage level with the assistance of the desired switching combination mentioned in Table 1. The sequence of the voltage generation path and charging path of the capacitor are set apart by dotted blue and green lines separately.

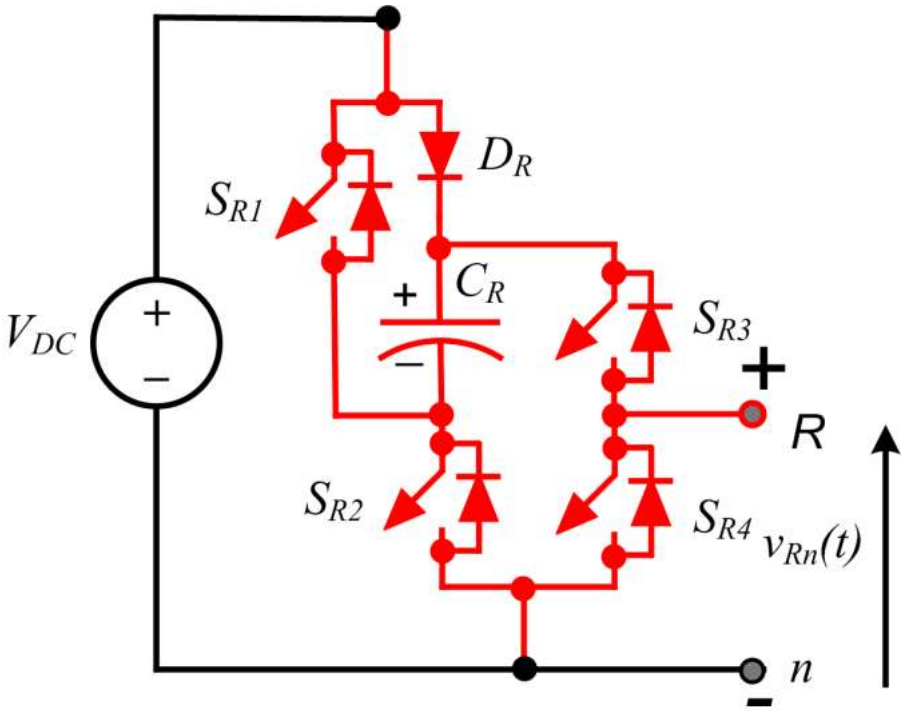


Figure 2. Circuit diagram for per phase leg R.

$$\text{Mode } \delta_1\text{: } v_{Rn}(t) = 0$$

In this mode of activity, the controlled switches S_{R2}, and S_{R4} are in on state, and S_{R1}, and S_{R3} are in off condition to accomplish zero volts across the load terminals. The capacitor (C_R) is energized to a voltage of magnitude V_{DC} through the forward-biased diode (D_R) because of the activation of switch S_{R2}. The leading way for pole voltage is shown in Figure 3a.

$$\text{Mode } \delta_2\text{: } v_{Rn}(t) = +1V_{DC}$$

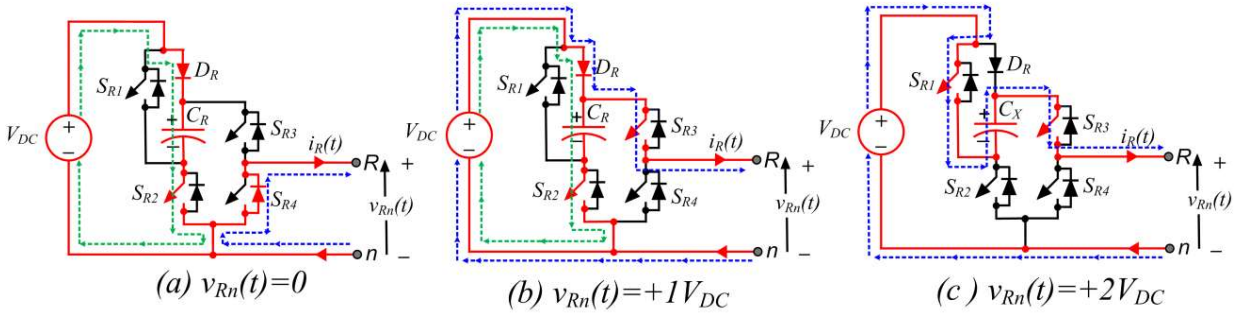


Figure 3. Different modes of operation of pole voltage generation. (**a**) $v_{Rn}(t) = 0$; (**b**) $v_{Rn}(t) = 1V_{DC}$; (**c**) $v_{Rn}(t) = 2V_{DC}$.

To achieve the targeted output voltage V_{DC}, this mode of operation simultaneously activates the switches S_{R2} and S_{R3} while simultaneously deactivating the switches S_{R4} and S_{R1}. Due to the activation of the switch S_{R2}, the capacitor is connected in shunt with the isolated dc voltage source and energized to a voltage of magnitude V_{DC}. The leading way for pole voltage is shown in Figure 3b.

$$\text{Mode } \delta_3\text{: } v_{Rn}(t) = +2V_{DC}$$

This voltage is achieved by simultaneously activating S_{R1} and S_{R3}, and deactivating S_{R2}, and S_{R4}. Due to the activation of the switch S_{R1}, the capacitor (C_R) is placed in cascade to the load through switch S_{R3} and releases its stored energy to the output. Hence, the output level becomes $2V_{DC}$. The leading way for pole voltage is shown in Figure 3c.

2.3. Capacitance Design and Self-Balancing

The capacitor (C_X) is used as a dc voltage source to provide the various output levels needed by the proposed SCMLI. Discharging to loads causes a decrease in their voltages.The capacitance of a capacitor typically decreases as the voltage ripple across it increases. Therefore, calculating the voltage ripple across the capacitor is the first task to complete in SC design. The voltage ripple can be computed as follows for a completely passive load, which represents the worstcase scenario because there is no load current flowing back to the capacitors [10].

$$\Delta V_{CR} = \frac{1}{\omega C_R} \int_{t_a}^{t_b} \frac{2V_{DC}}{R} dt \tag{1}$$

The capacitor design in an SCMLI is a significant factorto avoid undercharging and-voltage ripples. Consequently, the ideal estimation of capacitance is chosen in such a way, so as to fulfill the following condition [6]:

$$C_{optimum} \geq \frac{\Delta QC}{\Delta V_{CX}} \tag{2}$$

where ΔQ_C represents the amount of discharge from the capacitor, K is the percentage of extremely tolerable voltage ripple, and V_{DC} is the supply voltage.

The stability of the capacitor relies on the magnitude of the load current, power factor, and longest releasing period of the capacitor. Therefore, the maximum discharge amount of capacitors is obtained as: Therefore, the releasemeasure of charge (ΔQ_C) can be communicated as

$$\Delta Q_C \int_{t_a}^{t_b} I_{peak} sin(2\pi ft - \varphi) dt \tag{3}$$

where I_{peak} is the maximum current flowing through the load, f is the modulated wave frequency, and φ is the phase angle difference between voltage and current; The longest discharging times for each capacitor is ($t_a - t_b$).

This discharging period can be calculated from Figure 3b as follows [6]:

$$t_a = \frac{sin^{-1}\left(\frac{1}{2}\right)}{2\pi f} \tag{4}$$

$$t_b = \frac{\pi - sin^{-1}\left(\frac{1}{2}\right)}{2\pi f} \tag{5}$$

Taking into account the voltage ripple, the value of capacitance for C_{R1} is

$$C_R \geq \frac{\int_{t_a}^{t_b} I_{peak} sin(2\pi ft - \varphi) dt}{\Delta V_{CR}} \tag{6}$$

The other capacitors (C_Y and C_B) can be treated in the same way.

The capacitor C_R ischarged to V_{DC} during the voltage level of zero and $+1V_{DC}$ by activating the switch S_{R2} through the power diode D_R, as portrayed in Figure 3a,b. The capacitor delivers its stored energy to load at the voltage level $+2V_{DC}$ shown in Figure 3c. This charging and releasing of a sequence of capacitors over every cycle keep it self-balanced automatically.

3. Modulation Scheme

The level shift sinusoidal pulse width modulation (LS-SPWM) control strategy is executed. A continuous comparison is made between two carrier signals and a referencesignal $U(t)$ at 50 Hz with a modulation index of M = 0.95. Carrier signals above the zero reference axis are labeled $C_1(t)$, and those below it are labeled $C_2(t)$ for each phase leg X (t). As $U(t)$ becomes more significant than the carrier signal, it produces a "1" above the zero reference axis and a "0" below. Under the zero reference axis, a reading of "0" is obtained when the reference signal is more dominant than the carrier signal, while a reading of "−1" is obtained otherwise. All of the signals from the comparator are put together to form a single signal $a(t)$. With the help of the lock-up Table 1, next, compare this aggregated signal to the fixed levels in order to obtained the gate signals. Figure 4a depicts the circuit design for the switching scheme for phase leg "X", and Figure 4b shows the modulated signal, carrier signal, and output voltage.

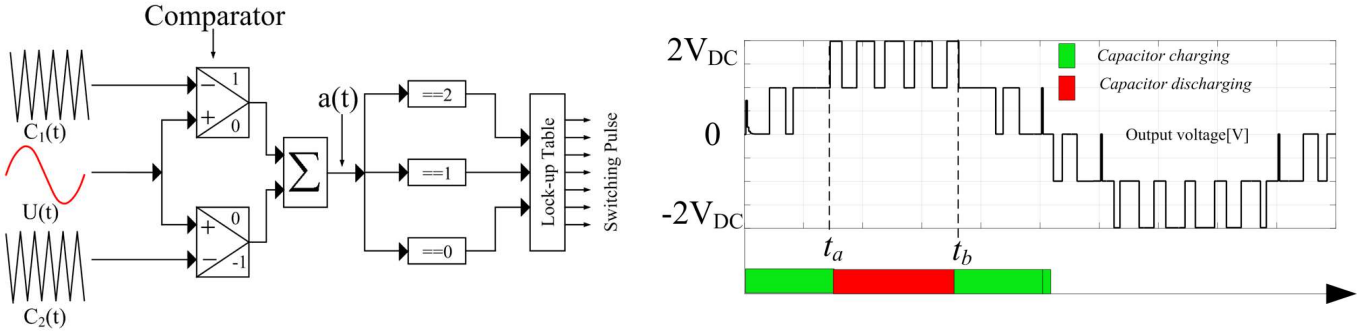


Figure 4. The proposed 3-ϕ five-level MLI. (**a**) Switching scheme for per phase leg; (**b**) Output voltage.

4. Loss Analysis

Different kinds of losses take place in the PT, such as (i) conduction losses, (ii) switching losses, (iii) blocking state or off-state losses, and (iv) voltage ripple losses. At any rate, the blocking state losses are very small because, during the off state of the switches, the leakage current is exceptionally little. Hence, it will be negligibled [9].

4.1. Conduction Losses

When the switching components are in the conduction path for conveying their particular voltage level, conduction losses arise owing to the ohmic losses associated with the dynamic resistance of the switch. Therefore, conduction losses appear due to the power switch (R_S) and diode (R_D) are expressed mathematically as follows [7]:

$$P_C = [P_{C,\,S} + P_{C,\,D}] \tag{7}$$

where conduction losses (P_C) due to semiconductor switches ($P_{C,sw}$) and power diodes ($P_{C,D}$) an be expressed as:

$$P_{C,\,sw} = V_S I_{S,avg} + I^2_{S,rms} R_S \tag{8}$$

$$P_{C,\,D} = V_D I_{D,avg} + I^2_{D,rms} R_D \tag{9}$$

where V_S,V_D are the conduction state voltage drops of the switch and diode respectively.

$I_{S,avg}$ = average current flowing through a switches.

R_S, R_D = on-state resistance of the switch and diode respectively.

$I_{S,rms}$, $I_{D,avg}$ = root-mean-square and average current through the switch and diode respectively.

4.2. Ripple Losses

The voltage gap between the supply voltage and the voltage across capacitors is defined as a voltage ripple. The capacitor voltage ripple is expressed as [10]

$$\Delta V_{C_x} = \frac{1}{C_x}\int_{t_a}^{t_b} I_{C_x}(t)dt \tag{10}$$

where $I_{C_x}(t)$ is theinstantaneous current passing through the capacitor.

t_a and t_b is the discharging period.

Thus, the ripple loss (P_{rip}) can bestatedas [9]

$$P_{rip} = \frac{f_{sw}}{2}\sum_{x=1}^{n} C_x \Delta V_{C_x}^2 \tag{11}$$

4.3. Switching Losses

Switching losses, caused by the overlapping of current and voltage during the switching state change, can be calculated [9,20]. During turn-on, the power loss is given by

$$P_{S,i,ton} = \frac{1}{6}(f_{sw} V_{sw,i} I_{on,\,i} t_{on}) \tag{12}$$

Similarly, the switching loss due to turn-off can be calculated as

$$P_{SW,i,toff} = \frac{1}{6}(f_{sw} V_{sw,i} I_{off,\,i} t_{off}) \tag{13}$$

where $I_{on,\,i}$ and $I_{off,\,i}$ signify the current flowing through the switches after the ith switch is turned on and before it is turned off, respectively. $f_{sw,}$ is the switching frequency, and V_{sw} is the reverse voltage across the switch.

Thus, the total switching losses (P_{sw}) ofthe PT are calculated as follows:

$$P_{sw} = \sum_{n=1}^{5}\sum_{i=1}^{12}\left(P_{sw,i,ton} + P_{sw,i,toff}\right) \tag{14}$$

As a result, the PT's overall losses are composed of conduction and switching losses, as well as voltage ripple losses.

$$P_{total\ loss} = P_c + P_{sw} + P_{rip} \tag{15}$$

The PT's overall efficiency can be calculated as follows:

$$\%\text{Efficiency}(\eta) = (P_{output}/P_{input}) \times 100 \tag{16}$$

$$\%\eta = \left(\frac{P_{output}}{P_{output} + P_{total\ loss}}\right) \times 100 \tag{17}$$

where P_{output} and P_{input} represent the power output and input of the proposed inverter, respectively.

5. Comparative Assessment with the Existing Topologies

This section includes a comparison study to emphasize the importance of PT. The PT is compared to various recently proposed inverter architectures in terms of the semiconductor switches, diodes, capacitors, gain, total voltage stress, and cost function, among other

things. Table 2 compares the PTto existing inverter topologies in terms of the single-phase leg. However, the components necessary to build a three-phase architecture are three times those required for a single-phase leg. The component count per level ($F_{C/L}$) can be mathematically written as

$$F_{C/L} = \frac{N_C + N_{Sw} + N_D + N_S + N_{dri}}{N_L} \tag{18}$$

where N_L, N_C, N_D, N_{Sw}, and N_S are the number of levels, capacitors, diodes, switches, and the number of isolated DC sources per phase, respectively. Additionally, the cost function will decide the overall cost of the PT. The weight factor (α) for the PT is set to one because the switching components and TSV are both valued equally.

Table 2. Comparative assessment for per phase leg with recent SCMLI topologies.

Topology	*A*	*B*	*C*	*D*	*E*	*F*	*H*	$F_{C/L}$	G	CF	Losses (W)	Efficiency
[5]	7	10	-	4	1	10	8	3.14	1.5	4.57	25.44	92.4%
[7]	7	6	2	1	1	8	6	2.28	3	3.28	23.48	95.45%
[8]	5	6	2	2	1	8		2.2	2	3.6	23.67	95.23%
[12]	7	10	-	3	1	9	10	3.28	1.5	4.57	24.68	94.45%
[13]	7	9	-	3	1	6.5	8	2.87	1.5	3.78	25.89	94.76%
[14]	7	9	-	3	1	8	8	2.85	1.5	4	22.24	95.48%
[15]	5	9	-	1	1	9	9	3.8	2	5.6	22.45	95.34%
[16]	5	6	2	3	1	6	6	3.4	1	4.6	18.69	96.23%
[18]	5	10	-	-	2	14	9	3.8	1	13.2	25.25	92.14%
[P]	5	4	1	1	1	6	4	2	2	3.2	14.21	96.7%
A : N_L, B : N_{SW}, C : N_D, D : N_C, E : N_S, F : TSV, G : Gain, H : N_{dri}												

The cost factor is defined by Equation (18) as

$$CF = \frac{[N_{SW} + N_C + N_D + N_{dri} + \alpha TSV] \times N_S}{N_L} \tag{19}$$

The PT has a smaller *CF* and $F_{C/L}$ than prior topologies. The proposed topology is compared with other existing topologies for TSV and in references [16,18] are better as compared to proposed topology and the proposed topology is better while comparing all other topologies in Table 2 for specific levels, i.e., five levels. Although topologies [7,8,22] share the same gain factor, they have a higher component count per level factor and cost function. As a result, PT employs the least number of components, resulting in a more compact inverter. As a result, the weight and energy consumption of the PTare decreased. Additionally, it lowers equipment costs by lowering the TSV and provides the lowest possible voltage and current THD performance. As a result, the proposed inverter beats its competitors in every way.In comparison to other existing topologies, the PT's overall efficiency is superior. Table 3 presents a cost comparison, which was evaluated to help further clarify the unique benefits of the proposed topology. All topologies were given the same voltage parameters for the sake of cost analysis. In addition, the cost analysis gave equal weight to all factors. The costs for alternative topologies are listed in Table 3, and the proposed topology is shown to have the lowest overall component costs.

Table 3. Cost analysis of the proposed topology compared with the existing topologies.

C	PN	R	UP	Topology							
				[7]	[5]	[12]	[13]	[14]	[16]	[18]	[P]
MOSFET *	IRFP240PBF	100 V, 23 A	2.2	-	6	6	6	6	-	-	-
	IRFP350PBF	200 V, 20 A	2.68	6	24	21	21	24	18	18	9
	IRFP21N60LPBF	400 V, 16 A	3.48	12	-	-		-	-	12	3
	IRFP9140NPBF	600 V, 21 A	8.16		-	-		-	-	-	-
Diode *	VS-20ETF02-M3	200 V, 20 A	3.68	3	-	-		-	6	-	3
Capacitor	23M252F200BH1H1	200 V, 2500 µF	23.61	6	12	9	9	9	9	-	3
Gate Driver	IR2110	-	1.8	18	27	24	24	27	18	27	12
Total Cost (USD)				240.6	409.4	325.6	325.6	338.6	315.2	138.6	138.03
C = Components, R = Rating, UP = Unit Price (USD), PN = Part Number											

* www.digikey.com, www.galco.com (accessed on 20 December 2022).

6. Simulated and Experimental Results

6.1. Simulated Results

To validate the theoretical notion, the PT's modeling and simulation results were taken using MATLAB/Simulink software. The modeling and experimental factors are enumerated in Table 4.

Table 4. Simulation and experimental results: Useful parameters.

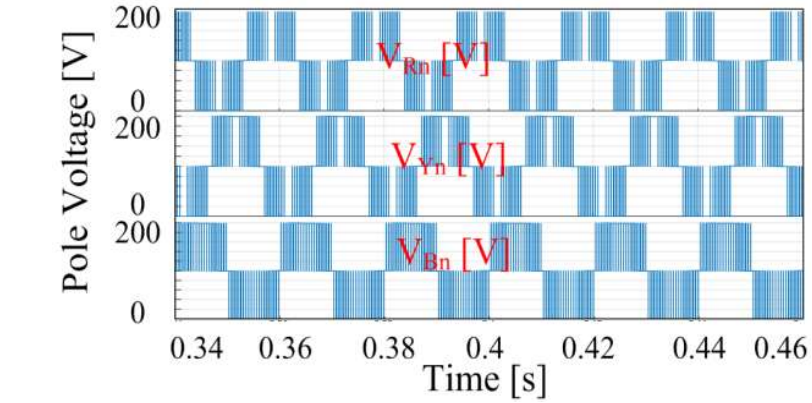
Parameter	Specification
Supply voltage (V_{DC})	100 V
Supply frequency	50 Hz
Carrier frequency	2 kHz
Capacitors ($C_R = C_Y = C_B$)	1100 µF
Load	R = 40 Ω, L = 30 mH
Switch	IRFP460 MOSFETs
Diodes	VS-20ETF02-M3
Controller	dSPACE DS1104
Modulation index	0.95

Figure 5 illustrates the time-varying outcomes of line voltages and pole voltages for a PT. The source configuration is held constant at Vdc = 100 V, while the modulation index is held at M = 0.95. Each phase leg's pole voltage output is depicted in Figure 5a. The maximum voltage at the poles is 200 V. Figure 5b–d show the line voltages V_{RY}, V_{YB}, V_{BR}, line current (I_R, I_Y, I_B), and the capacitors' voltages V_{CR}, V_{CY}, and V_{CB} when the load isvaried. This dynamic load current change is indicative of relatively stable load voltages. When the load current rises, the voltage ripples of the capacitors also grow.Figure 5d illustratesthat the capacitor voltage for phase R is self-balanced with small voltage ripples when the load varies suddenly. As can be seen in Figure 5d, the voltage across the capacitors tends to stabilize at its nominal value, V_{CX} = 100 V. This equilibrium is maintained in the presence of varying loads. As can be seen in Figure 5e, the blocking voltages for S_{R1}, S_{R2}, and S_{R3} are all 100 V DC. The stress voltages applied to S_{R4} should also total 200 V. Each leg switch has a stress voltage or blocking voltage of 500 V.

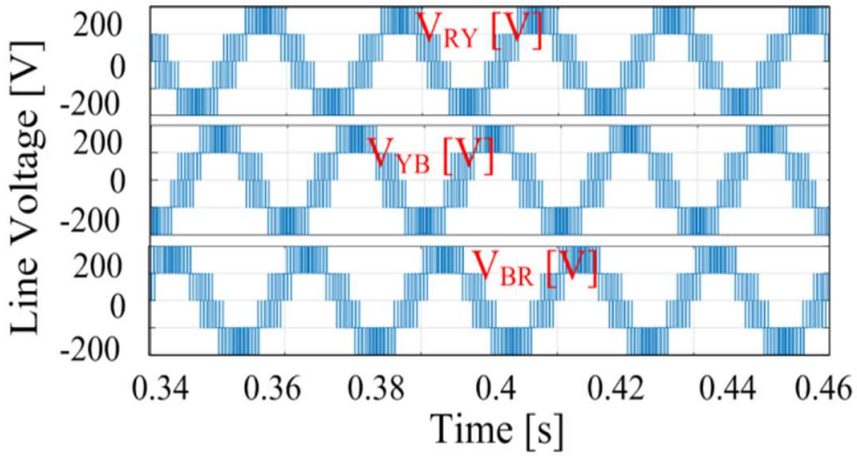
IRFP460 MOSFETs were utilizedas controlled switches on the PLECS SIMULINK platform, and the IRFP460 datasheet was brought in to quantify the power loss. This is seen in Figure 5f, which depicts the power loss distribution under full load.

6.2. Experimental Results

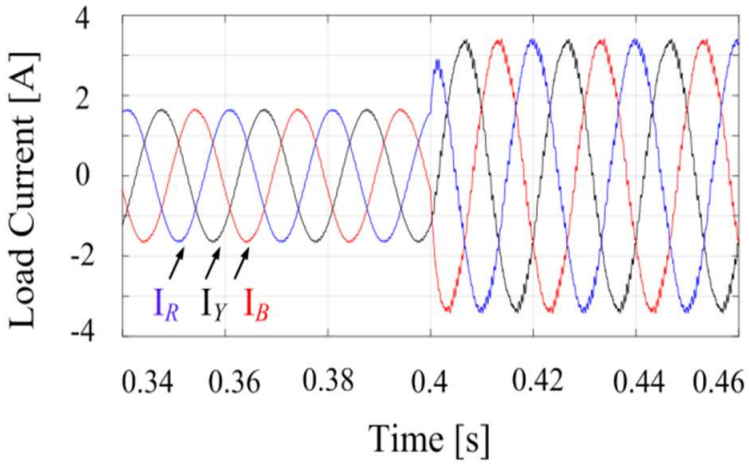
A prototype for hardware execution consists of twelve discrete power switches (IRFP460 MOSFETs and accompanying gate drivers circuit), three capacitors, three auxiliary power diodes, and one DC supply. The experimental configuration of the five-level prototype is depicted in Figure 6. Table 4, on the other hand, shows the components utilized to build the prototype. A controlled DC power supply is used as an isolated DC source for feeding a PT MLI topology. The experimental results are depicted in Figure 7.



(**a**)

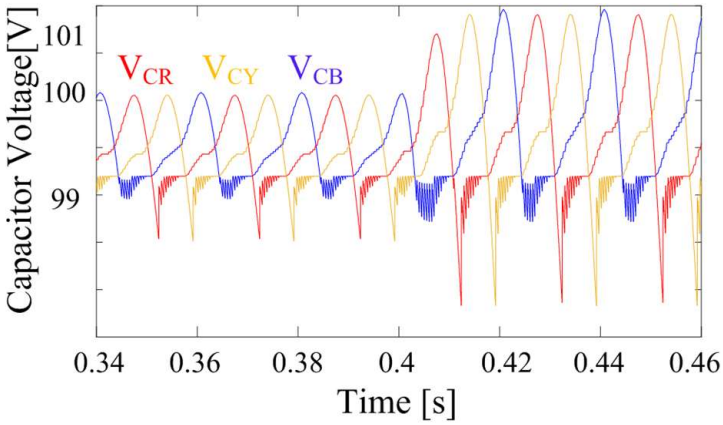


(**b**)

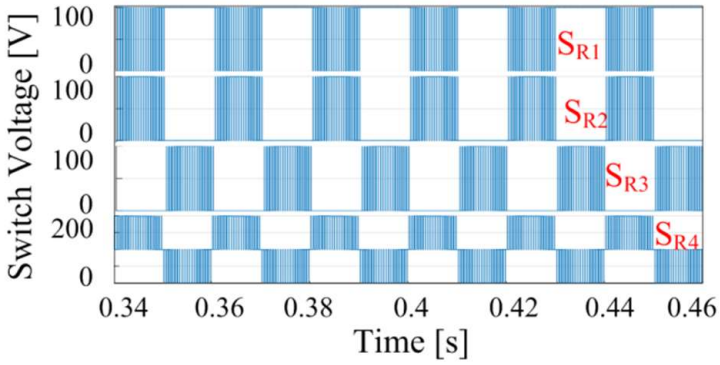


(**c**)

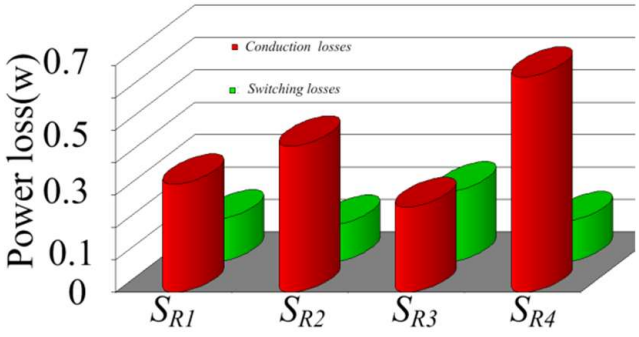
Figure 5. *Cont.*



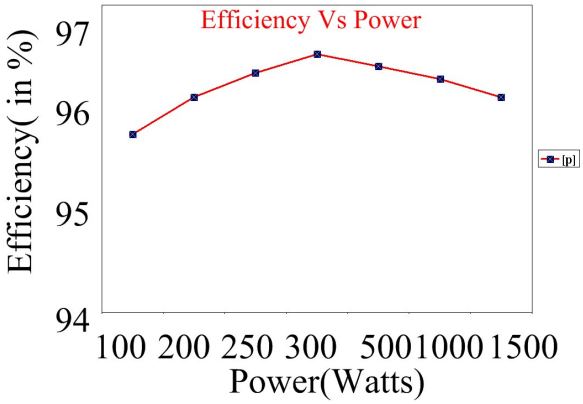
(**d**)



(**e**)



(**f**)



(**g**)

Figure 5. Simulated results. (**a**) Pole voltage; (**b**) Line voltage; (**c**) Line current; (**d**) Voltage across capacitors; (**e**) Voltage stress of switches; (**f**) Per phase distribution of power losses; (**g**) Power versus efficiency curve.

The results of the simulation and the experiment are comparable in a satisfactory manner. The voltages at the output poles are depicted in Figure 7a. There are three different levels of voltages at the pole. These levels are: +200 V, +100 V, and 0 V. Figure 7b shows the line voltages that were measured. It is clear to see that the generated line voltage is composed of five distinct levels. The voltages are as follows: –200 V, –100 V, 0 V, 100 V, and +200 V. The variation of the load current due to change in loading is demonstrated in Figure 7c. Figure 7c depicts the phase currents in their entirety. The maximum value that the phase current can reach upto 3.5 A. Figure 7d illustrates the voltages measured across the capacitors. The voltage magnitudes of the produced capacitors are as follows: V_{C1} = 100 V. Despite the sudden shift in load, the line voltage remained stable because the capacitors automatically balanced themselves. All the blocking voltages for S_{R1}, S_{R2}, and S_{R3} are at 100 V DC. Additionally, S_{R4} needs to be subjected to a total of 200 V in stress voltages. The blocking voltage of phase leg R is depicted in Figure 7e. Figure 7f shows the per-phase voltage and current under a steady state. It is worth noting that the experimental results closely match the simulated results. The efficiency at different powers andvoltages is shown in Figure 7g. The efficiency of the inverter is lowest at lower power values, rising to a maximum of around 300 W and then gradually falling back down again.

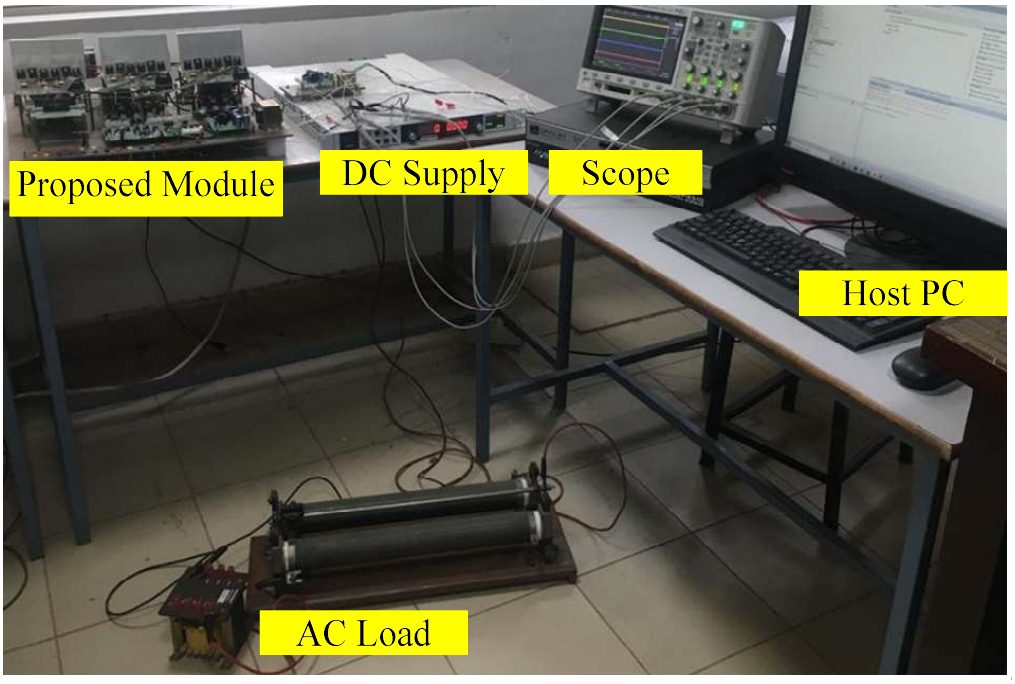
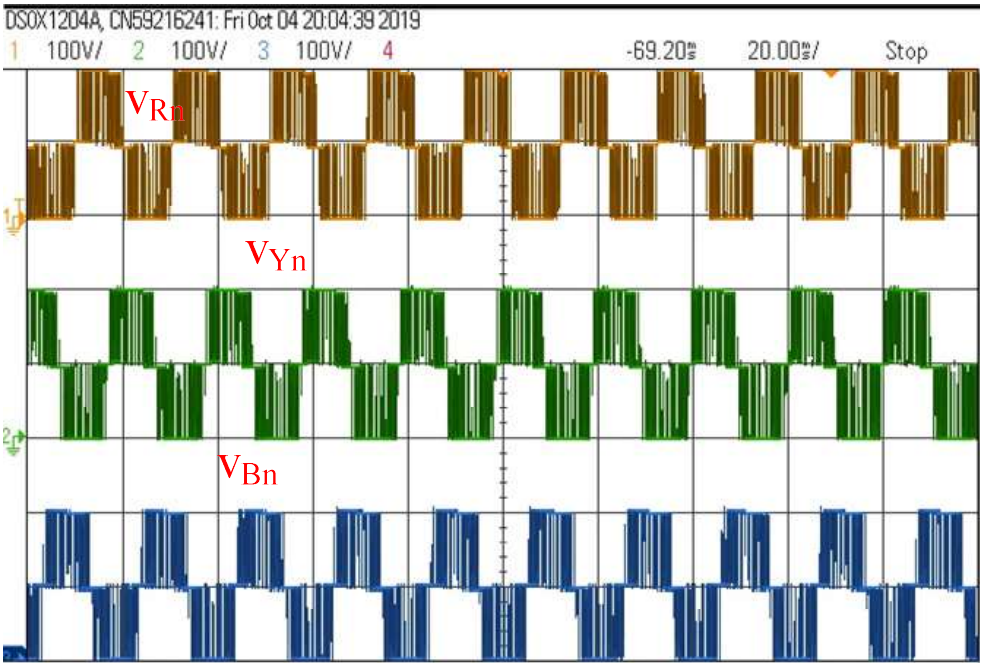
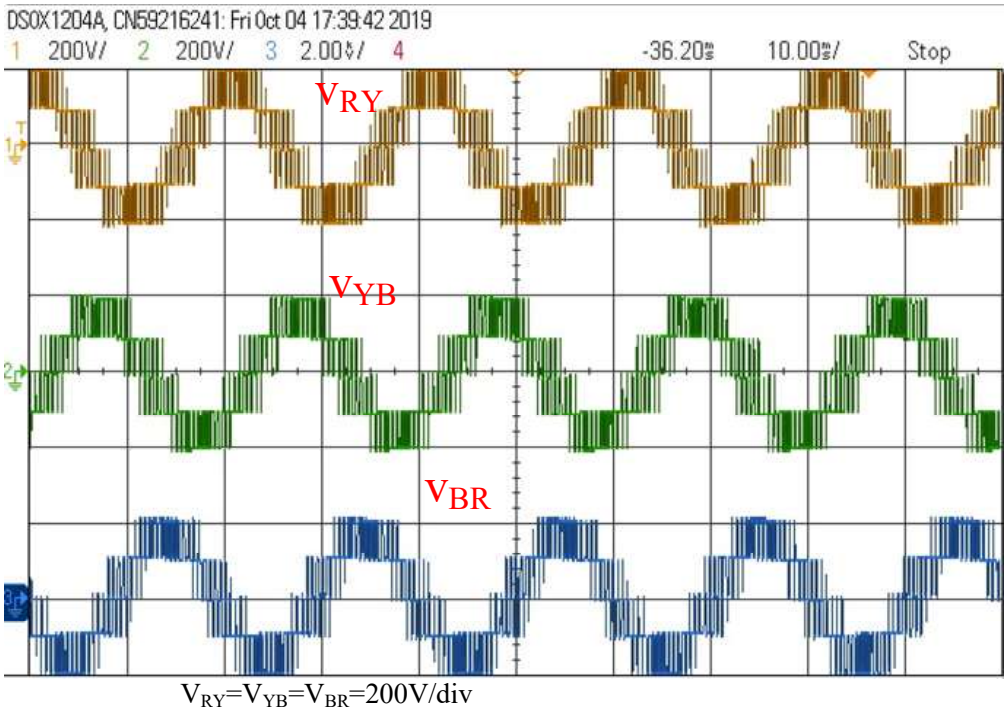


Figure 6. Experimental setup.



$V_{Rn}=V_{Yn}=V_{Bn}=100V/div$

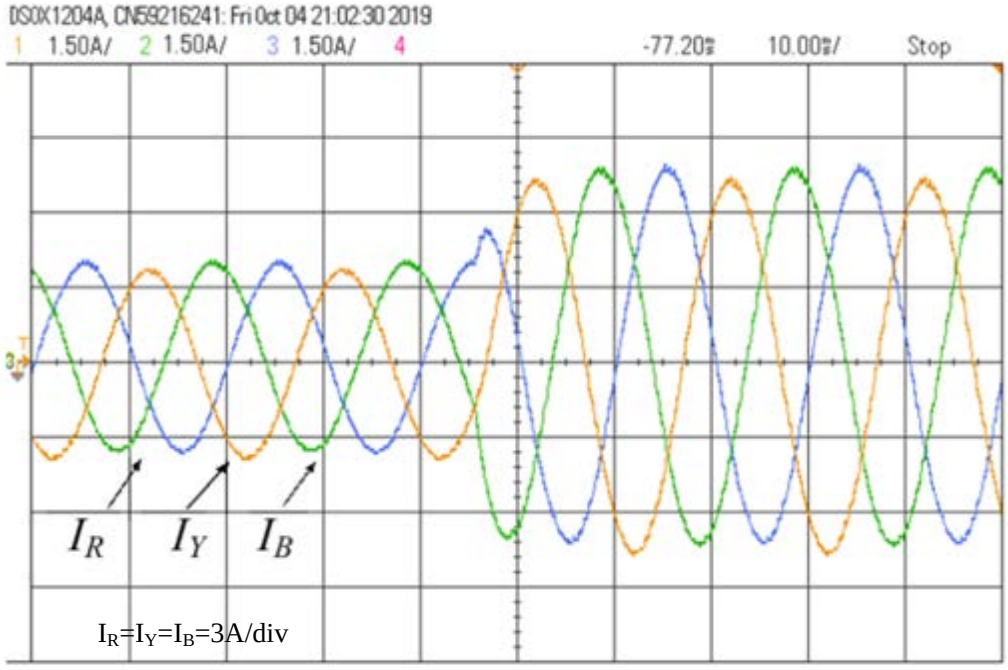
(**a**)



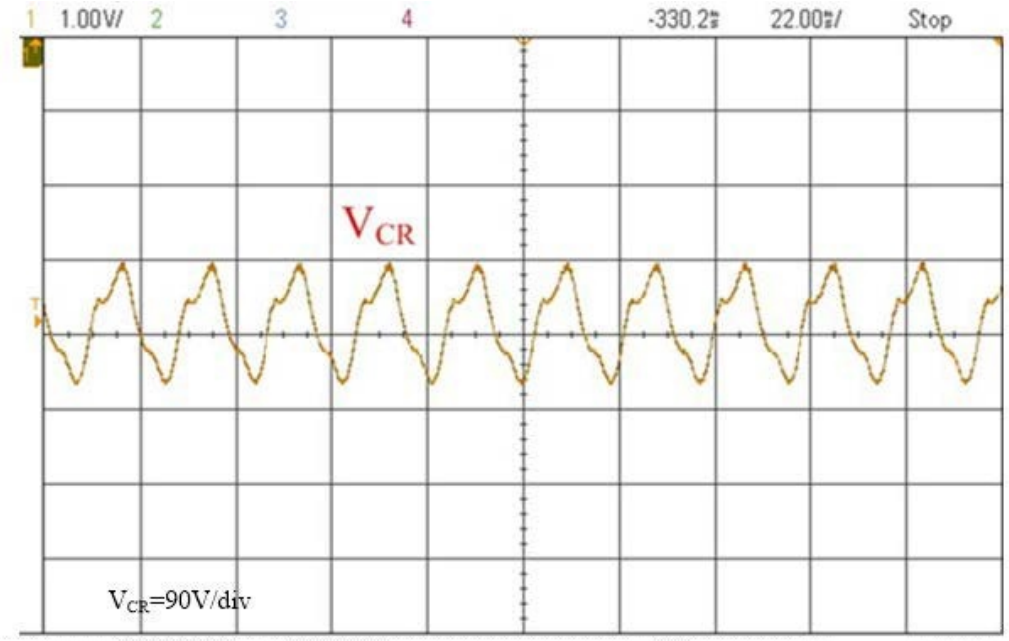
$V_{RY}=V_{YB}=V_{BR}=200V/div$

(**b**)

Figure 7. *Cont.*

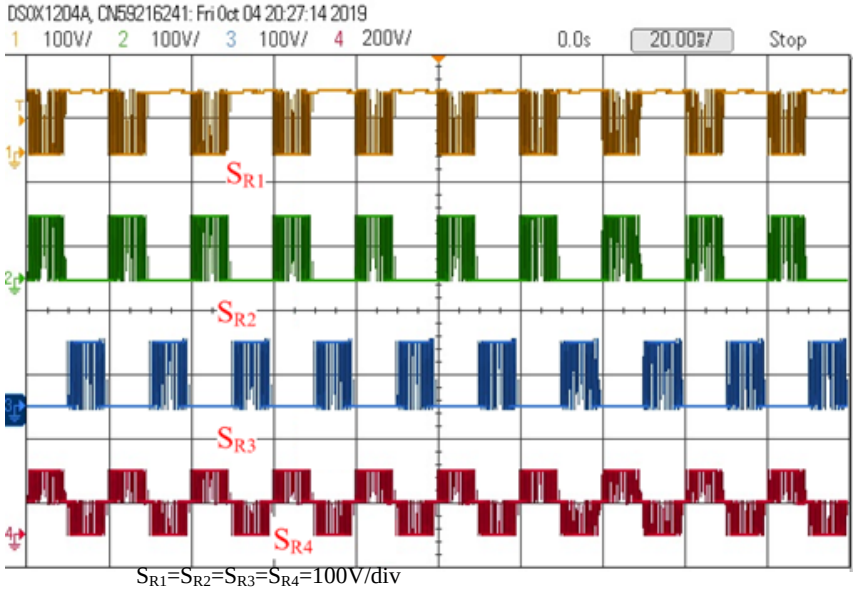


(**c**)

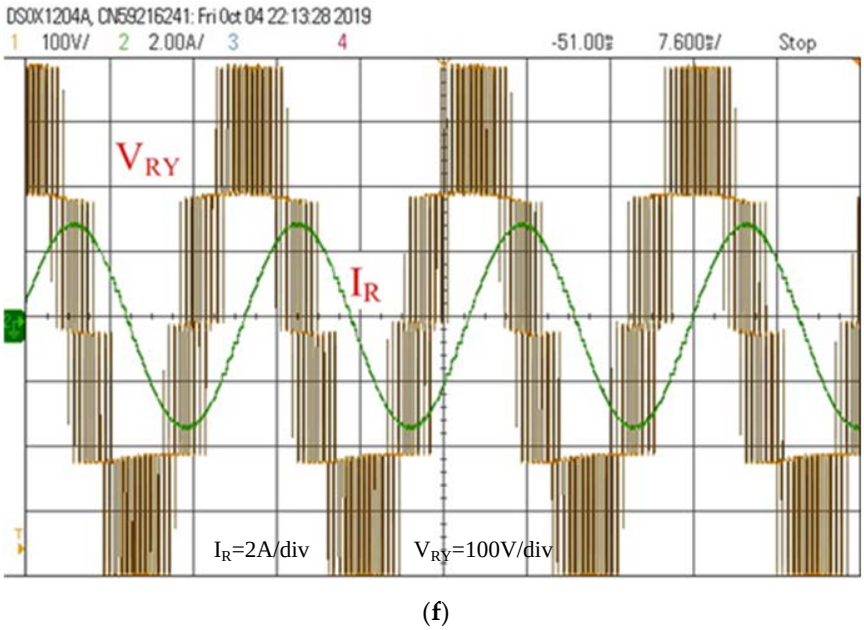


(**d**)

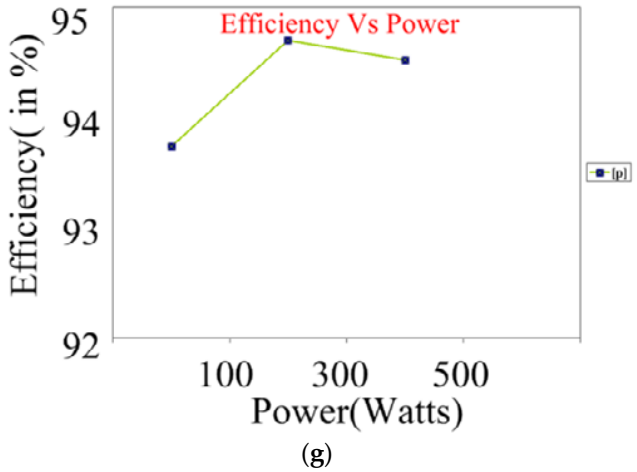
Figure 7. *Cont*.



(**e**)



(**f**)



(**g**)

Figure 7. Experimental results. (**a**) Pole voltage; (**b**) Line voltage; (**c**) Voltage ripple across the capacitors; (**d**) Line current; (**e**) Voltage across switches; (**f**) Current and voltage on phase R; (**g**) Power versus efficiency curve.

7. Conclusions

This article discusses the novel 3-SCMLI with explanatory notes. The proposed topology uses fewer switching components to achieve the three-phase system. The operation concept and modulation approach of the PT for a single-phase leg are demonstrated in detail, together with circuit schematics and waveforms. Compared to more traditional MLI topologies, the suggested architecture offers the lowest voltage stress across capacitors and switches. The number of sensors required and the complexity of the control system can be significantly reduced as a result of this self-balanced capacitor voltage. The suggested five-level SC-MLI topology is mathematically modeled, with loss and efficiency analysis. The profiles of pole voltage, line voltage, and output current under dynamic loading conditions are shown. The PT's performance is proven through simulated and experimental investigation for a variety of output voltages and capacitor counts. The suggested five-level SC-MLI topology is mathematically modeled, with loss and efficiency analysis, and it is determined that its efficiency is adequate.

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Nomenclature

δ_j	jth operating state
I_{peak}	Maximum current flowing through the load
φ	Phase angle difference between voltage and current
t_a	ath instant of time
N_L	Number of levels in multilevel waveform
N_{SW}	Number of power switches
N_D	Number of power diodes
N_{dri}	Number of gate driver units
N_S	Number of input dc sources
N_C	Number of capacitors
η	Efficiency
P_{output}	Output power
P_{input}	Input power
$P_{total\ loss}$	Total power losses
ΔV_{C_x}	Voltage ripple across capacitor
f_{ref}	Frequency of sinusoidal reference
$I_{C_x}(t)$	Instantaneous current through capacitor
V_{sw}	Blocking voltage of power switch
$I_{on,\,i}$	Current through ith power switch after the switch is turned on
t_{on}	Turn-on time of the power switch
t_{off}	Turn-off time of the power switch
f_{sw}	Switching frequency of the power switch

$I_{S,avg}$	Average current through power switch
R_s	On-state resistance of power switch
$I_{S,rms}$	The root-mean-square value of current through power switch
V_S	The on-state voltage of the power switch
V_D	The on-state voltage of the power diode
$I_{D,avg}$	Average current through power diode
R_D	On-state resistance of power diode
C_j	jth Frequency of carrier waveform
M	Modulation index

References

1. Abbott, D. Keeping the Energy Debate Clean: How Do We Supply the World's Energy Needs? *Proc. IEEE* **2010**, *98*, 42–66. [CrossRef]
2. Rodriguez, J.; Lai, S.; Peng, F.Z. Multilevel inverters: Asurvey of topologies, control, and applications. *IEEE Trans. Ind. Electron.* **2002**, *49*, 724–738. [CrossRef]
3. Gupta, K.K.; Ranjan, A.; Bhatnagar, P.; Sahu, L.K.; Jain, S. Multilevel Inverter Topologies With Reduced Device Count: A Review. *IEEE Trans. Power Electron.* **2016**, *31*, 135–151. [CrossRef]
4. Franquelo, L.G.; Rodriguez, J.; Leon, J.I.; Kouro, S.; Portillo, R.; Prats, M.A. The age of multilevel converters arrives. *IEEE Ind. Electron. Mag.* **2008**, *2*, 28–39. [CrossRef]
5. Lee, S.S.; Bak, S.Y.; Kim, A.; Joseph, M.; Lee, K.B. New Family of Boost Switched-Capacitor Seven-Level Inverters (BSC7LI). *IEEE Trans. Power Electron.* **2019**, *34*, 10471–10479. [CrossRef]
6. Taghvaie, A.; Adabi, J.; Rezanejad, M. A Self-Balanced Step-Up Multilevel Inverter Based on Switched-Capacitor Structure. *IEEE Trans. Ind. Electron.* **2018**, *33*, 199–209. [CrossRef]
7. Jena, K.; Panigrahi, C.K.; Gupta, K.K.; Kumar, D.; Dewangan, N.K. Generalized switched-capacitor multilevel inverter topology with self-balancing capacitors. *J. Power Electron.* **2022**, *22*, 1617–1626. [CrossRef]
8. Meysam, S.; Hosseini, M.; Adabi, J. A five-level step-up modulefor multilevel inverters: Topology, modulation strategy, and implementation. *IEEE J. Emerg. Andselec. Top. Power Electron.* **2018**, *6*, 2215–2226.
9. Babaei, E.; Gowgani, S.S. Hybrid Multilevel Inverter Using SwitchedCapacitor Units. *IEEE Trans. Ind.Electron.* **2014**, *61*, 4614–4621. [CrossRef]
10. Hinago, Y.; Koizumi, H. A SwitchedcapacitorInverter Using Series/Parallel Conversion WitInductiveLoad. *IEEE Trans. Ind. Electron.* **2012**, *59*, 878–887. [CrossRef]
11. Siwakoti, Y.P.; Mahajan, A.; Rogers, D.J.; Blaabjerg, F. A Novel Seven-Level Active Neutral-Point-Clamped Converter With Reduced Active Switching Devices and DC-Link Voltage. *IEEE Trans. Power Electron.* **2019**, *34*, 10492–10508. [CrossRef]
12. Sathik, M.J.; Sandeep, N.; Blaabjerg, F. High Gain Active Neutral Point Clamped Seven-Level Self-Voltage Balancing Inverter. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *67*, 2567–2571. [CrossRef]
13. Zeng, J.; Lin, W.; Liu, J. Switched-Capacitor-Based Active-Neutral-Point-Clamped Seven-Level Inverter With Natural Balance and Boost Ability. *IEEE Access* **2019**, *7*, 126889–126896. [CrossRef]
14. Lee, S.S.; Lim, C.S.; Siwakoti, Y.P.; Lee, K.-B. Hybrid 7-Level Boost Active-Neutral-Point- Clamped (H-7L-BANPC) Inverter. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *67*, 2044–2048. [CrossRef]
15. Sandeep, N.; Ali, J.S.M.; Yaragatti, U.R.; Vijayakumar, K. A Self-Balancing Five-Level Boosting Inverter With Reduced Components. *IEEE Trans. Power Electron.* **2019**, *34*, 6020–6024. [CrossRef]
16. Siwakoti, Y.P. A new six-switch five-level boost-active neutral point clamped (5L-Boost-ANPC) inverter. In Proceedings of the 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 4–8 March 2018; pp. 2424–2430. [CrossRef]
17. Mittal, A.; Janardhan, K.; Ojha, A. Multilevel inverter based Grid Connected Solar Photovoltaic System with Power Flow Control. In Proceedings of the 2021 International Conference on Sustainable Energy and Future Electric Transportation (SEFET), Hyderabad, India, 21–23 January 2021; pp. 1–6. [CrossRef]
18. Karasani, R.R.; Borghate, V.B.; Meshram, P.M.; Suryawanshi, H.M.; Sabyasachi, S. A Three-Phase Hybrid Cascaded Modular Multilevel Inverter for Renewable Energy Environment. *IEEE Trans. Power Electron.* **2017**, *32*, 1070–1087. [CrossRef]
19. Kumar, B.H.; Prabhu, S.; Janardhan, K.; Arun, V.; Vivekanandan, S. A Switched Capacitor-Based Multilevel Boost Inverter for Photovoltaic Applications. *J. Circuits Syst. Comput.* **2022**, *22*, 2350057. [CrossRef]
20. Kumar, B.H.; Lokhande, M.M. Investigation of switching sequences on a generalized SVPWM algorithm for multilevel inverters. *J. Circuits Syst. Comput.* **2019**, *28*, 1950036. [CrossRef]
21. Kumar, B.H.; Kadam, D.P.; Rajitha, S.; Sundaramoorthy, P.; Penchalaiah, T.; Janardhan, K. Modified Synchronous Reluctance Motor for Electric Vehicle Applications. *IJEER* **2022**, *10*, 926–931. [CrossRef]
22. Reddy, K.R.; Sabyasachi, S.; Meshram, P.; Borghate, V.B. An asymmetrical multilevel inverter topology with reduced source count. In Proceedings of the 2016 IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS), Bhopal, India, 5–6 March 2016; pp. 1–6. [CrossRef]

23. Jena, K.; Panigrahi, C.K.; Gupta, K.K. Three-phase triple-gain switched-capacitor inverter with reduced component count. *Electr. Eng.* **2022**, *104*, 3547–3559. [CrossRef]
24. Salem, A.; Ahmed, E.M.; Orabi, M.; Ahmed, M. New Three-Phase Symmetrical Multilevel Voltage Source Inverter. *IEEE J. Emerg. Sel. Top. Circuits Syst.* **2015**, *5*, 430–442. [CrossRef]
25. Dehghani, M.; Ghiasi, M.; Niknam, T.; Rouzbehi, K.; Wang, Z.; Siano, P.; Alhelou, H.H. Control of LPV Modeled AC-Microgrid Based on Mixed H 2/H∞ Time-Varying Linear State Feedback and Robust Predictive Algorithm. *IEEE Access* **2021**, *10*, 3738–3755. [CrossRef]
26. Dehghani, M.; Ghiasi, M.; Garpachi, M.G.; Niknam, T.; Kavousi-Fard, A.; Shirazi, H.H. Stabilization of DC/DC Converter with Constant Power Load using Exact Feedback Linearization Method based on Backstepping Sliding Mode Control and Nonlinear Disturbance Observer. In Proceedings of the 2021 12th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC), Tabriz, Iran, 2–4 February 2021; pp. 1–6.
27. Dehghani, M.; Niknam, T.; Ghiasi, M.; Baghaee, H.R.; Blaabjerg, F.; Dragicevǐć, T.; Rashidi, M. Adaptive backstepping control for master-slave AC microgrid in smart island. *Energy* **2022**, *246*, 123282. [CrossRef]
28. Ghiasi, M.; Niknam, T.; Dehghani, M.; Baghaee, H.R.; Wang, Z.; Ghanbarian, M.M.; Blaabjerg, F.; Dragicevic, T. Multipurpose FCS Model Predictive Control of VSC-Based Microgrids for Islanded and Grid-Connected Operation Modes. *IEEE Syst. J.* **2022**. [CrossRef]
29. Jena, K.; Panigrahi, C.K.; Gupta, K.K. A new design self-balanced 13-level switched-capacitor inverter. *Int. J. Circuit Theory Appl.* **2022**, *50*, 1216–1234. [CrossRef]