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A Novel Unbalance Compensation Method for Distribution Solid-State Transformer Based on Reduced Order Generalized Integrator

ZHENGWEI QU[1], YUNXIAO YAO[1,2], YUNJING WANG[1], CHUNJIANG ZHANG[1], ZHENXIAO CHONG[1], AND AHMED ABU-SIADA[3], (Senior Member, IEEE)

[1]Key Laboratory of Power Electronics for Energy Conservation and Drive Control, Yanshan University, Qinhuangdao 066004, China
[2]State Grid Hubei DC Operation and Maintenance Company, Yichang 443008, China
[3]School of Electrical Engineering Computing and Mathematical Sciences, Curtin University, Perth, WA 6102, Australia

Corresponding author: Zhengwei Qu (ysu_qzw@163.com)

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ABSTRACT Owing to its modular construction, ability for bi-directional power flow and suitability for AC/DC grids, solid-state transformer (SST) is expected to be the backbone of the future smart grids. One of the main drawbacks of SST is the generation of negative-sequence current component at its input stage under unbalanced distribution system which causes adverse impacts on the power quality of the electricity grids. This paper is aimed at proposing a novel unbalance compensation method based on reduced order generalized integrator to suppress the negative-sequence current. Unlike the conventional sequence compensation method that is based on dual synchronous reference frames, the new proposed method does not involve complex calculation of the command current and sequence decomposition. As such, the response speed of the compensation controller is significantly improved. Additionally, the proposed method is easy to implement when compared with the current conventional compensation technique as there is no need to inject sequence components into the grid. A simulation model of three-module cascaded SST with three-phase star connection is established in Matlab/Simulink. Several case studies are carried out under different operating conditions. Simulation results validate the feasibility of the proposed method.

INDEX TERMS Solid-state transformer, negative-sequence current suppression, reduced order generalized integrator, three-phase unbalance compensation.

I. INTRODUCTION

Solid-state transformer (SST) is commonly regarded as a prototype of energy router, which is expected to have broad applications in the future smart power grids [1], [2]. Unlike conventional power frequency magnetic transformer, SST is a combination of power electronic converters and medium- or high-frequency transformer, which can facilitate bi-directional power flow and is suitable for AC/DC grids [3]. Moreover, besides the advantage of its reduced size and weight, SST features several additional functionalities including fault isolation and harmonic suppression [4].

In recent years, the application of SST in distribution systems has gained increasing attention. The implementation of an SST with a simple two-level or three-level converter into the distribution systems is not cost effective due to the high rated voltage of the required power devices [5]. As such, adopting cascaded stages or multilevel converters of cost-effective low-voltage power electronic devices has been investigated in the literature [6]. Additionally, high-voltage power devices based on wide bandgap materials such as silicon carbide (SiC) IGBT that is capable of handling high voltage up to 25 kV are under development and soon they will be available for practical application [7]. Furthermore, combination of modular topologies and high-voltage power devices can acquire even higher voltage levels.

From topological point of view, the two most widely used SST structures are the single-phase SST topology based on cascaded H-bridge rectifiers [8] and the three-phase SST topology based on modular multilevel converters (MMC) [9].

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The main difference of these two topologies is that the former adopts cascaded H-bridge rectifiers while the latter employs MMCs as the input stage. Compared with MMC-SST, the cascaded SST exhibits higher power density, employs simpler control scheme and possesses better economic indicators under the same requirements of insulation and heat dissipation [10]. Therefore, the cascaded topology is selected as the research object in this paper.

Previous studies on SST have focused on aspects such as circuit topology, power control, high-frequency transformer design, utilization of wide bandgap power devices and SST applications [11]–[14]. However, no much attention was paid to the control strategy of SST under unbalanced operating conditions. Unbalanced operating state of power distribution systems often arises due to power system faults or asymmetric loads. If an SST is employed in the power grid without unbalance compensation, negative-sequence current will be generated and injected to the grid. Simultaneously, the negative-sequence current will also lead to unbalanced voltage across the DC capacitor in each phase of the SST, which affects the performance of the SST and may damage its power electronic devices. Therefore, it is necessary to adopt a reliable and cost-effective compensation method for SST operating under three-phase unbalanced condition.

The unbalance compensation of SST can be implemented through developing suitable topology design or by adopting an improved control strategy. However, topology design method will increase the complexity of the circuit and raise the cost [15], [16]. In comparison, compensation method by improved control strategy is more practical and cost-effective.

Currently, a common compensation method based on zero-sequence voltage injection is widely adopted [17], [18]. This method requires the calculation of the zero-sequence compensation voltage based on the deviation of the high voltage direct-current (HVDC) capacitor voltage. Hence, a pure sinusoidal compensation voltage cannot be achieved which results in a poor power quality. The narrow compensation range of this method is another disadvantage. Another compensation method based on the combination of zero- and negative-sequence components injection is proposed in [19]. The basic principle of this method can be briefly interpreted as follows: zero-sequence component is used under light unbalanced condition whereas negative-sequence component is used under severe condition. This method significantly expands the compensation range of SST under unbalanced load condition. However, the switching point of zero- and negative-sequence components injection should be identified precisely. Also, the injection of negative-sequence component will pollute the distribution system.

For grid-connected inverters, a sequence decomposition and compensation control strategy is presented in [20]. Positive- and negative-sequence current are controlled under dual synchronous reference frames and both are regulated by proportional integral (PI) controller. Although the method can effectively suppress negative-sequence current, the control system is complex, and the time delay caused by sequence decomposition is inevitable. To eliminate the time delay, an improved compensation method based on reduced order generalized integrator (ROGI) is proposed in [21]. This method can acquire decent power quality under unbalanced grid voltage, but still requires complicated command current calculation according to the different control objectives.

To fill this research gap, this paper proposes a novel compensation method for SST. The proposed technique avoides the sequence decomposition and reference current calculation, and thus improves the dynamic response speed of the compensation controller. The proposed control strategy is realized by an auxiliary ROGI controller based on current PI closed-loop control method. Adopting this method, the positive- and negative-sequence currents can be controlled simultaneously, which significantly reduces the complexity of the control scheme.

The rest of the paper is organized as follows. Section II interprets the basic principle of the proposed method. Section III presents the unbalanced control scheme for cascaded SST. Section IV analyzes the unbalance compensation ability of the proposed method. Section V presents the simulation results and discussion. Section VI concludes the paper.

II. UNBALANCE COMPENSATION PRINCIPLE

A. TOPOLOGY AND MATHEMATICAL MODEL

A typical cascaded SST topology shown in Fig. 1 consists of three parts: input stage, isolation stage, and output stage.

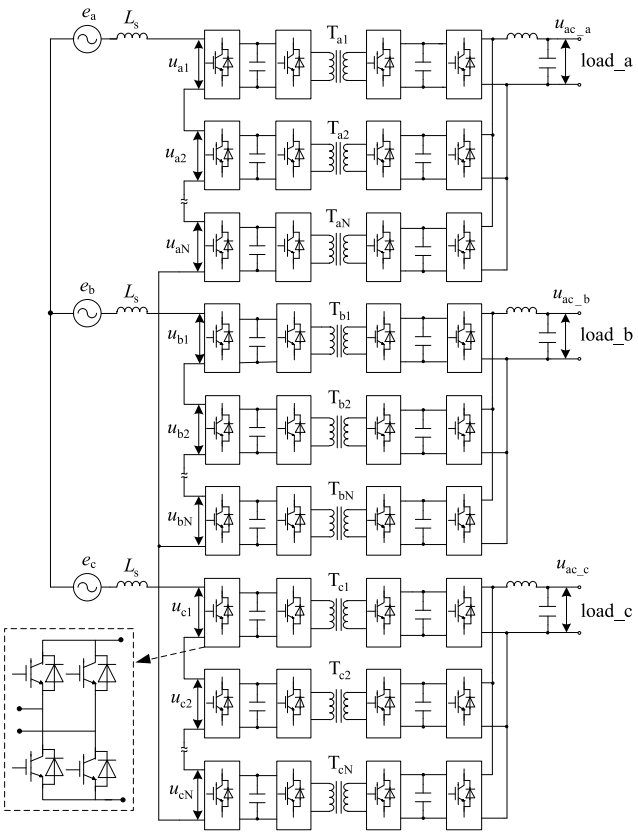

FIGURE 1. A typical three-phase cascaded SST topology.

The input stage includes three star-connected single-phase cascaded H-bridge rectifiers which are controlled by carrier phase-shift modulation. The isolation stage is a plurality of independent dual active bridge (DAB) converters. Each phase of the output stage consists of three voltage source inverters (VSI), and the output terminals of the VSIs are connected in parallel to improve the power rating of SST. The output stage can provide low-voltage alternating-current (LVAC) interfaces for connection with three-phase AC loads.

As shown in Figure 1, there is no neutral line between the power source and load. Therefore, there is no zero-sequence current in the system.

When the grid voltage and three-phase load power are unbalanced, the grid voltage can be expressed as:

$$\begin{cases} e_{\mathrm{a}} = E_{\mathrm{p}}\cos\ (\omega t+\varphi_{\mathrm{p}}) + E_{\mathrm{n}}\cos\ (\omega t+\varphi_{\mathrm{n}}) \\ +E_{\mathrm{z}}\cos\ (\omega t+\varphi_{\mathrm{z}}) \\ e_{\mathrm{b}} = E_{\mathrm{p}}\cos\ (\omega t+\varphi_{\mathrm{p}}-\dfrac{2\pi}{3}) + E_{\mathrm{n}}\cos\ (\omega t+\varphi_{\mathrm{n}}+\dfrac{2\pi}{3}) \\ +E_{\mathrm{z}}\cos\ (\omega t+\varphi_{\mathrm{z}}) \\ e_{\mathrm{c}} = E_{\mathrm{p}}\cos\ (\omega t+\varphi_{\mathrm{p}}+\dfrac{2\pi}{3}) + E_{\mathrm{n}}\cos\ (\omega t+\varphi_{\mathrm{n}}-\dfrac{2\pi}{3}) \\ +E_{\mathrm{z}}\cos\ (\omega t+\varphi_{\mathrm{z}}) \end{cases} \tag{1}$$

where e_{a}, e_{b}, e_{c} are the three phase grid voltages; E_{p}, E_{n}, E_{z} are the amplitudes of the positive-, negative- and zero-sequence components of the grid voltage; φ_{p}, φ_{n}, φ_{z} are the phase angles of the positive-, negative- and zero-sequence components; ω is the angular frequency of the grid.

Under unbalanced condition, the grid current is composed of positive- and negative-sequence components, which can be expressed as:

$$\begin{cases} i_{\mathrm{a}} = I_{\mathrm{p}}\cos\ (\omega t+\theta_{\mathrm{p}}) + I_{\mathrm{n}}\cos\ (\omega t+\theta_{\mathrm{n}}) \\ i_{\mathrm{b}} = I_{\mathrm{p}}\cos\ (\omega t+\theta_{\mathrm{p}}-\dfrac{2\pi}{3}) + I_{\mathrm{n}}\cos\ (\omega t+\theta_{\mathrm{n}}+\dfrac{2\pi}{3}) \\ i_{\mathrm{c}} = I_{\mathrm{p}}\cos\ (\omega t+\theta_{\mathrm{p}}+\dfrac{2\pi}{3}) + I_{\mathrm{n}}\cos\ (\omega t+\theta_{\mathrm{n}}-\dfrac{2\pi}{3}) \end{cases} \tag{2}$$

where $i_{\mathrm{a}}, i_{\mathrm{b}}$, i_{c} are the three-phase grid currents; I_{p}, I_{n} are the amplitude of the positive- and negative-sequence currents; θ_{p}, θ_{n} are the initial phase angles of the positive- and negative-sequence currents.

The input current of the cascaded H-bridge rectifiers can be expressed as:

$$\begin{bmatrix} e_{\mathrm{a}} \\ e_{\mathrm{b}} \\ e_{\mathrm{c}} \end{bmatrix} - \begin{bmatrix} u_{\mathrm{a}} \\ u_{\mathrm{b}} \\ u_{\mathrm{c}} \end{bmatrix} = L_{\mathrm{s}}\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{a}} \\ i_{b} \\ i_{\mathrm{c}} \end{bmatrix} + \begin{bmatrix} R_{\mathrm{a}}i_{\mathrm{a}} \\ R_{\mathrm{b}}i_{\mathrm{b}} \\ R_{\mathrm{c}}i_{\mathrm{c}} \end{bmatrix} \tag{3}$$

where L_{s} is the filter inductance at the grid side; R_{a}, R_{b}, R_{c} represent the equivalent resistances of the input stage. Normally, they are very small and can be neglected.

Applying the *dq*transformation on (3) along with neglecting the resistors, the equation in *dq* coordinate is derived as follows:

$$\begin{bmatrix} e_{\mathrm{d}} \\ e_{\mathrm{q}} \end{bmatrix} - \begin{bmatrix} u_{\mathrm{id}} \\ u_{\mathrm{iq}} \end{bmatrix} = \begin{bmatrix} L_{\mathrm{s}}\dfrac{\mathrm{d}}{\mathrm{d}t} & -\omega L_{\mathrm{s}} \\ \omega L_{\mathrm{s}} & L_{\mathrm{s}}\dfrac{\mathrm{d}}{\mathrm{d}t} \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{d}} \\ i_{\mathrm{q}} \end{bmatrix} \tag{4}$$

where e_{d} and e_{q} are the d- and q-axis components of the grid voltage; u_{id} and u_{iq} are the d- and q-axis components of the converter ac-side voltage; and i_{d} and i_{q} are the d- and q-axis components of input current.

After decoupling control, the active and reactive current controllers can be expressed as:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{d}} \\ i_{q} \end{bmatrix} = \frac{1}{L_{\mathrm{s}}}\cdot\begin{bmatrix} K_{\mathrm{P}}\ (i_{\mathrm{d}}^{*}-i_{\mathrm{d}})\ K_{\mathrm{I}}\int (i_{\mathrm{d}}^{*}-i_{\mathrm{d}})\mathrm{d}t \\ K_{\mathrm{P}}\ (i_{\mathrm{q}}^{*}-i_{\mathrm{q}})\ K_{\mathrm{I}}\int (i_{\mathrm{q}}^{*}-i_{\mathrm{q}})\mathrm{d}t \end{bmatrix} \tag{5}$$

where K_{P} is the proportional gain; K_{I} is the integral gain; i_{d}^{*} and i_{q}^{*} are the d- and q-axis components of command current.

When the system is unbalanced, the negative-sequence component of the grid current will be composed of double frequency component in dq coordinate, and the active and reactive currents can be expressed as:

$$\begin{bmatrix} i_{\mathrm{d}} \\ i_{\mathrm{q}} \end{bmatrix} = \begin{bmatrix} i_{1\mathrm{d}} \\ i_{1\mathrm{q}} \end{bmatrix} + \begin{bmatrix} I_{2\mathrm{d}}\cdot e^{\mathrm{j}(-2\omega_1 t+\varphi_0)} \\ I_{2\mathrm{q}}\cdot e^{\mathrm{j}(-2\omega_1 t+\varphi_0)} \end{bmatrix} \tag{6}$$

where $i_{1\mathrm{d}}$ and $i_{1\mathrm{q}}$ are the DC components of the active and reactive currents; $I_{2\mathrm{d}}$ and $I_{2\mathrm{q}}$ are the amplitudes of the active and reactive parts of the negative-sequence double frequency component; and φ_0 is the initial phase angle of the negative-sequence component.

It is not feasible to achieve non-error adjustment of the negative-sequence double frequency component only by the PI controller. Therefore, a compensation method based on ROGI controller is proposed to suppress the negative-sequence current.

B. UNBALANCE COMPENSATION PRINCIPLE

The ROGI controller is obtained by reducing the order of the second order generalized integrator (SOGI) [21]. SOGI can only achieve frequency selection, but ROGI is able to distinguish the polarities of frequencies. The transfer functions of SOGI and ROGI are given in (7) and (8) respectively.

$$G_{\mathrm{SOGI}}(s) = \frac{2k_{\mathrm{r}}s}{s^2+\omega_{\mathrm{r}}^2} = \frac{k_{\mathrm{r}}}{s+\mathrm{j}\omega_{\mathrm{r}}} + \frac{k_{\mathrm{r}}}{s-\mathrm{j}\omega_{\mathrm{r}}} \tag{7}$$

$$G_{\mathrm{ROGI}}(s) = \frac{k_{\mathrm{r}}}{s+\mathrm{j}\omega_{\mathrm{r}}} \tag{8}$$

where k_r represents the integral gain, and ω_r represents the resonant angular frequency.

SOGI can be regarded as a combination of two ROGIs with positive- and negative-polarities of resonant frequencies. SOGI has two conjugate poles of $\pm\,\mathrm{j}\omega_{\mathrm{r}}$, whereas ROGI has only one pole of $-\mathrm{j}\omega_{\mathrm{r}}$. The magnitude-frequency characteristic curves of the two integrators are shown in Fig. 2 and Fig. 3, respectively.

It can be seen from Fig. 2 and Fig. 3 that SOGI has infinite gains at $\pm$100Hz, whereas ROGI has an infinite gain at only $-$100Hz. The gains of the two integrators at other frequencies

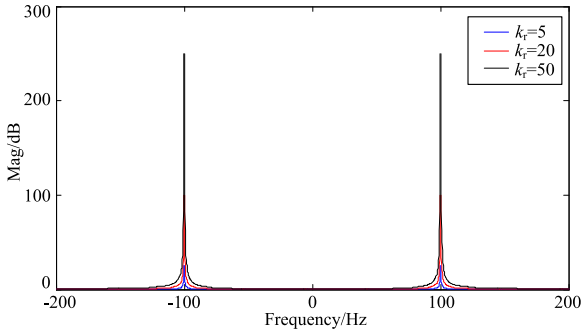

FIGURE 2. Magnitude-frequency characteristic of SOGI.

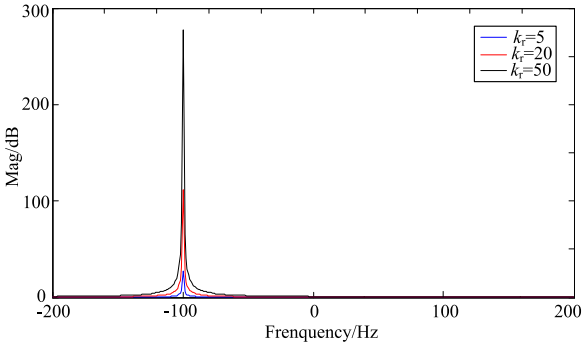

FIGURE 3. Magnitude-frequency characteristic of ROGI.

are almost zero. Therefore, ROGI can be used to regulate the negative-sequence double frequency component without influencing the positive-sequence component.

The output voltage of ROGI can be expressed as:

$$\begin{aligned}\begin{bmatrix} U_{\mathrm{d}}^{\mathrm{com}} \\ U_{\mathrm{q}}^{\mathrm{com}} \end{bmatrix} &= \mathscr{L}^{-1} G_{ROGI}\ (s) * \begin{bmatrix} i_d^* - i_d \\ i_q^* - i_q \end{bmatrix} \\ &= -\frac{k_{\mathrm{r}}}{\mathrm{j}2\omega_1}(1 - e^{-\mathrm{j}2\omega_1 t}) \cdot \begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} \\ &\quad -k_{\mathrm{r}} \begin{bmatrix} I_{2d} t \cdot e^{\mathrm{j}(-2\omega_1 t + \varphi_0)} \\ I_{2q} t \cdot e^{\mathrm{j}(-2\omega_1 t + \varphi_0)} \end{bmatrix} \end{aligned} \tag{9}$$

where $U_{\mathrm{d}}^{\mathrm{com}}$ and $U_{\mathrm{q}}^{\mathrm{com}}$ represent the output compensation voltages of the controller; $\mathscr{L}^{-1}$ represents the inverse Laplace transform; and $*$ represents the convolution operator.

The exponential function in the second term of (9) will increase rapidly with the time and its value will be much larger than the first term. Then (9) can be simplified as below.

$$\begin{bmatrix} U_{\mathrm{d}}^{\mathrm{com}} \\ U_{\mathrm{q}}^{\mathrm{com}} \end{bmatrix} = -k_{\mathrm{r}} \begin{bmatrix} I_{2\mathrm{d}} t \cdot e^{\mathrm{j}(-2\omega_1 t + \varphi_0)} \\ I_{2\mathrm{q}} t \cdot e^{\mathrm{j}(-2\omega_1 t + \varphi_0)} \end{bmatrix} \tag{10}$$

After positive-sequence decoupling control and negative-sequence current suppression, the command voltages of the input stage in dq coordinate can be expressed as:

$$\begin{bmatrix} U_{\mathrm{d}}^* \\ U_{\mathrm{q}}^* \end{bmatrix} = \begin{bmatrix} E_{\mathrm{d}} \\ E_{\mathrm{q}} \end{bmatrix} - \begin{bmatrix} U_{\mathrm{d}}^{\mathrm{PI}} \\ U_{\mathrm{q}}^{\mathrm{PI}} \end{bmatrix} - k_{\mathrm{r}} \begin{bmatrix} I_{2\mathrm{d}} \cdot e^{\mathrm{j}(-2\omega_1 t + \varphi_0)} \\ I_{2\mathrm{q}} \cdot e^{\mathrm{j}(-2\omega_1 t + \varphi_0)} \end{bmatrix} \tag{11}$$

where U_{d}^* and U_{q}^* are the d- and q-axis command voltages of the input stage; $U_{\mathrm{d}}^{\mathrm{PI}}$ and $U_{\mathrm{q}}^{\mathrm{PI}}$ are the d- and q-axis output voltages of the PI controller;

It can be seen from (11) that the command voltages of the input stage are only composed of the fundamental positive- and negative-sequence components. The positive-sequence component is used to control the power flow of SST, and the negative-sequence component is utilized to suppress the negative-sequence grid current.

In distribution systems, the grid frequency is allowed to have a fluctuation range of $-2.5\sim +1.5$Hz [22]. If used without any frequency margin, the robustness of ROGI will get poor as the grid frequency fluctuates. Therefore, it is necessary to introduce a cutoff frequency to increase the gain bandwidth range of the controller. Then the ROGI becomes a reduced order quasi-resonant (ROQR) integrator with a transfer function expressed as:

$$G_{\mathrm{ROQR}}\ (s) = \frac{k_{\mathrm{r}}\omega_{\mathrm{c}}}{s + \mathrm{j}\omega_{\mathrm{r}} + \omega_{\mathrm{c}}} \tag{12}$$

where ω_{c} is the cutoff angular frequency (usually $5\sim15$ rad/s).

The closed-loop transfer function of the ROQR integrator is expressed as

$$G_{\mathrm{close\_ROQR}}\ (s) = \frac{2k_{\mathrm{r}}\omega_{\mathrm{c}}}{(R + sL_{\mathrm{s}})(s + \mathrm{j}\omega_{\mathrm{r}} + \omega_{\mathrm{c}}) + 2k_{\mathrm{r}}\omega_{\mathrm{c}}} \tag{13}$$

where R represents the equivalent resistance of the input stage's switching loss and is usually neglected.

By substituting $s = \mathrm{j}\omega$ into (13) and omitting the resistance R, the transfer function can be derived as

$$G_{\mathrm{close\_ROQR}}\ (s) = \frac{\frac{2k_{\mathrm{r}}\omega_{\mathrm{c}}}{2k_{\mathrm{r}}\omega_{\mathrm{c}} - \omega^2 L_{\mathrm{s}} - \omega\omega_{\mathrm{r}}L_{\mathrm{s}}}}{1 + \mathrm{j}\frac{\omega\omega_{\mathrm{c}}L_{\mathrm{s}}}{2k_{\mathrm{r}}\omega_{\mathrm{c}} - \omega^2 L_{\mathrm{s}} - \omega\omega_{\mathrm{r}}L_{\mathrm{s}}}} \tag{14}$$

Setting $\left|\frac{\omega\omega_{\mathrm{c}}L_{\mathrm{s}}}{2k_{\mathrm{r}}\omega_{\mathrm{c}} - \omega^2 L_{\mathrm{s}} - \omega\omega_{\mathrm{r}}L_{\mathrm{s}}}\right| = 1$, the gain bandwidth (BW) of the ROQR integrator can be obtained as

$$\mathrm{BW} = \frac{2k_{\mathrm{r}}\omega_{\mathrm{c}} - \omega^2 L_{\mathrm{s}} - \omega\omega_{\mathrm{r}}L_{\mathrm{s}}}{2\pi L_{\mathrm{s}}} \tag{15}$$

If the BW is too small, the controller will lack robustness to adapt to the grid frequency fluctuation and the response speed will be slow. On the other hand, if the BW is too large, the frequency distinction of the controller will be poor, which will affect the control precision. Therefore, the BW should be set in a reasonable range, i.e., $f_{\mathrm{min}} \leq \mathrm{BW} \leq f_{\mathrm{max}}$. In order to ensure the robustness of the controller to adapt to the grid frequency fluctuation, f_{min} should not be less than the maximum fluctuation range of the grid frequency. In general, the fluctuation of the grid frequency is usually within ±1.5 Hz, so f_{min} is set at 1.5 Hz. In order to ensure the frequency distinction of the controller, f_{max} should not be too large, usually set at 30 Hz. Therefore, the range of the control parameter (k_{r}) can be derived as

$$\frac{2\pi L_{\mathrm{s}} f_{\mathrm{min}} + \omega\ (\omega + \omega_{\mathrm{r}})L_{\mathrm{s}}}{2\omega_{\mathrm{c}}} \leq k_{\mathrm{r}} \leq \frac{2\pi L_{\mathrm{s}} f_{\mathrm{max}} + \omega\ (\omega + \omega_{\mathrm{r}})L_{\mathrm{s}}}{2\omega_{\mathrm{c}}} \tag{16}$$

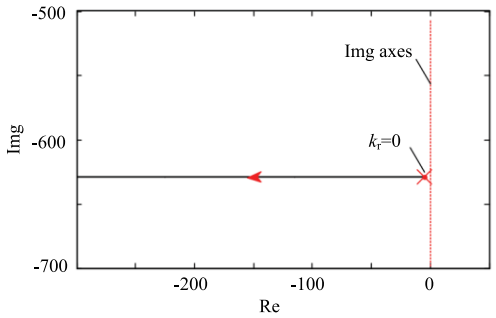

FIGURE 4. Root locus diagram of the control system based on ROQR.

Since k_r is closely related to the response speed, frequency selectivity and robustness, its design should comprehensively consider the above requirements.

The corresponding root locus diagram of the control system based on ROQR is shown in Fig. 4. It can be seen that when $k_r > 0$, the root trajectory of the system is always on the left side of the imaginary axis, i.e., all closed-loop poles of the system have negative real parts. It denotes that the control system is always stable as long as k_r is designed in the range given by (16).

III. CONTROL SCHEME FOR CASCADED SST

When the three-phase load is unbalanced, the three-phase power flow is also uneven, which will result in a negative-sequence component in the grid current. A compensation method in [23] utilizes a three-phase four-leg inverter at the output stage, but this method increases the complexity of the topology and control scheme, and exhibits a poor compensation ability for unbalanced grid voltage. Whereas the control strategy proposed in this paper can not only be fit in the condition of unbalanced grid voltage and asymmetric loads, but also provides decent power quality of AC and DC outputs. The control schemes of SST are elaborated below.

A. CONTROL SCHEME OF INPUT STAGE

For the input stage of SST, there are three control objectives: I) maintain the total HVDC voltage and realize the power factor correction; II) achieve voltage equalization between the sub-modules of each phase; III) suppress the negative-sequence grid current. To achieve the above control objectives, the input stage control block diagram proposed in this paper is shown in Fig. 5.

The control scheme of the input stage consists of three parts: decoupled control of positive-sequence current, negative-sequence current suppression and phase internal balancing control. The decoupled control of the positive-sequence current component is aimed to acquire stable average HVDC voltage and unity power factor. A notch filter with a frequency of 100Hz is utilized to extract the positive-sequence current in the d- and q-axis. The negative-sequence current suppression is achieved by embedding a ROGI controller in the positive-sequence synchronous reference frame

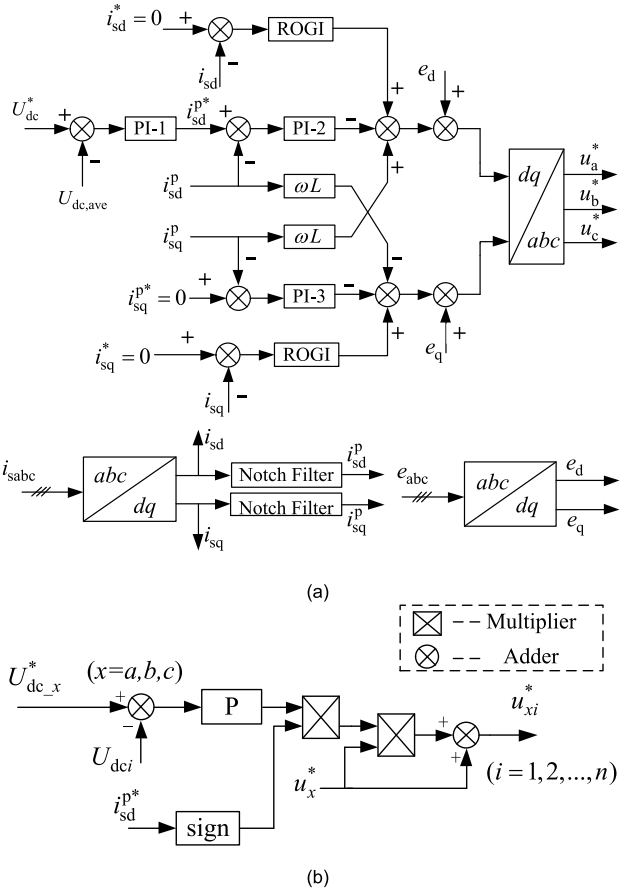

FIGURE 5. Proposed control scheme of the SST input stage. (a) Decoupled control of positive-sequence current and negative-sequence current suppression. (b) Phase internal balancing control.

based on current decoupled control. Phase internal balancing control is responsible for reducing the effects of switching devices power losses and achieving balanced HVDC voltage among each sub-module.

B. CONTROL SCHEME OF ISOLATION STAGE

The control objectives of the DAB converters in the isolation stage are to keep the voltage of the low voltage direct-current (LVDC) capacitors constant and realize bidirectional power flow. The voltage closed-loop PI controller is utilized to maintain the voltage of the LVDC capacitors, and the single-phase-shift pulse width modulation (PWM) is exploited to implement the bidirectional power flow by controlling the phase shift angle between the primary and secondary sides of each DAB converter. The proposed control scheme of the isolation stage is shown in Fig. 6 in which each DAB converter is controlled independently.

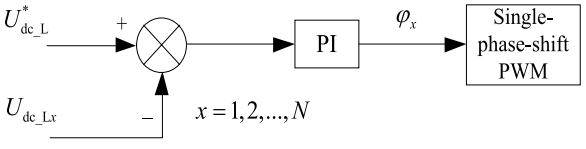

FIGURE 6. Control scheme of the isolation stage.

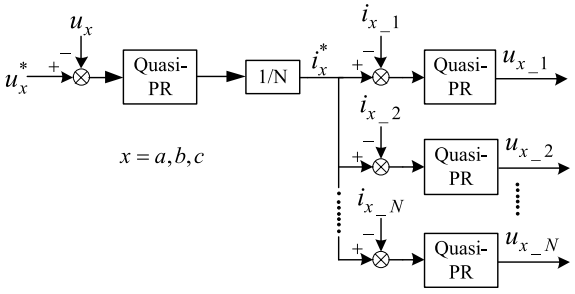

FIGURE 7. Control scheme of the output stage.

C. CONTROL SCHEME OF OUTPUT STAGE

The control objectives of the VSIs in the output stage are to provide constant output voltage and balanced current among the parallel VSIs. The proposed control scheme of one phase in the output stage is shown in Fig. 7; the control schemes of the other two phases are exactly the same. In the proposed controller, the outer voltage loop regulates the output voltage and generates the current reference, while the inner current loop tracks the same current reference to achieve current balancing control among the parallel VSIs. Quasi-proportional resonant (PR) controllers are employed in the output stage for its better performance in tracking AC signals. Since the output voltage of each parallel VSI in one phase is identical, the power of each VSI can be controlled by regulating the current.

IV. ICOMPENSATION ABILITY ANALYSIS

According to the national standard in China, the voltage fluctuation at the point of common coupling in distribution systems should be less than 2%∼4% [24]. Simultaneously, there are lots of asymmetric loads in distribution systems, and the unbalance factor of loads may be more severe than the grid voltage fluctuation. Therefore, the compensation ability of the proposed control scheme for three-phase unbalanced loads is emphatically analyzed in this section.

With the unbalance compensation, the three-phase grid current is controlled and balanced. However, the voltage of the HVDC capacitors will drift from their command value due to the unbalanced load. If the unbalance factor is severely high, it may result in distortion and potentially damaging power devices by overvoltage. Hence, the stability margin of the input stage is determined by the voltage of the HVDC capacitors. In other words, the SST can't operate stably unless the voltage of each HVDC capacitor does not exceed the maximum allowable value.

As the phase internal balancing controller is adopted, the HVDC voltage of sub-modules in each phase is already balanced. Therefore, the power devices will not be damaged by the overvoltage as long as the average voltage of the HVDC capacitors in each phase does not exceed the maximum permissible value.

For simplicity, this paper assumes that the power loss among different phases and sub-modules are the same and can be neglected. Therefore, the output power of each phase is expressed as follows:

$$\begin{cases} U_{\mathrm{dc\_a}} I_{\mathrm{dc\_a}} \approx P_{\mathrm{a}} \\ U_{\mathrm{dc\_b}} I_{\mathrm{dc\_b}} \approx P_{\mathrm{b}} \\ U_{\mathrm{dc\_c}} I_{\mathrm{dc\_c}} \approx P_{\mathrm{c}} \end{cases} \tag{17}$$

where $U_{\mathrm{dc\_a}}$, $U_{\mathrm{dc\_b}}$, $U_{\mathrm{dc\_c}}$ are the average voltages of the-HVDC capacitors of each phase; $I_{\mathrm{dc\_a}}$, $I_{\mathrm{dc\_b}}$, $I_{\mathrm{dc\_c}}$ are the rated root-mean-square values of the three-phase grid currents.

Once the grid current is balanced, i.e., $I_{\mathrm{dc\_a}} = I_{\mathrm{dc\_b}} = I_{\mathrm{dc\_c}} = I_{\mathrm{dc}}$, the output power of each phase is proportional to the average HVDC capacitor voltage of each phase. Suppose that the three-phase output power is expressed as follows:

$$\begin{cases} P_{\mathrm{a}} = k_{\mathrm{a}} \cdot P_{\mathrm{LN}} \\ P_{\mathrm{b}} = k_{\mathrm{b}} \cdot P_{\mathrm{LN}} \\ P_{\mathrm{c}} = k_{\mathrm{c}} \cdot P_{\mathrm{LN}} \end{cases} \quad (k_{\mathrm{a}} > k_{\mathrm{b}} > k_{\mathrm{c}} \geq 0) \tag{18}$$

where P_{LN} is the rated load power.

The unbalance factor of the three-phase load power is calculated as:

$$\Delta P\% = \frac{P_{\max} - P_{\min}}{P_{\mathrm{ave}}} = \frac{3(k_{\mathrm{a}} - k_{\mathrm{c}})}{k_{\mathrm{a}} + k_{\mathrm{b}} + k_{\mathrm{c}}} \times 100\% \tag{19}$$

where $P_{\max}$ is the maximum load power among the three phases and P_{ave} is the average load power of the three-phases.

To ensure that the average HVDC capacitor voltage of each phase does not exceed the maximum permissible value (U_{lim}), the limitation equation of the output power is derived as follows:

$$\frac{\max\ (P_{\mathrm{a}}, P_{\mathrm{b}}, P_{\mathrm{c}})}{I_{\mathrm{dc}}} = \frac{k_{\mathrm{a}} \cdot P_{\mathrm{LN}}}{I_{\mathrm{dc}}} \leq U_{\mathrm{lim}} \tag{20}$$

Substituting (18) and (19) into (20), the limitation equation of the unbalance factor among the three-phase load is derived as follows:

$$\Delta P\% \leq \frac{3(U_{\mathrm{lim}} \cdot I_{\mathrm{dc}} - k_{\mathrm{c}} \cdot P_{\mathrm{LN}})}{(k_{\mathrm{b}} + k_{\mathrm{c}}) \cdot P_{\mathrm{LN}} + U_{\mathrm{lim}} \cdot I_{\mathrm{dc}}} \tag{21}$$

Only the control objectives of the input stage are considered when analyzing the compensation ability of the SST in most literatures. However, the control of the isolation stage and input stage are not completely decoupled. When the HVDC capacitors voltage is too low, the corresponding LVDC capacitors voltage will be also too low to track the command voltage. Therefore, the voltage of the HVDC capacitors after unbalance compensation should not be less than a pre-defined minimum voltage that can maintain the LVDC capacitors voltage constant.

The relationship between the output power, input and output voltage and phase-shift angle of DAB converters is derived in [25], as given below:

$$P_{\mathrm{o}} = \frac{n U_{\mathrm{dc\_H}} U_{\mathrm{dc\_L}} \varphi\ (\pi - \varphi)}{2\pi^2 f_{\mathrm{s}} L_{\mathrm{k}}} \left(-\frac{\pi}{2} < \varphi < \frac{\pi}{2}\right) \tag{22}$$

where n is the ratio of the high-frequency transformer; φ is the phase-shift angle of the DAB converters; f_{s} is the switching

TABLE 1. Simulation parameters of cascaded SST circuit.

Parameter	Value
Rated capacity/MVA	2
Grid line voltage/kV	10
HVDC capacitor voltage/kV	4
LVDC capacitor voltage/kV	0.75
LVAC output voltage/kV	0.22
Grid side filter inductance/mH	18
HVDC capacitor/μF	5100
Ratio of HFT	40:9
Operating frequency of HFT/kHz	10
Rated load power/kW	500

frequency of the isolation stage and L_k is the leakage inductance of the high-frequency transformer.

Ignoring the power losses of the VSIs, the output power of the DAB converters in each phase will be equal to the rated load power, i.e.:

$$N \cdot P_o = P_{LN} = U_{dc\_L}^2 \Big/ R_L \tag{23}$$

where N is the number of cascaded modules; R_L represents the equivalent resistance of the load.

Substituting (22) into (23), the relationship of the input and output voltages of the DAB converters can be derived as:

$$U_{dc\_H} = U_{dc\_L} \cdot \frac{2\pi^2 f_s L_k}{n\varphi\,(\pi - \varphi)\,NR_L} \tag{24}$$

One of the control objectives of the isolation stage is to maintain the LVDC capacitors voltage constant. When φ is equal to 0.5, the voltage of the LVDC capacitors reaches a minimum value. The limitation equation of the output power at this condition is derived as follows:

$$\frac{\min\ (P_a, P_b, P_c)}{I_{dc}} = \frac{k_c \cdot P_{LN}}{I_{dc}} \geq U_{min} \tag{25}$$

where U_{min} is the minimum allowable value of the voltage of the LVDC capacitors.

Substituting (18) and (24) into (25), the limitation equation of the three-phase unbalance factor is derived as follows:

$$\Delta P\% \leq \frac{3(k_a - f_s L_k I_{dc})}{(k_a + k_b) \cdot nNU_{dc\_L} + f_s L_k I_{dc}} \tag{26}$$

The compensation ability of the proposed control scheme for unbalanced load can be obtained by (21) and (26). It can also be concluded that when designing the HVDC capacitor, the voltage margin should be considered to cope with the three-phase unbalanced condition.

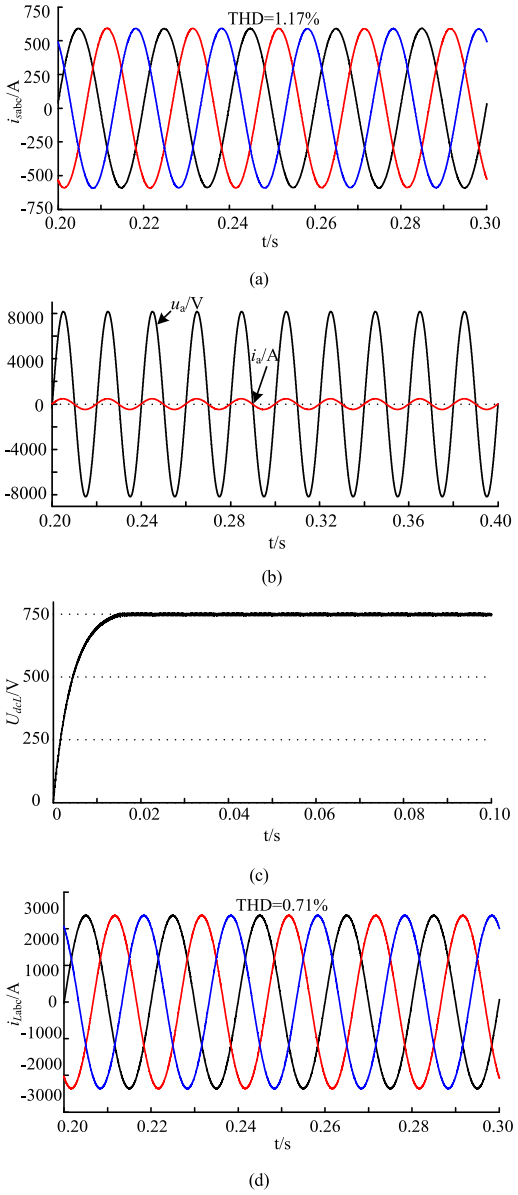

FIGURE 8. Simulation results of SST under ideal grid and balanced load. (a) Three-phase grid-connected current. (b) Grid voltage and current of phase-A. (c) LVDC capacitor voltage of the isolation stage. (d) Three-phase load current of the output stage.

V. SIMULATION RESULTS AND DISCUSSION

To verify the effectiveness of the proposed ROGI-based unbalance compensation method, a three-module cascaded SST simulation model with a three-phase star connection as shown in Fig. 1 has been built in MATLAB/Simulink. The main parameters of the simulation model are listed in Table 1.

Simulation studies are carried out under three situations: a) ideal grid and balanced load; b) unbalanced load; c) severe grid voltage drop. Results of these case studies are presented and discussed below.

A. IDEAL GRID AND BALANCED LOAD

In order to verify the output power quality and operation stability of the SST with the proposed control scheme under

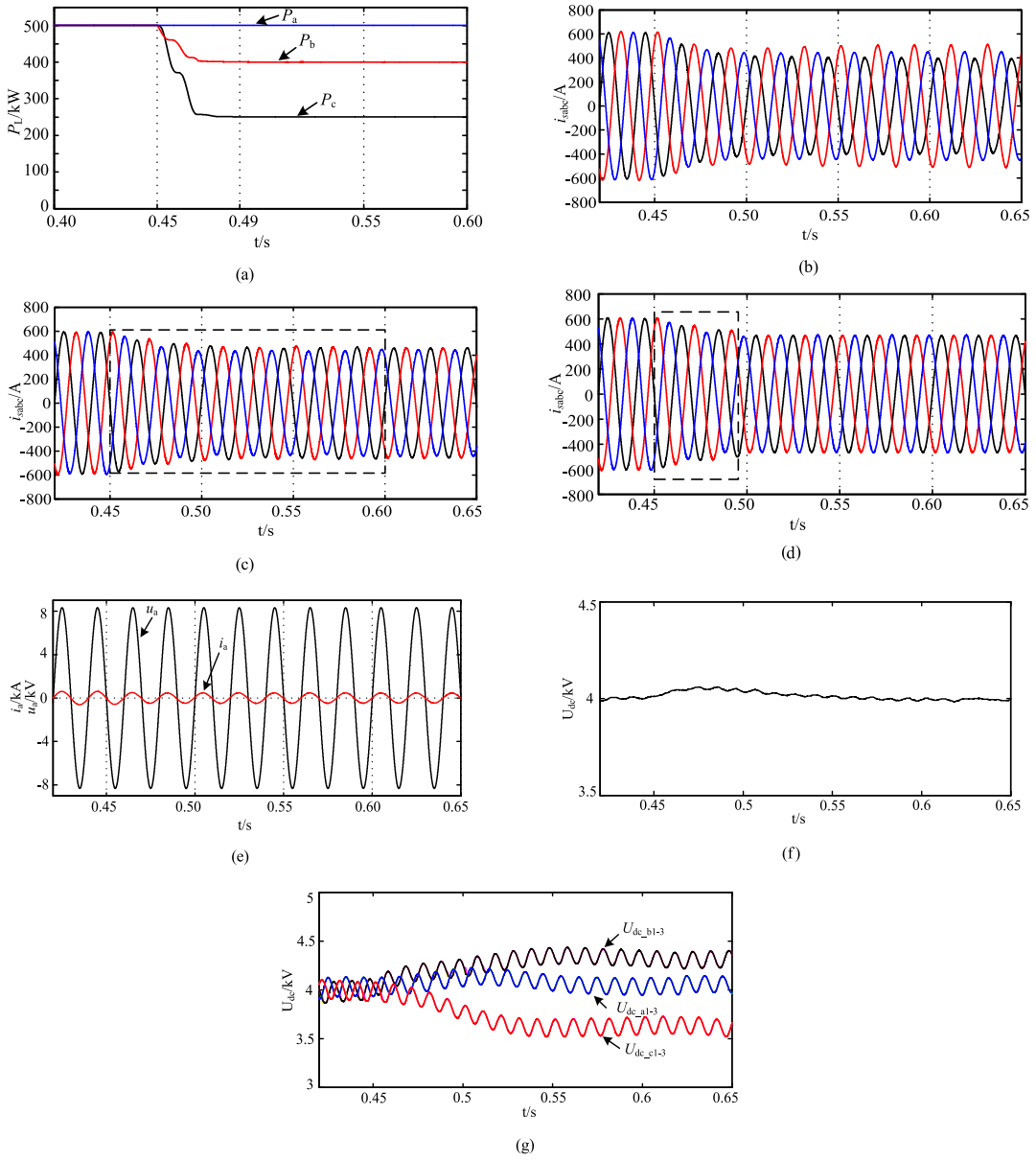

FIGURE 9. Simulation results of SST under unbalanced load condition. (a) Three-phase load power of the output stage. (b) Three-phase grid-connected current without compensation. (c) Three-phase grid-connected current with sequence compensation based on dual synchronous reference frames. (d) Three-phase grid-connected current with the proposed compensation method. (e) Grid voltage and current of phase-A after compensation. (f) Average voltage of the HVDC capacitors. (g) Voltage of all sub-modules HVDC capacitors.

ideal grid and balanced load, the grid voltage and load power for the three phases are assumed to be identical, i.e., 1:1:1. Simulation results of this case study are shown in Fig. 8.

It can be seen from Fig. 8(a) that the three-phase grid-connected current of the SST is symmetric under ideal grid and balanced load condition, and the total harmonic distortion (THD) of the current is only 1.17%. Taking one phase as an example, Fig. 8(b) shows that the grid voltage and current are in phase, which indicates that the SST operates at unity power factor. Fig. 8(c) shows that the LVDC capacitor voltage control performance is excellent. Fig. 8(d) shows that the three-phase load current is balanced with a THD of 0.71% only.

The simulation results of case A indicate that the proposed compensation scheme in this paper does not affect the power quality and operation ability of the SST under ideal grid and balanced load condition.

B. UNBALANCED LOAD CONDITION

In order to testify the compensation effects and response speed of the proposed control scheme, the ratio of the three-phase load power is changed from 1:1:1 to 1:0.8:0.5 at 0.45 s. The simulation results of this case study are shown in Fig. 9.

Fig. 9(a) shows that the load power is becoming unbalanced at $t = 0.45$s as per the ratios specified above. It can be seen from Fig. 9(b) that the grid-connected current is

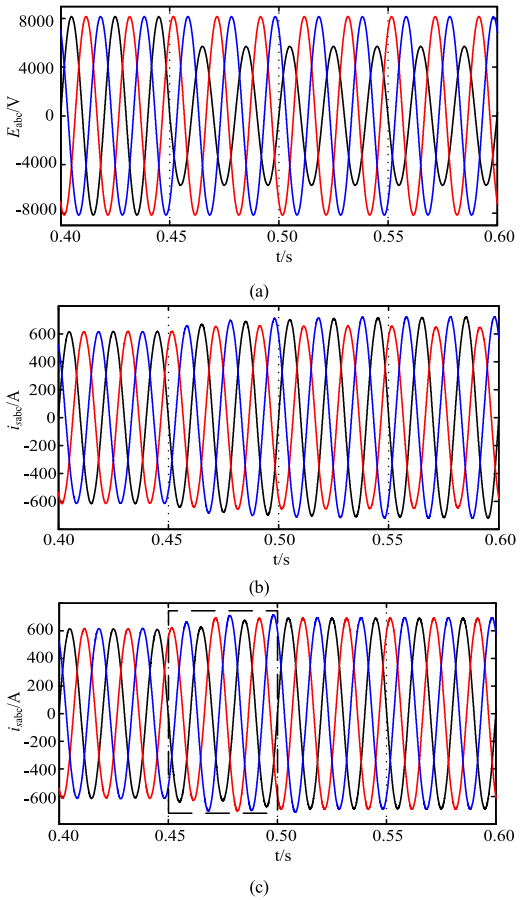

FIGURE 10. Simulation results of the SST under severe grid voltage drop condition. (a) Three-phase grid voltage. (b) Three-phase grid-connected current without compensation. (c) Three phase grid current with compensation based on ROGI controller.

becoming asymmetric when the SST operates under unbalanced load condition without any compensation technique. In this case, a negative-sequence current will be injected into the power grid.

Fig. 9(c) and Fig. 9(d) depict the grid-connected current of the SST with the conventional sequence compensation based on dual synchronous reference frame and the proposed method in this paper; respectively. While both compensation techniques are successful in retaining the balance of the grid-connected current, the ROGI-based unbalance compensation control scheme shows a rapid response time. It can be seen from Fig. 9(c) and Fig. 9(d) that the grid-connected currents are compensated after 0.04 s when the ROGI-based compensation scheme is adopted, whereas the response time is 0.15 s when the sequence compensation is used. This indicates that the proposed compensation scheme features better dynamic performance than the traditional method.

Fig. 9(e) shows that the grid voltage and current are still in phase after compensation, which indicates that the SST is still operating at unity power factor condition during the compensation process.

Fig. 9(f) presents the average voltage waveform of the HVDC capacitors. It can be seen that the average voltage of capacitors deviates from 4 kV for a while, but quickly returns to the command value.

Fig. 9(g) illustrates the voltage waveforms of all sub-modules HVDC capacitors. It can be seen that the HVDC capacitors voltage of each phase is unbalanced after the compensation process, but the highest voltage does not exceed 4.5kV. If the voltage margin is taken into consideration when selecting power devices, the unbalance in case B is still within the compensation capability of the proposed method.

In order to quantify the compensation effects intuitively, the three-phase unbalance factor of current is introduced [26], which is defined as follows:

$$\Delta I_s\% = \frac{i_{s\,max} - i_{s\,min}}{i_{s\_ave}} \times 100\% \tag{27}$$

where i_{smax} and i_{smin} are the maximum and minimum peak values of the three-phase grid currents, respectively; i_{s_ave} is the average value of the three-phase current amplitudes.

A numerical comparison of the compensation effects based on the conventional and proposed control schemes is presented in Table 2.

TABLE 2. Comparison of unbalance compensation effects based on conventional and proposed control schemes.

Compensation scheme	Phase current	Peak value/A	Three-phase unbalance factor/ΔI_s%	Response time/s
None	i_{sa}	398.3	22.64%	-
	i_{sb}	498.1		
	i_{sc}	449.9		
Sequence compensation	i_{sa}	459.4	2.2%	0.15
	i_{sb}	456.8		
	i_{sc}	449.5		
ROGI-based compensation	i_{sa}	466.5	0.5%	0.04
	i_{sb}	464.1		
	i_{sc}	465.9		

It is obvious to conclude from the Table 2 that the ROGI-based compensation scheme has better steady- and dynamic-compensation performances than the conventional sequence compensation. This attributed to the quarter cycle time delay caused by the decomposition of positive- and negative-sequence currents when the sequence compensation scheme is adopted. Moreover, the complex coordinate transformation and command current calculation of the conventional technique decrease the compensation precision. Conversely, ROGI-based compensation scheme precludes the above process, which definitely improves the response speed and performance of the controller.

C. SEVERE GRID VOLTAGE DROP

In order to verify the robustness of the proposed technique under grid significant voltage drop condition, e_a is assumed to experience a voltage drop of 30% at 0.45 s while the

TABLE 3. The compensation effects of SST under severe grid voltage drop condition.

Compensation scheme	Phase current	Peak value/A	Three-phase unbalance factor/ΔI_s%	Response time/s
No	i_{sa}	711.3	8.1%	-
	i_{sb}	655.6		
	i_{sc}	711.2		
Yes	i_{sa}	690.6	0.5%	0.05
	i_{sb}	690.1		
	i_{sc}	693.7		

three-phase load is balanced. The simulation results of this case study are shown in Fig. 10.

Fig. 10(a) shows the 30% drop of phase-A voltage at $t = 0.45$ s as specified above. Fig. 10(b) presents the grid-connected current of the SST when the grid experiences a voltage drop. Fig. 10(c) presents the gird-connected current when the proposed compensation control scheme is adopted. It can be seen from the Fig. 10(c) that the grid current is retained balancing condition when the ROGI-based compensation scheme is utilized. Thus, the grid current of a particular phase will not be much larger than the other two phases and the largest power device current will be lower than the case without compensation.

The unbalance factor for this case study is calculated and presented in Table 3.

According to the results in Fig. 10 and Table 3, it can be concluded that the SST with the proposed ROGI-based compensation scheme can not only deal with the unbalanced load, but can also be equipped with the ability to withstand voltage drop.

VI. CONCLUSION

In order to enhance the ability of cascaded SST to cope with unbalanced conditions, this paper proposes a new ROGI-based compensation control scheme, which can suppress the negative-sequence current on the grid side by embedding a ROGI on the basis of current PI closed-loop control method in positive synchronous reference frame. The simulation results proved that: a) the proposed compensation scheme can effectively retain symmetrical grid currents and suppress the negative-sequence current under unbalanced condition; b) the response speed and compensation performance of the proposed technique are much better than the conventional sequence compensation scheme; c) the proposed compensation scheme does not affect the power quality and operation performance of the SST under ideal grid and balanced load condition; d) the SST with ROGI-based control scheme has the ability to withstand severe voltage drop.

Compared with the conventional compensation techniques, the proposed method is cost effective and easy to implement.

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ZHENGWEI QU received the B.Sc. degree in power system and automation from the Yanshan University of Hebei, China, in 2000, the M.S. degree in power electronics and power drives from Yanshan University, in 2003, and the Ph.D. degree in electrical engineering from Tsinghua University, Beijing, in 2010. He is currently an Associate Professor with the School of Electrical Power Engineering, Yanshan University, China. His areas of research interests include energy management, power quality, and intelligent measurement in smart grid.

YUNXIAO YAO was born in Yichang, Hubei, China, in 1995. He received the B.Sc. degree in electrical engineering and automation, and the M.S. degree in electrical engineering from Yanshan University, Qinhuangdao, in 2016 and 2019, respectively.

He is currently with State Grid Hubei DC Operation and Maintenance Company, Yichang, China. His current research interests include solid state transformer and its applications in power distribution systems.

YUNJING WANG received the B.Sc. degree in power system and automation from the Yanshan University of Hebei, China, in 2000, the M.S. degree in power electronics and power drives from Yanshan University, in 2003, and the Ph.D. degree in instrument science and technology from Yanshan University, in 2014, where she is currently with the Department of Electrical Power Engineering, as an Associate Professor. Her areas of research interests include application of intelligent algorithm in power systems.

CHUNJIANG ZHANG received the B.Sc. degree in electrical engineering from Northeast Heavy Machinery Institute, Heilongjiang, China, in 1983, the M.S. degree in power electronics from Yanshan University, Hebei, China, in 1988, and the Ph.D. degree in power electronics from the Harbin Institute of Technology University, Harbin, China, in 2008. From 1995 to 2000, he was an Associate Professor with Yanshan University, where he has been a Professor and also the Director of the Key Laboratory of Power Engineering of Hebei Province, since 2000. From 2004 to 2016, he was the Dean of the School of Electrical Engineering, Yanshan University. Since 2016, he has been the President of the Periodical Press, Yanshan University. His current research interests include grid-connected inverter, microgrid control, energy storage systems, and dc/dc converter.

ZHENXIAO CHONG received the B.Sc. degree in electrical engineering from Hainan University, Haikou, China, in 2018. He is currently pursuing the M.S. degree in electrical engineering from Yanshan University, Qinhuangdao, China. His current research interests include solid state transformer and its applications in AC/DC microgrids.

AHMED ABU-SIADA (M'07–SM'12) received the B.Sc. and M.Sc. degrees from Ain Shams University, Egypt, in 1998, and the Ph.D. degree from Curtin University, Australia, in 2004, all in electrical engineering. He is currently an Associate Professor and the Discipline Lead of the electrical and computer engineering with Curtin University. His research interests include power electronics, power system stability, condition monitoring, and power quality. He is the Editor-in-Chief for the *International Journal of Electrical and Electronic Engineering* and a regular reviewer for the various IEEE Transactions. He is the Vice-Chair of the IEEE Computation Intelligence Society and the WA Chapter.