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A Novel Wafer Manipulation Method for Yield Improvement and Cost Reduction of 3D Wafer-on-Wafer Stacked ICs

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Abstract Three-dimensional IC (3D IC) exhibits various advantages over traditional two-dimensional IC (2D IC), including heterogeneous integration, reduced delay and power dissipation, compact device dimension, etc. Wafer-on-wafer stacking offers practical advantages in 3D IC fabrication, but it suffers from low compound yield. To improve the yield, a novel manipulation scheme of wafer named *n*-sector symmetry and cut (SSC*n*) is proposed. In this method, wafers with rotational symmetry are cut into *n* identical sectors, where *n* is a suitably chosen integer. The sectors are then used to replenish repositories. The SSC*n* method is combined with best-pair matching algorithm for compound yield evaluation. Simulation of wafers with nine different defect distributions shows that previously known plain rotation of wafers offers only a trivial benefits in yield. A cut number four is optimal for most of the defect models. The SSC4 provides significantly higher yield and the advantage becomes more obvious with increase of the repository size and the number of stacked layers. Cost model of SSC*n* is analyzed and the cost-effectiveness of SSC4 is established. Observations made are: 1) Cost benefits of SSC4 become larger as the manufacturing overhead of SSC4 become smaller, 2) cost improvement of SSC4 over conventional *basic* method increases as the number of stacked layers increases and 3) for most defect models, SSC4 largely reduces the cost even when manufacturing overhead of SSC4 is considered to be very large.

Keywords 3D IC · Wafer-on-wafer stacking · Compound yield · Sector symmetry and cut · Die per wafer · Cost analysis

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1 Introduction

Despite many challenges, the three-dimensional integrated circuit (3D IC) is a hot topic in semiconductor industry these days [3, 10, 12]. To achieve higher levels of integration, multiple layers of active electronic component are stacked vertically in a 3D IC. Connections between layers are provided by *through silicon vias* (TSVs) [1, 7, 11, 13]. TSVs are short and reduce the need for long interconnects as required on planar ICs, thus reducing the delay and power consumption [3, 25, 26]. Another promising aspect of 3D IC is the heterogeneous integration, which means that dies in the stack may have different functions may even be fabricated by different vendors. They can be optimized according to their own technologies [3, 10, 12]. Moreover a 3D IC offers smaller device footprint, which is desirable in hand-held devices.

Currently, there are three types of layer stacking methods in 3D IC fabrication, namely, die-on-die, wafer-on-wafer and die-on-wafer. Among these wafer-on-wafer stacking is most attractive. It offers the highest production throughput since each stack bonding produces a large number of stacked ICs. Other advantages of wafer-on-wafer stacking include smallest die sizes, thinner wafers, and high TSV

densities [14, 18, 27]. Although the other two stacking methods offer higher final yield, they are harder to handle, stack, and process, besides being expensive [6, 16].

On the other hand, a bottleneck in the wafer-on-wafer stacking is its relatively low compound yield, especially for large number of stacked layers and low wafer yields. Compound yield is defined as the final yield of the 3D IC, ignoring any defect induced during fabrication process such as stacking, bonding, interconnect formation, packaging, etc. It is a theoretical value based on the simple assumption that a pre-bond tested good die stacked on another pre-bond tested good die (or good partial stack) would definitely produce a good stack (or good 3D IC). Without any matching, compound yield of randomly stacked wafers will rapidly decrease as more die are stacked, thus dramatically increasing the cost of wafer-on-wafer fabricated 3D ICs. To improve the compound yield two kinds of efforts are worth mentioning:

1) Matching algorithms have been proposed so as to select the best matching wafers to stack instead of stacking them randomly [14, 16–18, 21, 23, 27].
2) Exploiting empirically observed defect distribution models (e.g., wafer maps with radially clustered defects [17]) or special layouts of wafers (such as fabricating wafer with rotational symmetry so that two wafers can be matched in more ways than one [16, 31, 32]) have been proposed.

Our effort in this work has five parts:

1) A hybrid wafer-on-wafer stacking procedure is proposed in Section 3.5, which combines advantages from several methods [16, 21, 23]. With a combination of best practices in the existing work, this hybrid procedure serves as a reference for comparing with the novel sector symmetry and cut method, which is the core contribution of this work.
2) A novel manipulation scheme of wafers is introduced. To be specific, wafers fabricated with rotational symmetry are cut into identical sectors (called subwafers). We refer to two subwafers as identical if they have the same die distribution and die orientation. These identical subwafers are then used to replenish the repository. A repository consists of wafers corresponding to a specific layer of a 3D IC stack. The simulation results show that sector symmetry and cut method produces much higher compound yield than that of existing methods [14, 16–18, 21, 23, 27]. For example, compared with the work in [17, 21, 23], the relative improvement of compound yield can reach as high as 189 %.
3) We derive mathematical formulations for die per wafer (DPW) calculation considering rotational symmetric wafers. We demonstrate that larger capability of rotation produces more flexibility of wafer matching, but also increases the number of die lost due to the sector symmetry. Extensive experiments (parts of experimental results are shown in the appendix) have been done to find the optimal number of cuts.
4) We compare the compound yield of different stacking procedures under various defect distribution models.
5) We construct a cost model of SSC*n* and conduct detailed cost analysis of SSC4. We demonstrate that compared to conventional method, SSC4 largely reduces the 3D IC cost under various defect distribution models, especially for situations where the number of stacked layers is large.

The rest of this paper is organized as follows. Section 2 introduces the background and motivation for this work. Section 3 discusses various aspects of wafer-on-wafer stacking closely related to this work. An original contribution is given in Section 4 that proposes a novel wafer manipulation method named *sector symmetry and cut* (SSC*n*). Simulation results are presented in Section 5 where yield comparison with related work [17, 21, 23] is given. The cost-effectiveness of SSC*n* is analyzed in Section 6. Section 7 concludes the paper.

2 Background and Motivation

Since a major bottleneck in wafer-on-wafer stacking is the low compound yield, many researchers have proposed optimal matching algorithms to improve the yield. Smith et al. [18] stack wafers with same or similar wafer maps from different repositories. Reda et al. [14] propose several matching algorithms including a globally greedy matching, an iterative matching heuristic (IMH), and a global optimal matching based on integer linear programming (ILP). Verbree et al. [27] propose an iterative greedy matching algorithm, which applies globally greedy matching to only two repositories at a time. Both proposals [14, 27] are based on static repositories, which means none of the repositories will be replenished until they run out of wafers. Contrary to the static repository scheme, Taouil et al. [21, 23] propose the concept of running repositories. After a wafer leaves a repository, a new wafer immediately enters that repository so the repository will always be full of wafers. This new scheme of replenishing repositories is proven to offer higher compound yield and, more importantly, lower run time complexity than the static repository system.

All of the above methods consider only wafer maps with uniform defect distribution, which is not a good model for describing defect distribution in the real world. It is

well known that the defects on wafers are clustered [9, 24, 29, 30]. A clustered defect distribution model was first applied by Singh [17] to wafer-on-wafer stacking. Singh's work shows that with the same stacking procedure, more practical wafer maps generate higher compound yield than wafer maps with uniformly distributed defects. However, the matching algorithm [17] is based on a static repository instead of running repository, which may not fully exploit the advantage of the clustered defect model. Also, in industry, there may be various kinds of defect distribution models on the wafer.

Singh [16] proposes a way to fabricate wafers with rotational symmetry such that two wafers can be matched four ways to find the best match. The rotational symmetry offers a new strategy regardless of what matching algorithm is used. With rotations the repository size is virtually multiplied by the rotation number (4 in this case), which is helpful for the improvement of compound yield. Weaknesses of the contribution [16] include an impractical assumption of uniform defect distribution and the use of only a static repository.

Figure 1 shows four different aspects of the stacking procedures: defect distribution models, wafer manipulations, repository replenishment schemes, and matching algorithms. Notice that these aspects are generally independent of each other and any alternative can be generally selected for one aspect without interfering with choices for others. In Fig. 1, a top to bottom path shows the choices made by a referenced work. For example, the leftmost path [14] means that uses a uniform defect distribution model, takes no action for wafer manipulation, and uses greedy, IMH, and an ILP matching algorithms based on static repository replenishment scheme. Viewed horizontally, Fig. 1 arranges existing works in an ascending order of their publication date.

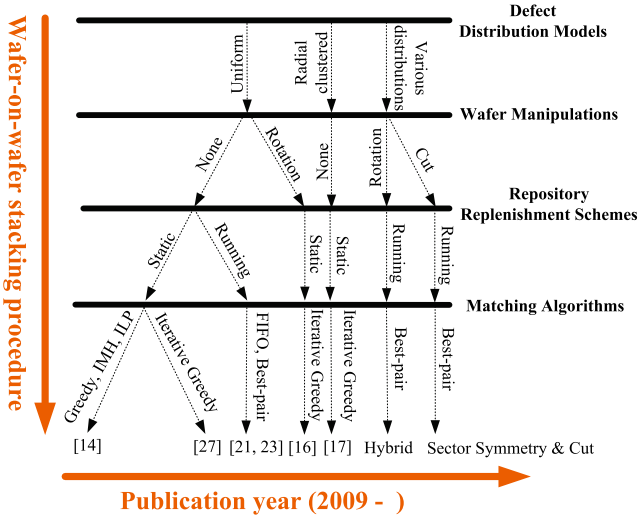


Fig. 1 Wafer-on-wafer stacking procedures

To express the motivating factors for the present work, let us examine the two rightmost paths in Fig. 1:

1) If we consider the manipulation of wafer rotation [16], and wafer matching based on a running repository scheme [21, 23], the compound yield should be improved. That motivates the *hybrid* scheme.
1) The motivation for a *sector symmetry and cut* strategy comes from the realization that compared with die-on-die and die-on-wafer stacking, the low yield of wafer-on-wafer stacking is due to the restriction that a die on a wafer must be matched with exactly one die on another wafer. In other words, any pair of dies to be bonded together must occupy the same geometric position on respective wafers. If the wafers are cut into smaller parts of identical shape, then the effect of this restriction can be reduced. Moreover, if the wafers being cut are fabricated with rotationally symmetric sectors, then each cut sector (subwafer) will look identical. As will be illustrated in this paper, greater matching flexibility and higher compound yield can be achieved. Cost analysis of this manipulation method also shows large reduction of 3D IC cost.

3 Preliminaries

3.1 Defect Distributions on a Wafer

A negative binomial defect distribution model [2, 15, 19, 20] has been widely used to estimate the die yield as a function of defect density, die area, and a clustering parameter. However, this model does not provide enough information for us to generate wafer maps with certain observed patterns like radial symmetry, periodicity, offset, etc. Because of the strict confidentiality in the industry, data on real wafers are not always exposed. This explains why most publications assume a uniform distribution of defects [14, 16, 18, 21, 23, 27]. The problem with this assumption is that the *unrealistic* uniform distribution model always leads to a pessimistic compound yield in the wafer-on-wafer stacking procedure [17].

Based on previous literature [4, 5], nine patterns of wafer maps corresponding to different defect distributions are generated for the yield analysis of wafer-on-wafer stacking procedure. The spatial probability functions of these nine patterns are shown in Fig. 2 where different gray levels correspond to different levels of yield ranging from zero (black pixel) to one (white pixel).

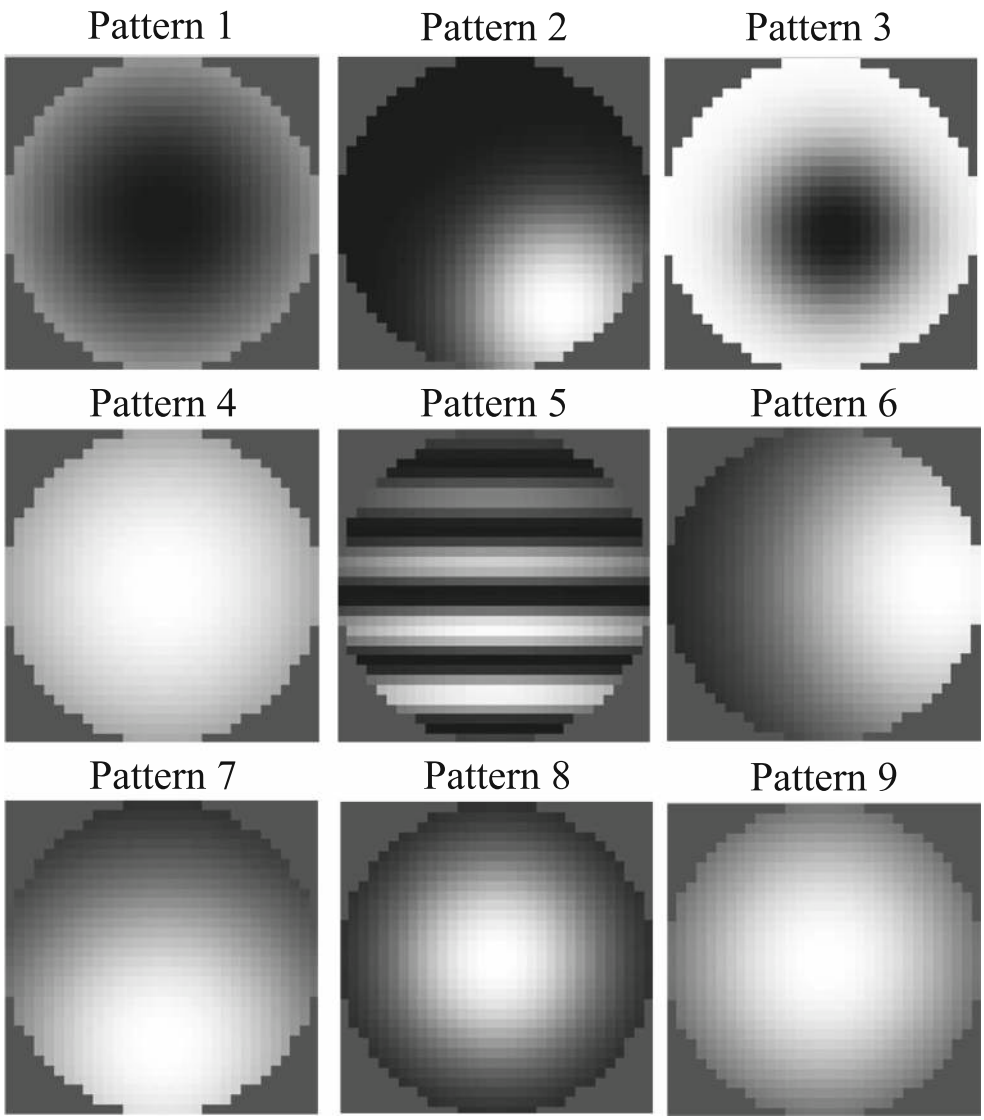


Fig. 2 Gray maps showing the yield level distribution on the wafer

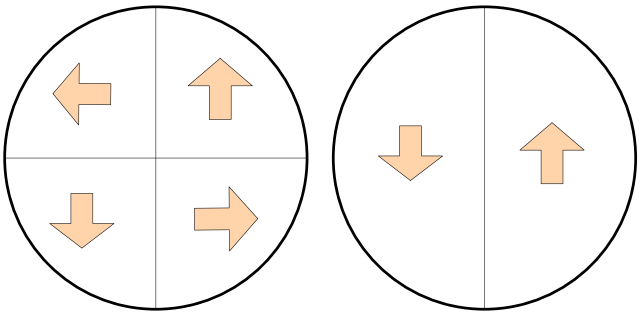
Briefly, the nine defect distribution patterns are:

- Pattern 1: A large central spot showing the low yield at the center of the wafer.
- Pattern 2: A shifted semi-ring showing higher yield at the lower right corner of the wafer.
- Pattern 3: A slightly shifted small spot.
- Pattern 4: A very thin centered ring showing radial yield degradation.
- Pattern 5: A mixed pattern of repetitive rows and shifted semi-ring.
- Pattern 6: A shifted semi-ring showing higher yield level at the right corner of the wafer.
- Pattern 7: A shifted semi-ring showing higher yield level at the lower part of the wafer.
- Pattern 8: A thick centered ring showing radial yield degradation.
- Pattern 9: A relatively thin centered ring showing radial yield degradation.

In this paper, experiments are conducted based on the wafer maps generated from Fig. 2.

3.2 Wafers with Rotational Symmetry

An example of a wafer with rotational symmetry is illustrated in Fig. 3a where the die distribution on the wafer is symmetric with respect to both the horizontal and vertical lines. The die orientation in (a) has 90° difference between adjacent quadrants. If wafers in all repositories have this characteristic, then any pair of wafers drawn from two different repositories can be matched in four ways where one wafer is rotated with respect to the other by 0, 90, 180 or 270 degrees. This virtually enlarges the physical repository



(a) Four-fold rotation (b) Double rotation

Fig. 3 Wafer maps showing rotational symmetry

size four times. The wafer map introduced in [16] is only capable of such four fold rotation. We also consider wafers capable of two fold rotation. As shown in Fig. 3b, the wafer will look identical after each 180° rotation if the die distribution is anti-symmetric across the vertical line, i.e., two halves of the die are oriented with 180° rotation.

3.3 Running Repository Based Best-Pair Matching Algorithm

Running repository scheme is considered in all experiments in this paper since it provably produces higher yield and lower run time complexity than the static repository. Based on such a scheme, the matching algorithm is chosen as the best-pair based algorithm [21, 23] due to its high yield. Thus, wafers from the first two repositories are matched without any restriction, and the pair producing maximum yield is selected (best-pair match). Then the pair of wafers as a whole is matched with every wafer from the next repository to find the best one (best-one match), and the same process iterates until the last repository. After one complete stack is formed, each repository is replenished immediately. This process is repeated until the production size (total number of stacks fabricated in production) is reached. Note that in the matching algorithm, the matching criterion can produce multiple choices.

3.4 Matching Criteria

The purpose of wafer matching is to get the maximum final compound yield for a given production size. Given two pre-bond tested wafers, there are basically three criteria to find how well they match [21, 23]: (1) the number of matching good dies (MGD); (2) the number of matching bad dies (MBD); (3) the number of unmatched faulty dies (UFD). An UFD is formed either by a good die overlapping a bad die or a bad die overlapping a good die. Since most publications on wafer matching consider only MGD as the criteria [14, 16–18, 27] we also use MGD, given that evaluating the best matching criterion is not our focus here.

Wafers are tested prior to bonding. To determine the matching yield of wafer bonding, the state of a tested wafer is represented by a $h \times v$ test matrix of h columns and v rows, where h and v are the maximum number of chips on the wafer along two perpendicular axes termed as horizontal and vertical, respectively. Elements of the test matrix are [0,1] integers. A "1" means a good device and "0" means a bad or non-existing device. Thus, the sum of all elements normalized with respect to the number of device sites on the wafer gives the wafer yield.

When two wafers are stacked, a stacking matrix for the wafer stack is another $h \times v$ matrix whose elements are products of the corresponding elements of test matrices of wafers. The stacking matrix assumes an ideal stacking, i.e., two good devices produce a good stack. It provides the stacking yield in the same way as the test matrix of a wafer gives the wafer yield. Adding wafers to a partial stack combines test matrices of wafers with the stacking matrix of the previous stack in a similar way. Depending on the manufacturing procedure, whenever a complete or partial stack is tested, the stacking matrix is converted into a test matrix by changing the entries for failed stacks to "0".

3.5 A Hybrid Wafer-on-Wafer Stacking Procedure

Based on previous work, we propose a hybrid wafer-on-wafer stacking procedure, which incorporates the rotational symmetry of wafers [16] and running repository based best-pair matching algorithm [21, 23]. This procedure combines the merits of several practices shown in Fig. 1.

It has been proven [16] that by simple rotation the compound yield can be improved. The reason is quite straightforward: each rotation of a symmetric wafer actually produces a new wafer map, and the repository size is virtually enlarged by as many times as the wafer can be rotated (Fig. 3). Therefore, we choose a rotationally symmetric wafer in this work. We further select the running repository replenishment scheme and a best-pair matching algorithm to construct a hybrid procedure. We evaluate this hybrid procedure for various defect distribution models.

The initial expectation from this hybrid stacking procedure was that it would produce a considerable compound yield improvement. However, detailed experimental results in Section 5 actually show only trivial improvement. Nevertheless, the hybrid procedure serves as a reference for comparison to the work in the next section which is the core contribution of this paper.

4 Sector Symmetry and Cut for Yield Improvement

The hybrid procedure does not adequately overcome the restrictions of flexibility in matching good dies in wafer

stacking. In this section, a novel manipulation scheme of *sector symmetry and cut* is presented to help ease such restrictions.

4.1 Wafers Cut into Sectors

Compared with just rotating the wafer, a more flexible manipulation is to cut each individual wafer to several sectors (called subwafers). If all wafers can be cut to subwafers, then a subwafer can match with any subwafer cut from the same wafer location in another repository. Previously, all subwafers of a wafer were kept together (uncut) during wafer matching. Because by cutting the wafer, the restriction of matching a sector from one wafer with another sector of another wafer applied. Figure 4 shows four 90° sectors cut from a conventional wafer where the arrow indicates the die orientation within a sector. Similarly, we can cut the wafer into halves (180° sectors) or any number of sectors.

Cutting the wafer into sectors offers an adaptive method between wafer-on-wafer stacking and die-on-die stacking. Comparing with die-on-die stacking, the throughput is largely increased because now each stack produces a sector of 3D ICs. Comparing with wafer-on-wafer-stacking, the yield should be improved because of reduced restrictions in matching sectors rather than matching wafers.

It is quite obvious that extreme cutting (too many sectors) will start losing the advantage because it will get closer to die-on-die stacking, which has highest yield but has a high assembly cost too. Compared to wafer stacking a downside of sector stacking is that stacking and bonding of individual sectors requires larger amount of effort. Besides, the sector oriented wafer layout causes a loss of chip sites that increases with the number of sectors. With a properly selected sector size, the benefit of matching flexibility, higher yield, and lower cost can outweigh the disadvantages.

4.2 Sector Symmetry and Cut

After cutting the wafers into subwafers (sectors), each subwafer can only be matched to another subwafer located at the same position within the wafer. For example, the top-left subwafer (second subwafer in Fig. 4) from repository 1 can only be matched to the top-left subwafer from repository 2. If all subwafers look identical, the restriction due to subwafer location on wafer is eliminated and matching will become more flexible. The idea to obtain identical subwafers from a wafer is straightforward. If subwafers are cut from a wafer fabricated with rotational symmetry, all subwafers will look identical.

Figure 5 illustrates the sector symmetry and cut manipulation to the wafer in Fig. 3a. Similarly, the wafer can be cut to halves to get two identical subwafers. Now, any subwafer from one repository can be matched to any subwafer from another repository. The sector symmetry and cut method provides more choices for subwafer stacking in matching algorithms.

4.3 Discussion on the Number of Cuts

It is natural to think about cutting wafers with rotational symmetry to more sectors than just 2 or 4. However, if a wafer is cut to either 3 or more than 4 sectors, new challenges appear. We make two observations. First, dies on the wafer cannot be arranged as compactly as in the case of 2 or 4 sectors. In other words, there will be space wasted at the edges of each sector due to the square or rectangular shape of the chip. Second, cutting a wafer to too many small sectors will generate a circular area of certain radius inside which chips cannot be printed, i.e., the area within the circle will be too small to accommodate a complete die.

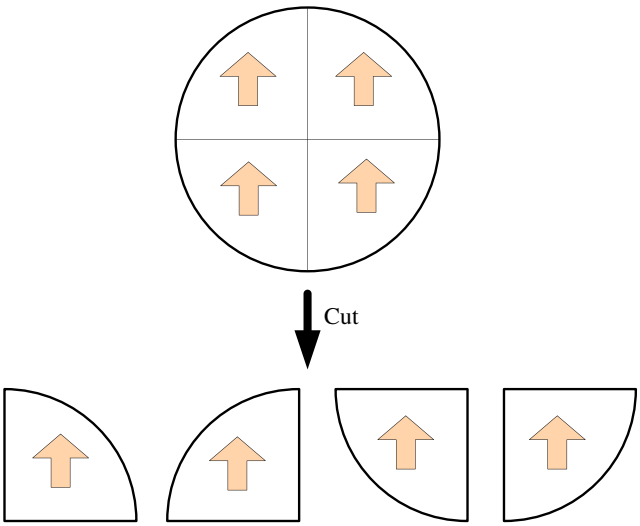


Fig. 4 A conventional wafer cut into four sectors

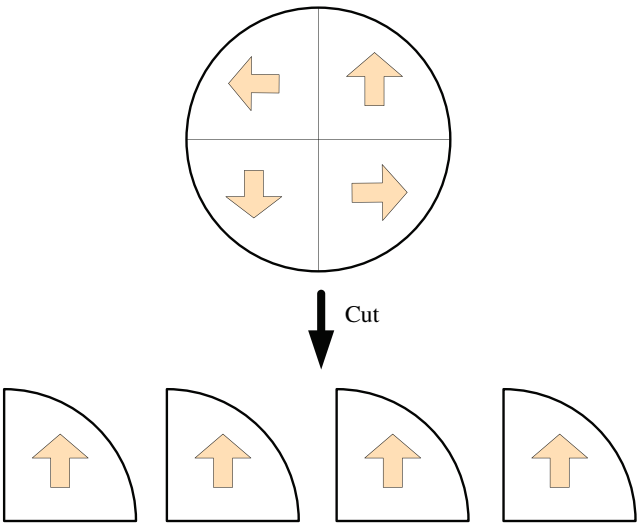


Fig. 5 Cutting a rotationally symmetric wafer into identical subwafers

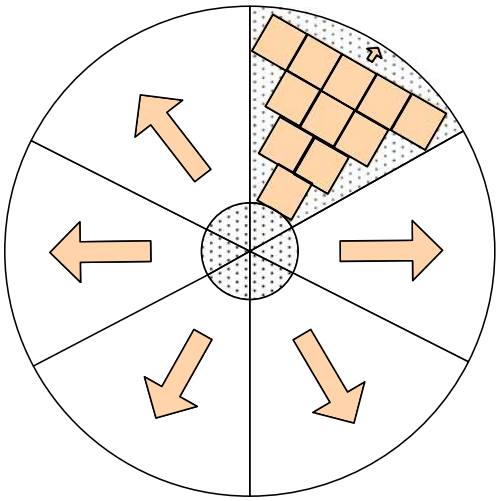


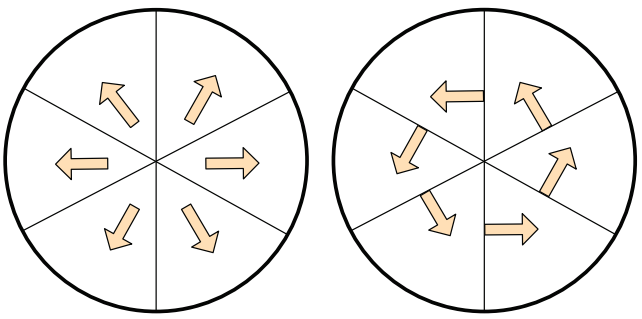
Fig. 6 Illustration of die loss for cutting the wafer into 6 sectors

Figure 6 illustrates this point where the wafer is divided into 6 equal sectors. The dotted areas indicate where there is not enough space to accommodate a full die. These areas are either at the edge of the sector or near the center of the wafer. The dotted central area form a small circle where no single die can be placed within a sector.

Thus, cutting a wafer into sectors when the number of sectors is neither 2 nor 4 will waste some wafer area and reduce the number of dies per wafer (DPW). Correspondingly, the cost of producing a 3D IC will increase which must be compensated for by the increased stacking yield.

Rotationally symmetric wafers can use two alternative die placements as illustrated in Fig. 7. The two placements yield different DPW. Geometrical parameters used for computing DPW are defined in Table 1. Note the vertical and horizontal spacings between dies on the wafer are already included in the die height H and die width L.

Figure 8 shows a sector with die orientation of Fig. 7a. We call this placement method 1. Number of rows $N1_1$ of



(a) Placement method 1 (b) Placement method 2

Fig. 7 Two different ways of placing dies on a rotationally symmetric wafer

Table 1 Geometrical parameters for dies per wafer (DPW) calculation

Variable	Definition
r	Radius of wafer excluding edge clearance
cut_{num}	Number of cuts per wafer
H	Height of die
L	Length or width of die
α	Angle of sector

die that can be placed below the dotted line in Fig. 8 is computed as,

$$N1_1 = \left\lfloor \frac{r cos\frac{\alpha}{2} - \frac{L}{2tan\frac{\alpha}{2}}}{H} \right\rfloor \tag{1}$$

Note that the triangle of height $\frac{L}{2tan\frac{\alpha}{2}}$ part at the tip of the sector cannot hold any die. Number of die per sector $DPS1_1$ in $N1_1$ rows is obtained as,

$$DPS1_1 = \sum_{i=1}^{N1_1} \left\lfloor 1 + 2(i-1)\frac{H}{L} tan\frac{\alpha}{2} \right\rfloor \tag{2}$$

Number of rows $N1_2$ of die that can be placed above the dotted line in Fig. 8 is computed as,

$$N1_2 = \left\lfloor \frac{r - N1_1 H - \frac{L}{2tan\frac{\alpha}{2}}}{H} \right\rfloor \tag{3}$$

and the number of die per sector $DPS1_2$ accommodated in these $N1_2$ rows is,

$$DPS1_2 = \sum_{i=1}^{N1_2} \left\lfloor \frac{2\sqrt{r^2 - \left(N1_1 H + iH + \frac{L}{2tan\frac{\alpha}{2}}\right)^2}}{L} \right\rfloor \tag{4}$$

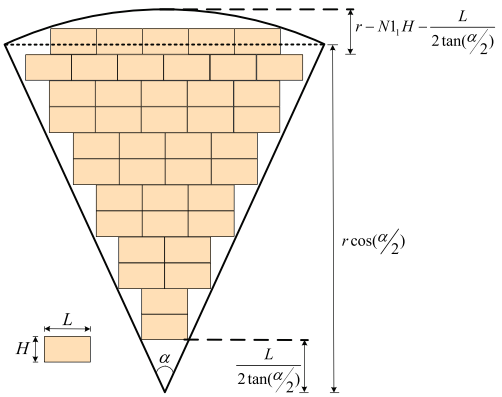


Fig. 8 Calculation of $DPW1$ for sector placement method 1

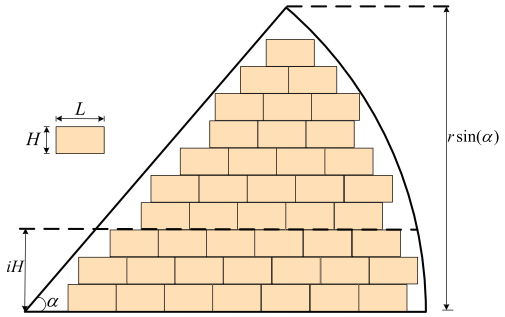


Fig. 9 Calculation of $DPW2$ for sector placement method 2

Thus, total number of die per sector $DPS1$ in Fig. 8 is obtained as,

$$DPS1 = DPS1_1 + DPS1_2 \tag{5}$$

Figure 9 shows a sector from Fig. 7b. We refer to this as placement method 2. Number $N2$ of rows of die that can be placed in this sector is,

$$N2 = \left\lfloor \frac{rsin(\alpha)}{H} \right\rfloor \tag{6}$$

A careful examination of method 2 shows that the case for 3 cuts need to be examined separately. Die distribution on a sector with 2 cuts is basically a combination of two sectors from the 4 cut placement. For 4 or more cuts, we obtain the number of die per sector as,

$$DPS2 = \sum_{i=1}^{N2} \left\lfloor \frac{\sqrt{r^2 - (iH)^2} - \frac{iH}{tan(\alpha)}}{L} \right\rfloor \tag{7}$$

Figure 10 shows the die placement of 3-cuts in placement method 2. $N2_1$ and $N2_2$ are the numbers of rows of die that can be placed below and above the dotted line, respectively, in Fig. 10. Numbers of die per sector $DPS2_1$ and $DPS2_2$ for these sections are computed as follows:

$$N2_1 = \left\lfloor \frac{rsin(\alpha)}{H} \right\rfloor \tag{8}$$

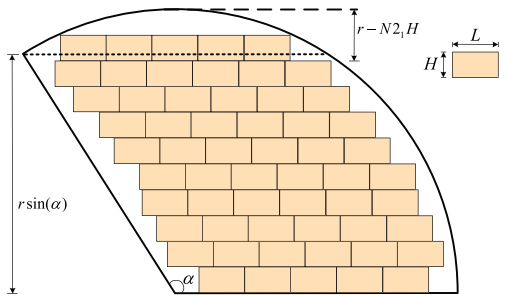


Fig. 10 Calculation of $DPW2$ of 3-cuts for sector placement method 2

$$DPS2_1 = \sum_{i=1}^{N2_1} \left\lfloor \frac{\sqrt{r^2 - (iH)^2} - \frac{(i-1)H}{cot(\alpha)}}{L} \right\rfloor \tag{9}$$

$$N2_2 = \left\lfloor \frac{r - N2_1 H}{H} \right\rfloor \tag{10}$$

$$DPS2_2 = \sum_{i=1}^{N2_2} \left\lfloor \frac{2\sqrt{r^2 - [(N2_1 + i)H]^2}}{L} \right\rfloor \tag{11}$$

Thus, total number of die per sector $DPS2$ for method 2 in Fig. 10 is obtained as,

$$DPS2 = DPS2_1 + DPS2_2 \tag{12}$$

Number of die per wafer $DPWq$ for cut_{num} cuts, where $q = 1$ or 2 refers to the placement method 1 or 2, is calculated as,

$$DPWq = DPSq \times cut_{num} \tag{13}$$

We consider 8 inch wafers with 5-mm edge clearance and square die of size 31.8 mm × 31.8 mm. A die spacing of 0.04 mm is assumed. For the selected wafer size and die area, the number of die per wafer is 812 for normal wafers. This number is obtained by using (7) and (13) for 4 cuts in placement method 2.

Figure 11 compares the two placement methods for various numbers of cuts. We see a general trend that as the number of cuts increases (larger capability of rotation) the DPW decreases. Also, placement method 2 always outperforms method 1 from DPW point of view. Actually, through large amount of experiments considering different wafer sizes, die sizes, and chip aspect ratios, we find placement method 2 outperforms method 1 most of the time. That is why we consider placement method 2 in this work. Note that DPW for 2-cuts and 4-cuts with placement method 2 have the DPW of a conventional wafer without cutting.

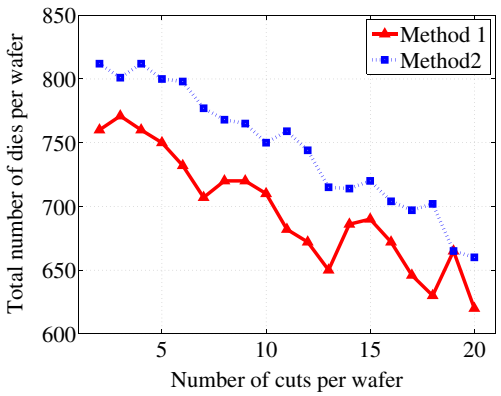


Fig. 11 $DPW1$ and $DPW2$ versus number of cuts for placement methods 1 and 2

Equations (1)–(13) are derived for calculating DPW of rotational symmetry wafers, however, like previous work on DPW calculation [8, 28], they can also be applied to DPW calculation of conventional wafers.

4.4 Summing it up

Figure 12 shows the complete stacking procedure of the sector symmetry and cut method applied to an example of 3 stacking levels. Initially all repositories are filled with subwafers. For a given repository size k, there will be either $2k$ or $4k$ subwafers within each repository, depending on whether a wafer is cut into 2 or 4 pieces. The best-pair match between the first two repositories and the best match for the rest of the repositories are conducted afterwards. Consider for now that the matching is with respect to subwafers instead of wafers. For each repository replenishment, there is a back-up wafer which is cut and rotated. As one subwafer leaves a repository, a new subwafer from the back-up wafer will replenish the repository, immediately. Once the back-up wafer is used up, a new back-up wafer will replace it. Since running repository based best-pair matching algorithm is used in Fig. 12, the run time complexity is $O(cut_{num} \times k \times p \times i)$ [21, 23] where cut_{num}, k, p and i are number of cuts, repository size, production size and number of stacked layers, respectively.

We have done extensive Monte Carlo experiments based on different defect models, wafer sizes, and die sizes. The results show that in most cases 4-cuts yield the maximum number of good 3D ICs compared to other numbers of cuts. So a rule-of-thumb is to cut wafer into 4 quadrants. Part of our experiment results are shown in the appendix to illustrate this point. In this work, we emphasize on introducing the significance of wafer cut methodology, and only consider cutting wafers into 2 or 4 sectors (where no die loss occurs) in the next section. We summarize five types manipulations of wafers in Table 2.

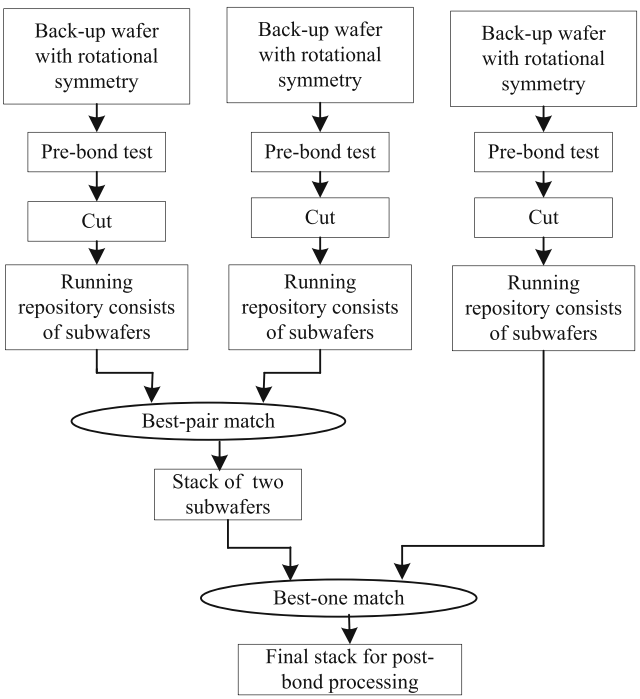


Fig. 12 Process flow of sector symmetry and cut method

5 Experimental Results

5.1 Experimental Setup

Same wafer and die as in Section 4.3 were used in this experiment. Figure 2 is used to generate the nine different patterns of wafer maps. If not specified explicitly, a default production size of 100,000 3D ICs is targeted in the experiments. All the experiments are repeated 1,000 times and results are averaged to remove noise.

The running repository based best-pair matching algorithm was used [21, 23]. Initially, k'^2 ($k' = cut_{num} \times k$) comparisons provide the match information for all wafer (subwafer) pairs from the first two repositories. To speed up the matching algorithm, a heap structure is used to store the match information. Each time a pair of wafers (subwafers) leaves the first two repositories, the corresponding elements are pruned from the heap. As two new wafers (subwafers) enter the first two repositories, their relationships with the existing wafers (subwafers) are constructed and added to the heap. Once the heap is constructed, only $2k'-1$ comparisons are needed each time to replenish the heap.

Five manipulations of Table 2 are combined with running repository based best-pair matching algorithm. The names of these manipulations refer to the complete stacking procedures depending on the context. Recall that the rotation manipulation in Table 2 combined with running repository based best pair matching algorithm is the hybrid stacking procedure proposed in Section 3.5. Thus, Rotation in this section represents the hybrid procedure.

Table 2 Wafer manipulation methods

Names	Explanations
Basic	Wafers without rotational symmetry are matched.
Rotation 4	Wafers are matched using 4-way rotational symmetry.
Rotation 2	Wafers are matched using 2-way rotational symmetry.
Sector Symmetry and Cut 4 (SSC4)	Sectors are matched after 4-way symmetric wafers are cut into 4 sectors.
Sector Symmetry and Cut 2 (SSC2)	Sectors are matched after 2-way symmetric wafers are cut into 2 sectors.

5.2 Comparison of Various Stacking Procedures for Different Defect Distributions

In this section we examine the compound yields of final 3D ICs with different stacking procedures under nine different defect distribution models. Initially, the yield of *basic* procedure with repository size 1 (i.e., random stacking without matching) is calculated for nine types of defect patterns. Subsequently, for each type of pattern, yields for all procedures are normalized with respect to the corresponding random stacking yield. The normalized yield versus repository size for different stacking procedures and defect distributions are shown in Fig. 13 for 3 stacked layers.

The legends in Fig. 13 indicate different stacking procedures. For example, ***basic*** (see Table 2) means the procedure uses running repository based best-pair matching algorithm, without any manipulation to wafers. As mentioned in Section 5.1, *Rotation* is the hybrid procedure in Fig. 1.

Next, we compare the performance of different stacking procedures. Regardless of what defect model is used, yield of SSC*n* procedure is always higher than that of others. The reason for superiority of the SSC*n* procedure is that the restrictions among subwafers are reduced while in Rotation

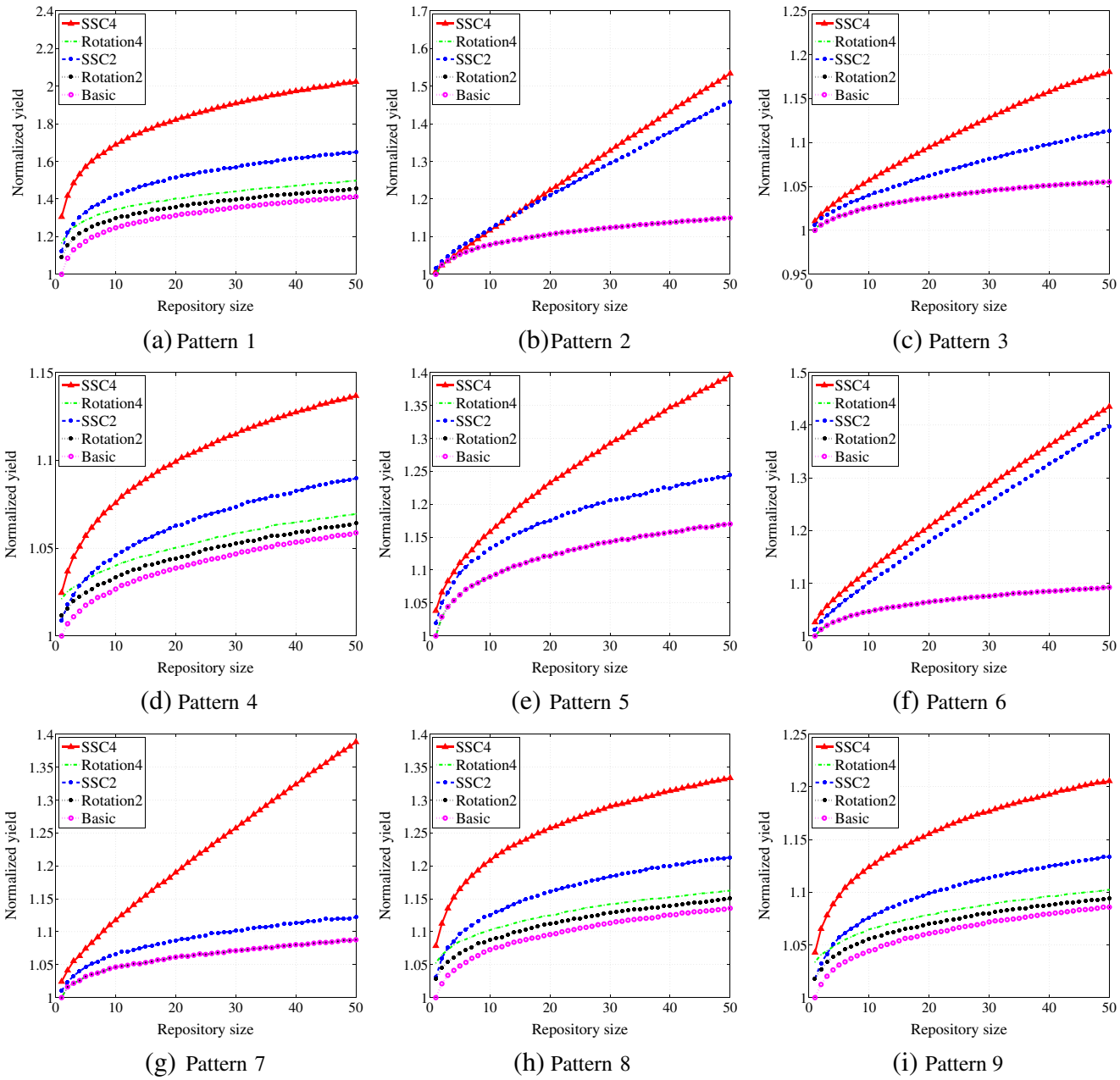


Fig. 13 Yield improvement by various stacking procedures for different defect distribution patterns of Fig. 2

and *basic* all subwafers are bonded together. In SSC*n*, subwafers selected from the same repository are not necessarily from the same wafer. The differences between SSC*n* and Rotation become more obvious as the repository size grows from 1 to 50. As shown in Fig. 13, there are up to 50 % differences in normalized yield between SSC4 and Rotation 4 when repository size reaches 50.

We evaluate the impact of number *n* of cuts on the yield of SSC*n* procedure. It is obvious from Fig. 13 that SSC4 always has a higher yield than SSC2. The reason for the yield difference between these two is that in both cases there is no die loss and greater flexibility is provided in SSC4. In SSC4, each wafer is cut to 4 pieces reducing restrictions between subwafers and this produces a virtual repository twice the size of the virtual repository of SSC2.

We further evaluate the impact of rotation number *n* on the yield of proposed hybrid procedure. As can be seen from Fig. 13, for patterns 1, 4, 8 and 9, yield of Rotation 4 is better than those for Rotation 2 and *basic*, but the improvement is slight. Why does larger rotation number not help the hybrid procedure significantly? A possible explanation is that under patterns 1, 4, 8 and 9, bad dies are already clustered either at the center or near the edge of wafers, in which case rotating the wafer does little for aligning good dies. For the rest of the patterns, we can see the yield of Rotation and *basic* are the same. To explain this phenomenon,

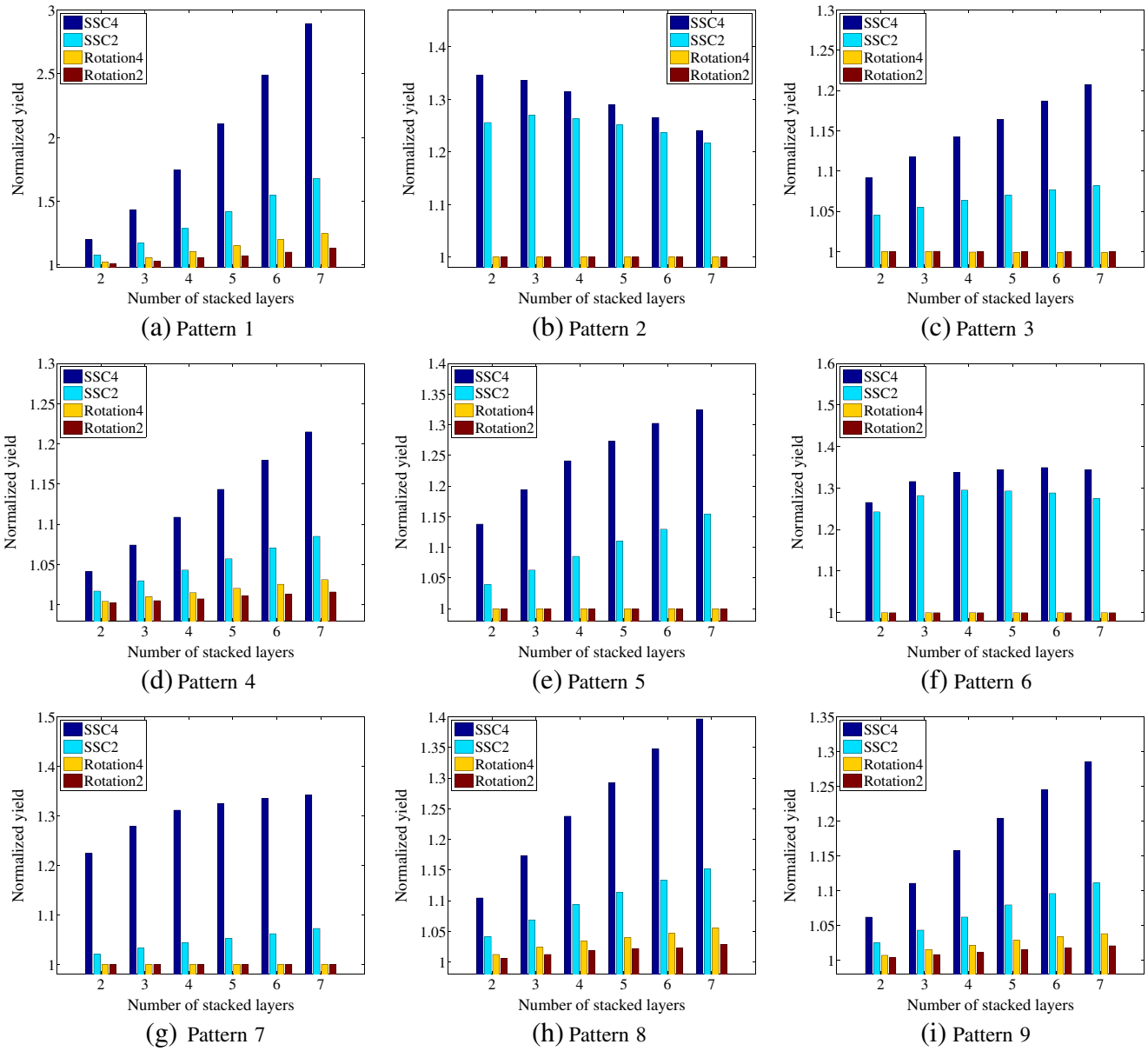


Fig. 14 Normalized yield for various stacking methods versus number of stacked layers for different defect distribution patterns of Fig. 2

let's re-examine the nine patterns. Of the nine patterns, only four of them (namely, patterns 1, 4, 8, 9) are symmetric to the wafer center while the rest of them are all shifted by some amount. It is obvious that given two wafer maps with the same probabilistically non-symmetric defect distribution, the best way to match them is not to rotate them at all. So even the wafer maps used in our experiments have the capability of four-fold rotation, the rotation method will automatically avoid any rotation. Our observations suggest that for practical wafers with various defect distributions, benefits gained from simple rotation are rather trivial.

Another interesting phenomenon is that the yield for all stacking procedures increases as repository size gets larger. This indicates relatively large repository is preferable for yield improvement. The explanation is that larger repository size provides more candidates for matching algorithms thus increasing the compound yield. Considering the extremely small repository with size 1, the wafers are stacked without any freedom for selection. However, larger repository will consume more time in matching algorithms, which correspondingly reduces the throughput.

5.3 Impact of Number of Stacked Layers on Compound Yield

In this section the impact of number of stacked layers on final compound yield is studied. The experimental results are shown in Fig. 14 where *y* axis indicates normalized yield with respect to the yield of the basic procedure under the same condition. In Fig. 14, the repository size is set to 50.

Though not shown in Fig. 14, the compound yields of all procedures decrease for larger number of stacked layers. However, as can be seen, higher improvement is gained for SSC4, SSC2 over Rotation 4, Rotation 2, and *basic*. SSC4 and SSC2 always outperform Rotation 4, Rotation 2 and *basic* especially for situations where compound yield becomes poorer (Fig. 14b is an exception). For example, in Fig. 14a, for 7-level stacks the normalized yield increases from 1.00 for *basic* [17, 21, 23] and 1.25 for Rotation 4 to almost 2.89 for SSC4, which indicates 189 % and 131 % relative increases, respectively. Note again, compared with *basic* the rotation procedure does not help at all for patterns 2, 3, 5, 6 and 7 regardless of the number of stacked layers.

5.4 Impact of Production Size on Compound Yield

Since running repository scheme is utilized in our work, repository pollution is unavoidable [21, 23]. Figure 15 shows how the yield decreases as the production size increases for different types of patterns. Note the *x*-axis indicates the number of wafers consumed for a single layer in production. The repository size is set to 25 and the number of stacked layers is selected as 3. Initially, the yield of SSC4 procedure using only one wafer per repository is pre-calculated for each type of defect distribution pattern. Then for each defect pattern, the yields for all procedures are normalized with respect to the corresponding pre-calculated values.

In Fig. 15, as the production size increases, the normalized yield for all procedures decreases and finally stabilizes. Interestingly, though yields of SSC4 and SSC2 still outperform Rotation 4 and *basic*, the yield advantages become less obvious for larger production size, especially for patterns with non-symmetric defect probability distributions. One possible explanation is that pollution is more severe for non-symmetric wafer patterns. In the later phase of the manufacturing process, the repository will be always somehow polluted. However, for symmetric defect patterns, a new incoming sector is more likely to match the rest of the unattractive sectors in the repository. For non-symmetric patterns, it is harder to get alignment of good dies. In other words, the compound yield of the selected best pair will be low. That is why the yield benefits of SSC*n* drops quickly for non-symmetric patterns.

To effectively eliminate pollution and better utilize the SSC*n* method, a new mechanism to force the unattractive wafers to leave the repository in a timely manner is needed. To our knowledge, no remedy has been proposed. Some possible solutions to reduce pollution could be:

1) Conduct running repository based matching and static repository based matching, alternatively.
2) Expunge poor wafers (quadrants) from the repository if they have not been used after a certain number of tries. Send them to a die stacking process to make some use of them.

6 Cost Effectiveness of Sector Symmetry and Cut Method

Previous sections demonstrated the benefits of SSC*n* method from aspect of compound yield. However, to decide whether SSC*n* is applicable, we need to determine the cost-effectiveness of SSC*n* method, since SSC*n* would require extra effort in wafer cutting and bonding, increasing the cost from a manufacturing perspective. The question remains whether the additional cost of wafer cutting and bonding in manufacturing can be compensated for by yield increase? We analyze the cost of a 3D IC in 3 phases: 1) testing, 2) manufacturing, and 3) packaging.

First, we consider the testing cost of 3D IC. There can be many different kinds of test flows for 3D ICs [22]. We assume an optimized testing flow from [27] to carry out the analysis. This test flow consists of three stages, 1) pre-bond

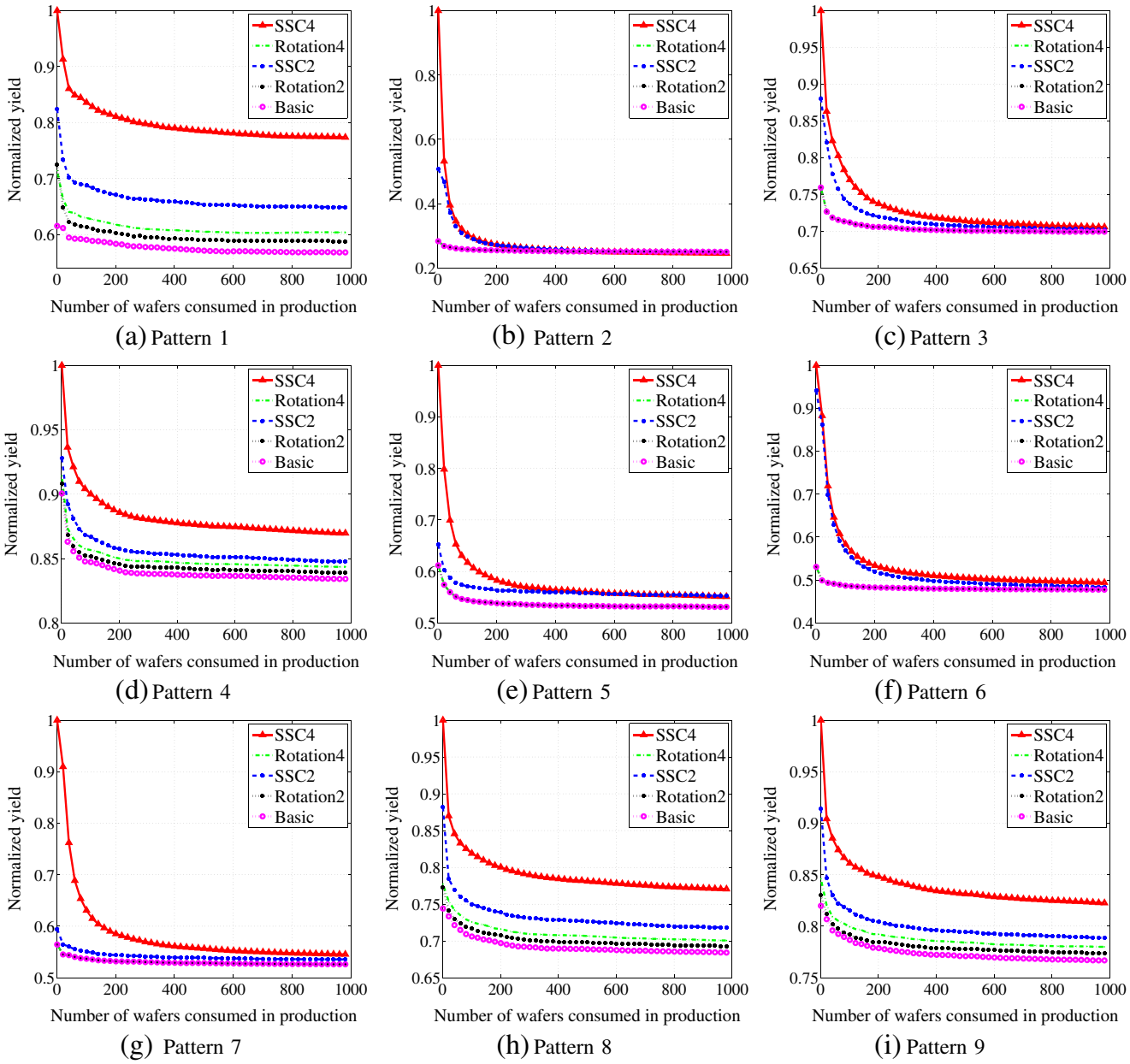


Fig. 15 Yield reduction for various defect distributions (Fig. 2) as production size increases

test, 2) post-bond test during which only the newly-formed interconnects are tested, and 3) final test after packaging assumed to cover all interconnects and dies to assure the quality of the final 3D ICs.

Costs of pre-bond test $Cost_{pretest}$, post-bond test $Cost_{postest}$, and final test $Cost_{finaltest}$ are given by Eqs. 14 through 16. These equations have similar format, i.e., number of items tested multiplied by test cost per item.

$$Cost_{pretest} = DPW \cdot l \cdot t_{die} \tag{14}$$

where t_{die} denotes the test cost of a single die. l is the number of stacked layers.

$$Cost_{postest} = DPW \cdot Y(l,k) \cdot (l-1) \cdot t_{int} \tag{15}$$

where $Y(l, k)$ is the compound yield for a stack of l layers and a repository size of k wafers. t_{int} is the test cost of the interconnect between two layers.

$$Cost_{finaltest} = DPW \cdot Y(l,k) \cdot Y_{int}^{l-1} \cdot (l \cdot t_{die} + (l-1) \cdot t_{int}) \tag{16}$$

where Y_{int} denotes the passing yield of interconnect test between two layers. The total testing cost is:

$$Cost_{test} = Cost_{pretest} + Cost_{postest} + Cost_{finaltest} \tag{17}$$

Next, we analyze the impact of wafer cutting on 3D manufacturing cost and find,

$$Cost_{manu} = l \cdot C_w + (l-1) \cdot C_{3D} \cdot (1 + cut_{num} \cdot \beta) \tag{18}$$

where C_w is the wafer cost, and C_{3D} [21] is the cost related to 3D stacking process including through silicon via (TSV) formation, wafer thinning, wafer bonding, etc. A fraction β accounts for the overhead of wafer cutting. Larger β indicates larger overhead caused by wafer cut and bonding. Note for the *basic* method in which the wafer is not cut before stacking, $cut_{num} = 1$ and $\beta = 0$.

The packaging cost is,

$$Cost_{pack} = DPW \cdot Y(l,k) \cdot Y_{int}^{l-1} \cdot t_{pack} \tag{19}$$

where t_{pack} denotes the cost of packaging a 3D IC.

The total cost is the sum of testing cost, manufacturing cost, and packaging cost:

$$Cost_{total} = Cost_{test} + Cost_{manu} + Cost_{pack} \tag{20}$$

Notice that the total cost need to be distributed over all functional 3D ICs. Here, the number of functional 3D ICs after final testing is,

$$Num_{3DIC} = DPW \cdot Y(l,k) \cdot Y_{int}^{l-1} \cdot Y_{die}^{l} \tag{21}$$

Therefore, the cost of a single functional 3D IC is,

$$Cost_{3DIC} = \frac{Cost_{total}}{Num_{3DIC}} \tag{22}$$

Based on the above cost model, we compare the 3D IC cost of SSC4 and *basic* for nine different wafer patterns. The parameters substituted in the cost model are as follows [2, 21, 27]: $k = 50$ $cut_{num} = 4$, $DPW = 812$, $t_{die} = \$0.23$, $t_{int} = \$0.023$, $Y_{die} = 99\ \%$, $Y_{int} = 97\ \%$, $C_w = \$1000$, $t_{pack} = \frac{C_w}{DPW} \cdot 0.5$.

Table 3 shows the cost analysis result. All positive numbers are in **boldface**, which indicate the percentage of cost improvement with SSC4 over *basic*. Negative numbers indicate cases where cost of SSC4 is higher. We make three observations from Table 3. First, given a certain β and number of stacking layers (l), the cost improvement of SSC4 increases as $\frac{C_{3D}}{C_w}$ decreases. This is because the negative impact of SSC4 on manufacturing cost becomes smaller as $\frac{C_{3D}}{C_w}$ decreases. Second, given a certain $\frac{C_{3D}}{C_w}$ and number of stacking layers, the cost improvement of SSC4 increases as β decreases, which is also evident in Eq. 18. These two observations suggest that the cost benefits of SSC4 become larger as the cost overhead of SSC4 become smaller. As the infrastructure of handling sectors of wafers in 3D manufacturing becomes mature, both $\frac{C_{3D}}{C_w}$ and β will decrease, and reduced manufacturing overhead of SSC4 can be expected. Third, given certain β and $\frac{C_{3D}}{C_w}$, the cost improvement becomes more significant as the number of layers (l) increases. This is because the yield improvement of SSC4 over *basic* becomes much larger when l increases as indicated by Fig. 14. At large l, the final number of good 3D ICs is much larger, thus compensating for the larger manufacturing overhead of SSC4 over *basic*.

As can seen from Table 3, for most defect distributions, SSC4 behaves very well even for very large $\frac{C_{3D}}{C_w}$ and β. Note that $\beta = 0.25$ indicates 100 % 3D manufacturing overhead of SSC4. For defect distributions 3, 4, and 9, there is a larger portion of negative numbers when $\frac{C_{3D}}{C_w} = 0.9$, which is of course the worst case condition. But as 3D technology matures, we expect smaller $\frac{C_{3D}}{C_w}$ and β in which case SSC4 is more cost-effective.

7 Conclusion

This paper deals with the problem of low compound yield in wafer-on-wafer stacking for 3D IC fabrication. We propose a manipulation method involving sector symmetry and cut (SSCn). In this manipulation method, each wafer is cut into n identical sectors that are used to replenish the repository for matching. By wafer cut, the matching restrictions for dies on a wafer are reduced and correspondingly the compound yield is improved. Extensive experiments are conducted to compare the compound yield of the proposed hybrid and SSCn procedures with existing works under various defect distributions. It is demonstrated that SSCn procedure improves the compound yield significantly irrespective of the type of defect distribution.

We derive mathematical formulas for DPS and DPW calculation for rotationally symmetric wafers. We find greater flexibility of wafer matching by sector symmetry and cut, which on the other hand induces larger die loss in turn reducing the total number of final good 3D ICs. Based on experiments, we conclude that SSC4 should be a rule-of-thumb in practice to maximize the benefit of the proposed technique. A cost model of 3D IC manufacturing is constructed and cost-effectiveness of SSCn is analyzed. It is demonstrated that SSC4 largely reduces the 3D IC cost under various defect models especially for situations where number of stacked layers is large. As 3D technology reaches maturity, even larger cost benefits of SSC4 may be expected.

The reported experiments assume that wafers used in the same stack all have the same kind of defect distribution. This may not be the case in practice since wafers from different vendors may be used for 3D stacking. Even for the same manufacturer, the fabricated wafers may have different defect distributions. More experiments are needed to study the compound yield of stacking wafers with different defect distributions. Another direction of future research is to develop a mechanism that can effectively force the unattractive wafers to leave repositories so as to reduce repository pollution. Once the problem of pollution is solved, the SSCn procedure is likely to reveal larger advantages.

Table 3 Cost improvement percentage for SSC4 over *basic* under various defect distributions (Fig. 2) and for number of staking layers (l) ranging from 2 to 6

Defect	Overhead	$\frac{C_{3D}}{C_w} = 0.3$					$\frac{C_{3D}}{C_w} = 0.6$					$\frac{C_{3D}}{C_w} = 0.9$				
pattern	β	$l = 2$	3	4	5	6	2	3	4	5	6	2	3	4	5	6
Pattern 1	0.05	**14.1**	**27.7**	**40.6**	**50.8**	**58.3**	**12.7**	**26.3**	**39.3**	**49.7**	**57.3**	**11.6**	**25.2**	**38.3**	**48.8**	**56.6**
	0.10	**12.3**	**25.8**	**38.8**	**49.2**	**56.9**	**9.5**	**22.8**	**36.2**	**46.9**	**54.9**	**7.2**	**20.6**	**34.2**	**45.3**	**53.5**
	0.15	**10.5**	**23.8**	**37.0**	**47.6**	**55.5**	**6.3**	**19.4**	**33.1**	**44.2**	**52.6**	**2.8**	**15.9**	**30.1**	**41.7**	**50.4**
	0.20	**8.8**	**21.8**	**35.1**	**46.0**	**54.1**	**3.0**	**15.9**	**29.9**	**41.5**	**50.2**	−1.7	**11.3**	**26.0**	**38.1**	**47.3**
	0.25	**7.0**	**19.8**	**33.3**	**44.4**	**52.7**	−0.2	**12.4**	**26.8**	**38.8**	**47.8**	−6.1	**6.7**	**21.8**	**34.6**	**44.2**
Pattern 2	0.05	**22.8**	**22.3**	**21.1**	**19.5**	**18.0**	**21.7**	**20.8**	**19.4**	**17.7**	**16.1**	**20.7**	**19.6**	**18.1**	**16.4**	**14.7**
	0.10	**21.3**	**20.2**	**18.7**	**16.9**	**15.3**	**18.8**	**17.1**	**15.3**	**13.3**	**11.5**	**16.8**	**14.7**	**12.7**	**10.6**	**8.7**
	0.15	**19.7**	**18.1**	**16.3**	**14.4**	**12.6**	**16.0**	**13.5**	**11.2**	**8.9**	**6.9**	**12.9**	**9.8**	**7.3**	**4.8**	**2.6**
	0.20	**18.1**	**16.0**	**13.9**	**11.8**	**9.9**	**13.1**	**9.8**	**7.1**	**4.5**	**2.2**	**9.0**	**4.9**	**1.8**	−1.0	−3.4
	0.25	**16.5**	**13.9**	**11.6**	**9.2**	**7.2**	**10.2**	**6.1**	**3.0**	**0.1**	−2.4	**5.1**	**0.0**	−3.6	−6.8	−9.5
Pattern 3	0.05	**5.4**	**7.1**	**9.0**	**10.5**	**12.1**	**4.0**	**5.5**	**7.1**	**8.7**	**10.3**	**2.9**	**4.2**	**5.7**	**7.3**	**8.9**
	0.10	**3.6**	**4.8**	**6.3**	**7.8**	9.4	**0.9**	**1.4**	**2.6**	**4.0**	**5.5**	−1.5	−1.3	−0.2	**1.1**	**2.6**
	0.15	**1.9**	**2.5**	**3.8**	**5.1**	**6.6**	−2.3	−2.7	−1.8	−0.7	**0.7**	−5.9	−6.8	−6.2	−5.1	−3.7
	0.20	**0.1**	**0.2**	**1.2**	**2.4**	**3.8**	−5.5	−6.8	−6.3	−5.4	−4.0	−10.2	−12.3	−12.1	−11.3	−9.9
	0.25	−1.6	−2.1	−1.4	−0.3	**1.1**	−8.7	−10.9	−10.8	−10.0	−8.8	−14.6	−17.9	−18.1	−17.4	−16.2
Pattern 4	0.05	**1.5**	**3.7**	**6.4**	**9.0**	**11.6**	**0.1**	**2.0**	**4.5**	**7.1**	**9.7**	−1.1	**0.6**	**3.1**	**5.6**	**8.3**
	0.10	−0.3	**1.4**	**3.7**	**6.2**	**8.8**	−3.2	−2.2	−0.1	**2.3**	**5.0**	−5.6	−5.1	−3.0	−0.6	**2.0**
	0.15	−2.1	−1.0	**1.1**	**3.5**	**6.0**	−6.4	−6.4	−4.7	−2.4	**0.2**	−10.1	−10.7	−9.1	−6.9	−4.3
	0.20	−3.8	−3.4	−1.5	**0.7**	**3.3**	−9.7	−10.6	−9.3	−7.1	−4.6	−14.6	−16.4	−15.2	−13.1	−10.5
	0.25	−5.6	−5.7	−4.2	−2.0	**0.5**	−13.0	−14.8	−13.8	−11.9	−9.4	−19.2	−22.1	−21.3	−19.4	−16.8
Pattern 5	0.05	**9.5**	**13.4**	**16.5**	**18.5**	**20.3**	**8.1**	**11.7**	**14.7**	**16.7**	**18.5**	**6.9**	**10.3**	**13.4**	**15.4**	**17.1**
	0.10	**7.7**	**11.0**	**14.0**	**15.9**	**17.7**	**4.8**	**7.6**	**10.4**	**12.3**	**14.0**	**2.3**	**4.8**	**7.6**	**9.5**	**11.2**
	0.15	**5.8**	**8.7**	**11.5**	**13.3**	**15.0**	**1.4**	**3.5**	**6.0**	**7.8**	**9.5**	−2.3	−0.6	**1.9**	**3.6**	**5.3**
	0.20	**4.0**	**6.3**	**9.0**	**10.7**	**12.4**	−2.0	−0.7	**1.7**	**3.3**	**5.0**	−6.9	−6.1	−3.9	−2.2	−0.6
	0.25	**2.1**	**4.0**	**6.5**	**8.1**	**9.7**	−5.3	−4.8	−2.7	−1.1	**0.5**	−11.4	−11.6	−9.6	−8.1	−6.5
Pattern 6	0.05	**17.2**	**20.4**	**21.8**	**22.3**	**22.6**	**16.1**	**19.0**	**20.3**	**20.7**	**21.0**	**15.2**	**17.9**	**19.1**	**19.5**	**19.7**
	0.10	**15.6**	**18.3**	**19.5**	**19.9**	**20.1**	**13.2**	**15.4**	**16.4**	**16.5**	**16.7**	**11.2**	**13.1**	**13.9**	**14.0**	**14.1**
	0.15	**14.0**	**16.3**	**17.3**	**17.5**	**17.6**	**10.3**	**11.8**	**12.4**	**12.4**	**12.4**	**7.2**	**8.3**	**8.7**	**8.5**	**8.5**
	0.20	**12.4**	**14.3**	**15.0**	**15.0**	**15.1**	**7.4**	**8.2**	**8.5**	**8.2**	**8.1**	**3.3**	**3.4**	**3.5**	**3.1**	**2.9**
	0.25	**10.8**	**12.2**	**12.7**	**12.6**	**12.6**	**4.5**	**4.6**	**4.5**	**4.1**	**3.8**	−0.7	−1.4	−1.8	−2.4	−2.7

Table 3 (continued)

Defect	Overhead	$\frac{C_{3D}}{C_w} = 0.3$					$\frac{C_{3D}}{C_w} = 0.6$					$\frac{C_{3D}}{C_w} = 0.9$				
pattern	β	$l = 2$	3	4	5	6	2	3	4	5	6	2	3	4	5	6
Pattern 7	0.05	**14.5**	**18.1**	**20.2**	**21.1**	**21.8**	**13.4**	**16.7**	**18.6**	**19.5**	**20.1**	**12.4**	**15.6**	**17.5**	**18.2**	**18.8**
	0.10	**12.9**	**16.0**	**17.9**	**18.6**	**19.2**	**10.4**	**13.0**	**14.6**	**15.3**	**15.8**	**8.4**	**10.6**	**12.2**	**12.7**	**13.2**
	0.15	**11.3**	**13.9**	**15.6**	**16.2**	**16.7**	**7.5**	**9.3**	**10.6**	**11.1**	**11.5**	**4.4**	**5.7**	**6.9**	**7.2**	**7.5**
	0.20	**9.7**	**11.8**	**13.3**	**13.8**	**14.2**	**4.6**	**5.6**	**6.7**	**6.9**	**7.2**	**0.3**	**0.7**	**1.6**	**1.7**	**1.9**
	0.25	**8.0**	**9.7**	**11.0**	**11.3**	**11.7**	**1.6**	**2.0**	**2.7**	**2.7**	**2.9**	−3.7	−4.2	−3.7	−3.8	−3.8
Pattern 8	0.05	**6.9**	**11.8**	**16.2**	**19.6**	**22.8**	**5.4**	**10.1**	**14.4**	**17.8**	**21.1**	**4.2**	**8.7**	**13.1**	**16.5**	**19.8**
	0.10	**5.0**	**9.4**	**13.7**	**17.0**	**20.3**	**2.0**	**5.9**	**10.1**	**13.4**	**16.7**	−0.5	**3.2**	**7.3**	**10.7**	**14.1**
	0.15	**3.1**	**7.1**	**11.2**	**14.5**	**17.7**	−1.4	**1.8**	**5.8**	**9.1**	**12.4**	−5.1	−2.3	**1.6**	**5.0**	**8.4**
	0.20	**1.2**	**4.7**	**8.7**	**11.9**	**15.2**	−4.8	−2.3	**1.4**	**4.7**	**8.1**	−9.8	−7.9	−4.1	−0.7	**2.8**
	0.25	−0.6	**2.4**	**6.2**	**9.4**	**12.7**	−8.2	−6.5	−2.9	**0.3**	**3.7**	−14.4	−13.4	−9.8	−6.5	−2.9
Pattern 9	0.05	**3.2**	**6.8**	**10.2**	**13.5**	**16.3**	**1.8**	**5.0**	**8.4**	**11.7**	**14.4**	**0.6**	**3.7**	**7.0**	**10.3**	**13.1**
	0.10	**1.4**	**4.4**	**7.7**	**10.9**	**13.6**	−1.5	**0.8**	**3.9**	**7.1**	**9.8**	−4.0	−2.0	**1.1**	**4.3**	**7.0**
	0.15	−0.4	**2.0**	**5.1**	**8.2**	**10.9**	−4.9	−3.4	−0.6	**2.5**	**5.2**	−8.6	−7.6	−4.9	−1.8	**1.0**
	0.20	−2.3	−0.4	**2.5**	**5.5**	**8.2**	−8.2	−7.6	−5.1	−2.1	**0.6**	−13.2	−13.3	−10.9	−7.8	−5.1
	0.25	−4.1	−2.8	−0.1	**2.9**	**5.5**	−11.5	−11.8	−9.6	−6.7	−4.0	−17.8	−18.9	−16.9	−13.9	−11.2

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Appendix

Figure 16 shows the final production size of good 3D ICs considering different number of cuts. Same setup as in Section 5.1 applies here. As we can see, in most cases four-cuts produces the largest number of good 3D ICs. Note that 2 cuts are not used in these experiments because DPW of 2 cuts is identical to that for 4 cuts. However, 2-cuts provide less flexibility in matching and will definitely yield fewer good 3D ICs than 4 cuts. Also note that 3 cuts are not used either because the DPW for 3 cuts is lower than that for 4 cuts. Besides, 3 cuts provide less flexibility in wafer matching. More experiments have been done considering different wafer sizes, die sizes, defect models, etc. Since results are similar, they are not duplicated here.

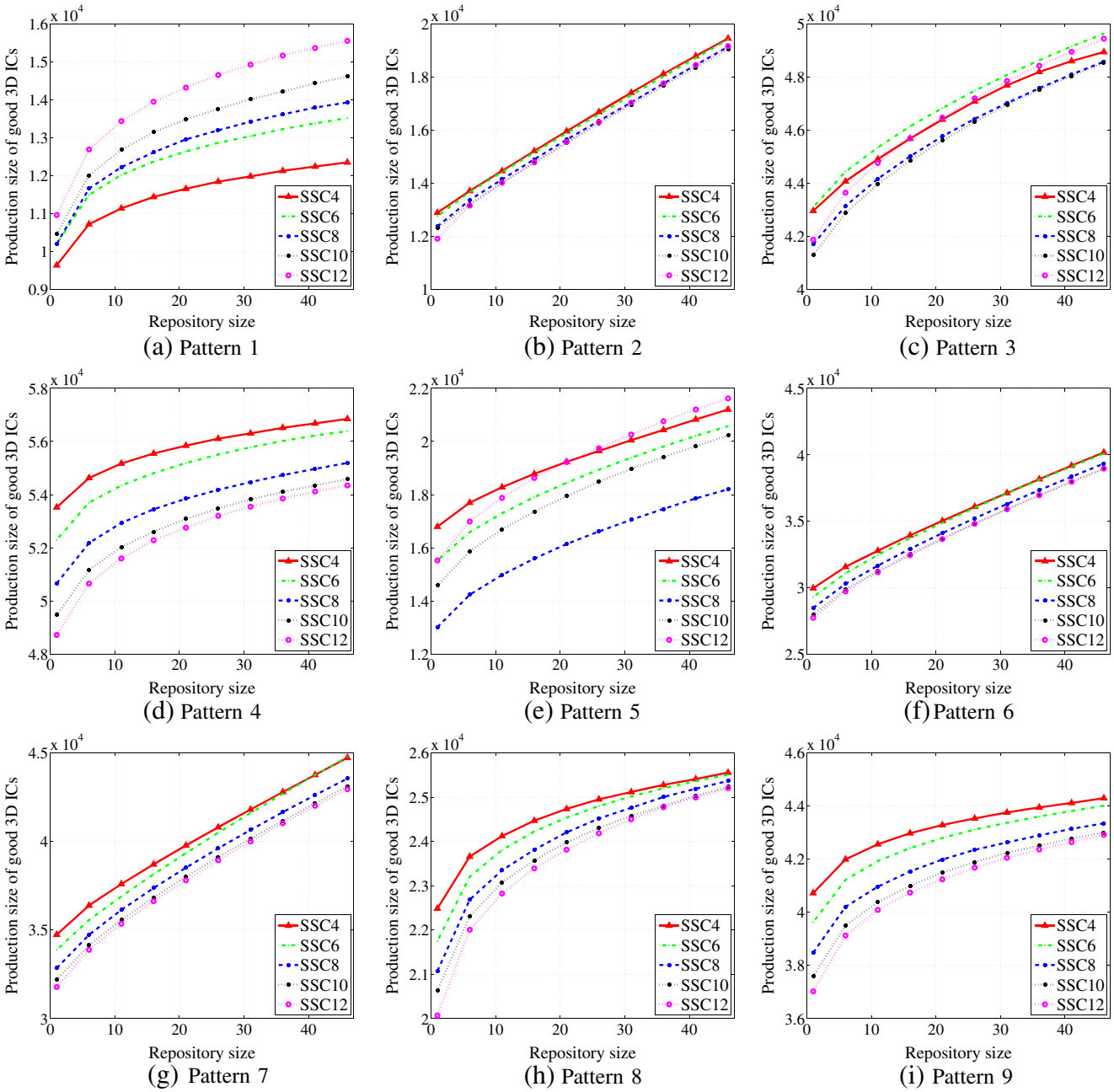

Fig. 16 Exploring the impact of number ***n*** of cuts on final production size of good 3D ICs produced by the sector symmetry and cut (SSC*n*) procedure

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